Device/Circuit/Architecture Co-Design of Reliable STT-MRAM

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Abstract— **Spin transfer torque magnetic random access memory (STT-MRAM), using magnetic tunnel junctions (MTJ) has garnered significant attention in the research community due to its immense potential for on-chip, high-density and non-volatile memory. However, process variations may significantly impact the achievable yield in STT-MRAM. To this end, several yield enhancement techniques that improve STT-MRAM failures at the bit-cell, and at the architecture level of design abstraction have been proposed in the literature. However, these techniques may lead to a suboptimal design because they do not consider the impact of design choices at every level of design abstraction. In this paper, we propose a unified device-circuit-architecture co-design framework to optimize and enhance the yield of STT-MRAM. We studied the interaction between device parameters (*viz.* energy barrier height) and bit-cell level parameters (*viz.* transistor width), together with different Error Correcting Codes (ECC) to optimize the robustness and energy efficiency of STT-MRAM cache. The advantages of our proposed approach to STT-MRAM design are explored at the 32nm technology node. We show that for a target yield of 500 Defects Per Million (DPM) for an example array with 64-bit word length, our proposed approach with realistic parameters can save up to 15% and 13% in cell area and total power consumption, respectively, in comparison with a design that does not use any array level yield enhancement technique.**

Keywords—STT-MRAM,

I. Introduction

Spin-transfer torque magnetic RAM (STT-MRAM) has emerged as a leading candidate for future universal memory technology due to its compatibility with CMOS process, high performance, near unlimited endurance, non-volatility, and high integration density [1-3] However, process variations in STT-MRAM severely impact the electrical characteristics of the magnetic tunnel junction (MTJ), the storage device, and significantly degrade the yield of STT-MRAM [4-8].

Research has begun in earnest to develop failure analysis and failure mitigation techniques to improve the yield of STT-MRAM [6]. However, the techniques published in literature are either focused on the optimization and failure mitigation at the bit-cell level [8,9,10], or on memory architecture design techniques to improve STT-MRAM yield [11,12]. As a result, the proposed techniques may lead to significant overdesign, resulting in increased power dissipation in order to meet the yield requirements. For example, let us assume that a bottom-up approach is followed to optimize STT-MRAM arrays for a specific memory array yield requirement. This places a lower bound on the bit-cell level yield. The failure mitigation methodologies targeting the bit-cell level yield do not consider array level techniques that may further improve the yield of the STT-MRAM array. Therefore, the device level parameters, which we will discuss later, are adjusted to meet the stringent reliability requirements. However, implementing array level yield enhancement techniques concurrently with the bit-cell level failure mitigation techniques may lead to acceptable array level yield and much improved energy consumption even though the bit-cell parameters are considered suboptimal by bit-cell level failure mitigation techniques. Hence, it is desirable to develop an yield enhancement technique that considers the tradeoffs of design choices at the device, memory cell, and array architecture levels to simultaneously optimize STT-MRAM for yield, performance, energy consumption, and integration density.

We propose a unified device-circuit-architecture co-design technique to improve the yield of STT-MRAM. Our technique is based on the insight that yield enhancement techniques may be implemented in multiple levels of STT-MRAM design abstraction leading to an optimized STT-MRAM memory array. Our proposed technique uses array level design techniques (such as error correction codes or ECC) to relax the design requirements at the STT-MRAM device and bit-cell levels of abstraction to mitigate failures (which we will discuss later). Consider for example, the power consumption of STT-MRAM. Write operations in STT-MRAM occur by passing bi-directional write current through the magnetic tunnel junction (MTJ) which is the storage device in STT-MRAM. The amount of write current needed is determined by the barrier height required to meet the retention time requirements [13]. Due to process variations, the actual write current supplied to the STT-MRAM bit-cell needs to be significantly higher in order to mitigate write failures [14]. As such, we can improve write energy by reducing the barrier height, which reduces retention time and increases retention failures. The retention failures (which are stochastic in nature) are then efficiently handled at the memory architecture level using proper ECC schemes [13]. In this case, data needs to be stored as a code word in the memory, which is usually longer in length than the unencoded data word. Hence, more bits need to be stored per word resulting in area overhead, additional write energy due to larger number of bits, the need to encode data, further incurring overhead in delay and energy of read operations due to the need for decoding. Furthermore, since electrical current flows through the STT-MRAM bit-cell during read operations as well, a lower barrier height may increase the chances of accidentally writing into the bit-cell during read operations. Hence,

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a careful analysis at all levels of STT-MRAM array design abstraction is required to study the feasibility of trading off retention time to reduce STT-MRAM write power consumption. Using the simulation framework proposed in this paper, we will show that different ECC schemes may be utilized to optimize the STT-MRAM array while meeting the target yield requirements. Note that redundant rows and columns may also be implemented to handle failures at the array level. We have omitted such redundancy from our analysis for simplicity. Nevertheless, the objective of this paper is to show that device-circuit-array co-design of STT-MRAM is needed to optimize the array yield and energy consumption, and is unaffected by the omission.

The rest of this paper is structured as follows. Section II presents the preliminaries of STT-MRAM. The design issues and failure mechanisms in STT-MRAM are also discussed. Then, Section III presents the modeling and simulation framework with which we evaluate our proposed device-circuit-architecture co-design technique for STT-MRAM. The ECC schemes analyzed in this work are also discussed. Results of our simulation study are then presented in Section IV. Finally, Section V concludes this paper.

II. Preliminaries of STT-MRAM

Several STT-MRAM bit-cell designs have been proposed in literature [2,3]. As seen in Fig. 1 (a,b), the STT-MRAM bit-cell consists of an MTJ and a MOSFET. Based on the connection of the MTJ and the MOSFET, one can have the standard connection as shown in Fig. 1(c) or the reverse connection as shown in Fig. 1(d).

Data is stored in STT-MRAM bit-cell as the magnetic configuration of the MTJ, which may be sensed as the resistance of the MTJ, R_{MTJ}. When the magnetization of the free layer (FL) and that of the pinned layer (PL) are *parallel*, or P, R_{MTJ} is low ($R_{MTJ} = R_L = R_P$). On the other hand, R_{MTJ} is high ($R_{MTJ} = R_H = R_{AP}$) when the FL magnetization and PL magnetization are *anti-parallel* or AP [14]. The metric used to quantify the difference in R_{MTJ} between high and low states is called the Tunneling Magnetoresistance Ratio, TMR = $(R_H - R_L)/R_L$. Also, an energy barrier, EB, is engineered into FL and PL to ensure thermal stability [15].

Operations on the STT-MRAM bit-cell occur by turning the MOSFET on and off using the word line (WL). To perform write operations, the voltages on WL, BL, and SL are set such that the current density flowing through the MTJ (called the write current density, J_{WR}) exceeds a threshold called the critical write current density, J_C [16]. Whereas J_C is directly proportional to the barrier height of FL, the direction of switching is determined by the direction of current flow [17,18]. Data stored in STT-MRAM bit-cells are read out by applying voltages on WL, BL and SL, and then comparing the current flowing between BL and SL (I_{RD}) with a reference current, I_{REF}. $R_{MTJ} = R_L$ if I_{RD} is greater than I_{REF}; otherwise, $R_{MTJ} = R_H$.

As discussed in [8], failures in the operation in STT-MRAM may occur in the presence of process variations. There are *write failures*, *read-disturb failures* and *read-decision failures*. Write failures occur because J_{WR} falls below J_C. On the other hand, read-disturb failures occur because I_{RD} is such that

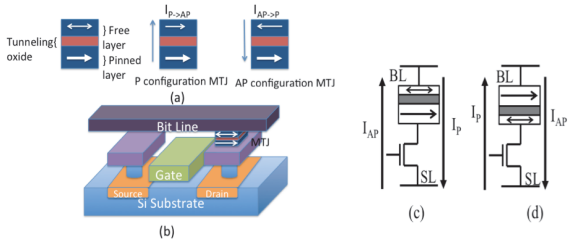


Fig. 1. (a) MTJ structure (b) bit-cell structure (c) standard connection, (d) reverse connection.

J_C is exceeded during read operations and the stored data is accidentally overwritten. Thus, increasing the access transistor width to mitigate write failures also increases the read-disturb failures. Also, limiting I_{RD} to mitigate read-disturb failures may result in slow read operations. Read-decision failure occurs when R_{MTJ} is sensed as R_{AP} when the MTJ is in P configuration, and when R_{MTJ} is sensed as R_P when the MTJ is in AP configuration. Under process variations, I_{RD} through the MTJ in AP may be larger than I_{REF}, and when I_{RD} through the MTJ in P may be smaller than I_{REF}. Hence, the state of the MTJ may not be correctly sensed.

There are also *retention failures* which can occur in STT-MRAM if thermal effects are large enough to flip the magnetic configuration of the MTJ. The stability or life time of the magnet can be represented as t_{LIFE}, which depends on the energy barrier height of the magnet, EB, given as:

$$t_{LIFE} = \frac{1}{f_0} \exp\left(\frac{EB}{K_B T}\right) \quad (1)$$

f_0 is the attempt frequency, typically assumed to be 1GHz. Although increasing EB improves retention failures, the energy barrier that needs to be overcome during write operations is also increased, resulting in increased write power dissipation.

As can be seen from the earlier discussion, there are many conflicting design requirements to meet write failure, read-disturb failure, read-decision failure, and retention failure requirements in STT-MRAM. Also, as mentioned in Section I, STT-MRAM failure mitigation techniques at various levels of design abstraction have been proposed. For example, different ECC schemes can be implemented in the array architecture to mitigate failures [19-22]. Among them, Hamming and BCH codes are widely used [20]. However, there are overheads in performance, power and area for implementing ECC. ECC schemes require extra bits to be stored. Also, data needs to be encoded prior to write operations into the array, and decoded when read out of the array. Thus, the access latency of the array may increase. However, the complexity of ECC can be reduced if the bit-cell failure rates are low. A lower ECC complexity reduces the overall overhead incurred from implementing the ECC. On the other hand, since ECC may allow for higher bit-cell failure rates, the design constraints at the device and bit-cell levels of design abstraction may be significantly relaxed. The benefits achieved by relaxing the design constraints at the device and bit-cell levels of design abstraction may outstrip the overheads due to ECC and may lead to a better overall STT-MRAM array design. However, a device-to-array architecture simulation framework is needed to evaluate our proposed approach to designing low power, robust, and high performance STT-MRAMs. In the following sections, we

TABLE I. PARAMETERS FOR MTJ

Magnetic anistropy	Perpendicular Magnetization Anisotropy
Nominal Free Layer volume	64nm x 64nm x 1nm
Oxide thickness	1nm
PMA Anisotropy Energy Barrier	$45k_BT$-$60k_BT$
Gyromagnetic Factor, γ	17.6 GHz/Oe
Saturation Magnetization, M_S	850 emu/cm^3
Damping factor, α	0.028

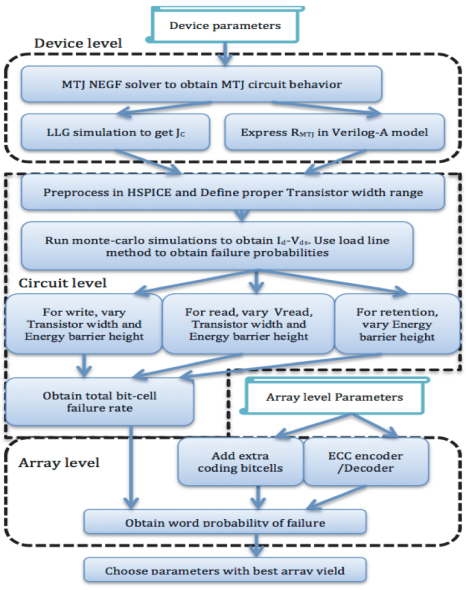


Fig. 2. Cross layer simulation framework.

will present our proposed approach to STT-MRAM design as well as the design methodologies used in this work.

III. CROSS-LAYER SIMULATION FRAMEWORK

We developed a cross-layer simulation framework that comprehends design choices made at the device, circuit, and array architecture levels of STT-MRAM design to evaluate our proposed STT-MRAM design methodology. Fig. 2 illustrates the flow of our cross-layer simulation framework.

A. Device level modeling

The device level model was adopted from the simulator published in [23], and consists of a magnetization dynamics solver and a Non-Equilibrium Green's Function (NEGF) based electron transport solver. The characteristics of the MTJ are encapsulated in a Verilog-A model [24] that may then be used to simulate the operation of STT-MRAM bit-cells using the HSPICE circuit simulator [25]. Table 1 shows the device parameters assumed for this work. Furthermore, our model is calibrated to experimental data published in the literature using other bit-cell parameters taken from [8].

We have enhanced the aforementioned MTJ model to capture the thermal stability of the device, which is characterized by the lifetime, or t_{LIFE}, of the device. t_{LIFE} is also called the retention time. The probability of retention failure in a single memory bit-cell at time t is given by [10]:

$$P_{FAIL\_THERMAL} = 1 - \cosh\left(\frac{t}{t_{LIFE}}\right) e^{\left(\frac{-t}{t_{LIFE}}\right)} \quad (2)$$

The failure probability of n bit-cells is then given by [26]:

$$P_{FAIL\_THERMAL}(n) = 1 - (1 - P_{FAIL\_THERMAL})^n \quad (3)$$

B. Circuit level modeling

The circuit level model for STT-MRAM bit-cells consists of the MOSFET model and the MTJ Verilog-A model. Together, they allow the failure probability of the bit-cell to be calculated using HSPICE circuit simulations. The method in [8] is adopted in this work for calculating STT-MRAM bit-cell failure rates. The advantage of using this approach is that the dependence of bit-cell failure rates on the device level parameters may be directly captured, which is different from the approach taken by prior works in the literature. Hence, our simulation framework is more suitable for evaluating the use of ECC (simultaneously considering device and circuit level designs) to improve the energy efficiency and robustness of high performance on-chip STT-MRAM.

C. Array level modeling

There are different methods to address reliability concerns at the array level such as utilizing ECC codes, inserting redundant rows, and scrubbing. Some of these techniques are used on each word such as the ECC codes. In contrast, others are used only after the cache size is defined, such as inserting redundant rows. Without loss of generality, we analyze the effectiveness of the ECC codes because they are applied to every word. Among different ECC schemes that are utilized in memories, Hamming and BCH codes are more widespread than others. Hamming codes, are "perfect codes", that is, they achieve the highest possible rate for codes with their block length and minimum distance of 3 [22]. Hamming codes are usually used to detect and correct only single error in the code word. However, if an additional parity bit is added, they are capable of single error correction and double (two) error detection (SECDED). BCH codes, based on binary Galois Fields, may be used if better error correction capability is needed. Binary Galois field with degree m is represented as GF(2^m) [27]. An *(n,k,t)* binary BCH code in GF(2^m) represents a code in which $n=2^m-1$, where k is the number of bits of data that is encoded and t is the number of bits the code is capable of correcting. The probability of error in the code word depends on the Galois field, the number of bits, and the desired correcting strength [27]. If single error correction is desired, the number of extra bits (*t,* on top of the number of bits in the

TABLE II. SYNTHESIZED DECODER SPECIFICATIONS

Decoder type, ECC configuration	**Hamming, (21,16,1)**	**Hamming, (38,32,1)**	**Hamming, (71,64,1)**	**Hamming, (136,128,1)**	**BCH, (26,16,2)**	**BCH, (44,32,2)**	**BCH, (78,64,2)**	**BCH, (144,128,2)**
Area (um2)	963	1370	2570	4907	1816	7924	30038	106700
Delay (ns)	0.75	0.91	1.1	1.33	0.65	0.91	1.14	3.62
Dynamic power (mW)	0.008	0.0222	0.051	0.109	0.098	0.657	2.7472	1.0919
Leakage power (mW)	0.022	0.0329	0.061	0.116	0.045	0.184	0.713	2.2346

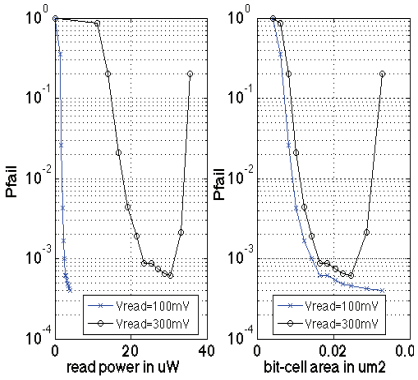
data word) is equal to that of Hamming code. If double error correction is desired, the number of extra bits increases.

ECCs have different correcting capability based on the distribution of error occurrence in the memory array. For uncorrelated error occurrences, the word failure can be modeled to have binomial distribution. The probability of error in the code word increases with increasing word length. In this work, three different word lengths (16, 32, 64) are analyzed. The additional hardware and/or circuitry required to imple ment ECC (the encoder/decoder and the extra bit-cells for storing the encoded words), are also accounted for. Note that the encoder/decoder used in this work for implementing Hamming and BCH based ECCs are found in [28] and [29], respectively.

IV. Results and Discussion

We evaluated our failure optimization methodology on a 64MB memory block with a word length of 64 bits. The bit-cells are designed using transistors from the 32nm technology [30] and MTJ with cross-sectional area equivalent to 64 nm x 64 nm. As explained in Section III, there are various design parameters that can affect the characteristics of the bit-cell. And, some of these parameters have a more pronounced impact on the failure rates. Therefore, in order to illustrate the capability of our simulation framework, we have selected the key parameters at the bit-cell level that play a significant role in the bit-cell design. The first parameter is the barrier height due to its impact on retention failures. The second parameter that was considered is the width of the bit-cell transistor. These parameters were considered to represent the required bit-cell area.

At the array level, we considered utilizing ECC codes. There are different ECC schemes that can be utilized for this purpose depending on architecture/system level requirements. We considered Hamming code with Single Error Correction and Double Error Detection (SECDED) capability and BCH code with Double Error Correction and Triple Error Detction (DECTED) capability. The ECC encoders/decoders were synthesized using the Synopsys Design Compiler. The synthesis results and the ECC block coding configurations are summarized in Table II. We analyzed three categories of failures: retention failure, write failure and read failure. We also analyzed the total failure rate with respect to different bit-cell and array level parameters.



(a) (b)

Fig. 6. Read failure rate vs (a) power and (b) bit-cell area.

A. Retention Failure Analysis

As explained previously, the retention failures depend on the thermal stability of the MTJ, which is characterized by the lifetime. Fig. 3 shows the word retention failure rates for different barrier heights and different word lengths. Note that $40k_BT$ barrier height has a failure rate close to 1. Even though $40k_BT$ is equivalent to 7.5 year lifetime (close to the required industry standard of 10 years [1]) at the bit-cell level, the word error probability is still very high. Hence, the minimum barrier height considered in this paper is kept at $45k_BT$. On the other hand, increasing the barrier height increases J_C. Furthermore, it was shown that $60k_BT$ is a reasonable barrier height for a variety of MTJ configurations [13]. Therefore, we also limited the maximum barrier height analyzed in this paper to $60k_BT$. Next, we discuss the analysis of write failures.

B. Write Failure Analysis

The bit-cell area and the energy barrier height were varied to study their impact on write failures of the array at nominal Vdd. Fig. 4 shows that the power consumption is approximately proportional to the bit-cell area. Fig. 5 shows the word failure probability vs. effective bit-cell area. The effective bit-cell area is the total area of all bit-cells normalized to the number of unencoded data bits stored in the array. The encoder/decoder area which was presented earlier has been excluded in this analysis. Note that for a fixed effective bit-cell area, the failure rate increases with the barrier height because J_C is increased. Thus, increasing the effective bit-cell area increases J_{WR} and reduces the write failure rate. However, the write

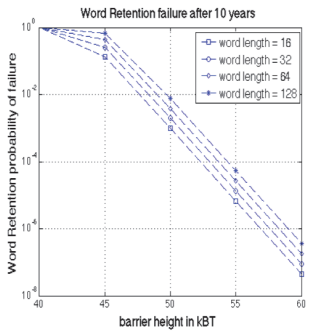


Fig. 3 . Retention failure vs. barrier height.

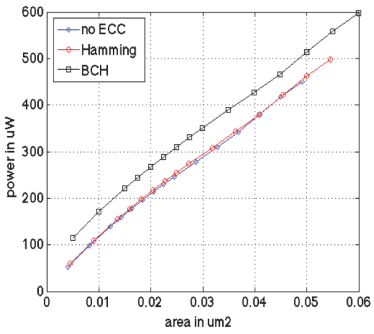


Fig. 4. The effective bit-cell write power vs bit-cell area.

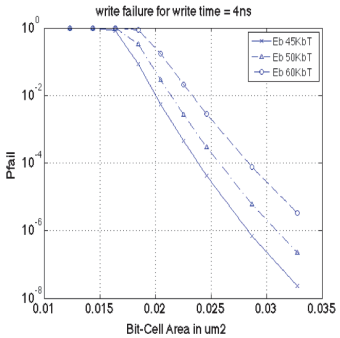


Fig. 5. Probability of write failure for different barrier heights.

power increases. A lower barrier height is preferred to reduce the write power consumption.

C. Read Failure Analysis

Next, the relationship between read voltage, the bit-cell area and read failures of the array is studied. Since the read power changes with bit-cell area, the failure rate is plotted against power and bit-cell area in Fig. 6 for the barrier height of 45 k_BT. Observe in Fig. 6 that for both read voltages, the failure rate decreases with an increase in area. This is due to the enhancement in the TMR of the bit-cell. On the other hand, read-disturb failures increase if Vread is increased from 100mV to 300mV, or if the bit-cell area is too large.

D. Overall Reliability Analysis

Finally, we show that read, write and retention failures need to be jointly considered to truly optimize the word failure rate. In our analysis, we consider 4ns delay for read and write operations. Also, the total power is calculated by giving equal weightage to read power and write power (i.e., equal probability of '0' and '1' in data, and equal probability of read and write operation occurrence).

Fig. 7 and 8 show the total bit-cell failure rate for different barrier heights and bit-cell areas without and with ECC, respectively. The total failure rate consists of retention, write and read failures. The figures show that as the bit-cell area increases, the probability of error decreases. Furthermore, the decrease is more pronounced when the MTJ barrier height is low compared to when its barrier height is high. This is be cause write failures are dominant and the rate at which write failures decrease with increasing bit-cell area is different as was shown earlier in Fig. 5. Note also that the total failure probability saturates after the bit-cell area is increased beyond a certain value. Furthermore, the total failure probability for different MTJ barrier heights saturate at different values–the saturation value is higher for lower barrier height. This occurs because retention failures become the dominant failure mechanism when the effective bit-cell area is large. Observe from Figs 5 and 6 that if area is increased, the failure rate decreases. This is due to larger write current improving write robustness and improvement in TMR in the case of read. On the other hand, the retention failures purely depend on the device parameters and not on the bit-cell circuitry parameters; therefore, they remain constant regardless of changes in the bit-cell area. Hence, total bit-cell failures may be dominated either by write and read failures or by retention failures.

Let us now consider some simple design examples. When ECC is not used and the effective bit-cell area is constrained to 0.025μm^2, Fig. 7 shows that the best achievable failure rate is 3e-3 using MTJs with 60 k_BT barrier height. Therefore, if the array level enhancements are not considered at the bit-cell level of abstraction, the barrier height can be set to 60 k_BT. However, if ECC is implemented to enhance the failure rate, Fig. 8 shows that the best possible failure rate is 2e-5 using the BCH code. Interestingly, a barrier height of 50 k_BT can achieve this failure rate instead of 60 k_BT. Let us point out that if we were to design the bit-cell and the ECC at different levels of abstraction without considering them jointly, as mentioned previously, the choice of barrier height at bit-cell level would be 60 k_BT and the best possible failure rate after ECC application would be 2e-4, which is an order of magnitude higher than the best possible failure rate when our methodology is used. This is due to the alteration in the barrier height from 60 k_BT to 50 k_BT when ECC is applied. In order to thoroughly understand the reason for this alteration in barrier height, let us emphasize that the area represented in Fig. 7 is solely the bit-cell area of an individual bit-cell consisting of the MTJ and the bit-cell transistor. In contrast, the effective area in Fig. 8 not only represents the individual bit-cell area, but also represents the area required for ECC overheads such as additional bit-cells.

Therefore, in Fig. 7, since the area is constrained to 0.025μm^2 the only available choice to tune the failure rate is changing the barrier height; and since the area is positioned such that the retention failures dominate, the barrier height should be increased.

On the contrary, in Fig. 8, the total area of 0.025μm^2 can be utilized by the individual bit-cells together with the ECC overheads. Therefore, each individual bit-cell can have a smaller area with increased write failure; yet, extra bits for ECC are inserted to compensate for the increased failure rate. Thus, unlike the previous case, the individual bit-cell is positioned at the write and read dominated region, therefore, decreasing the barrier height would decrease the failure rate.

Note, by considering the bit-cell level and array level considerations jointly, lower failure rate can be achieved for a specific area constraint. Also note, from Fig. 4, however, that

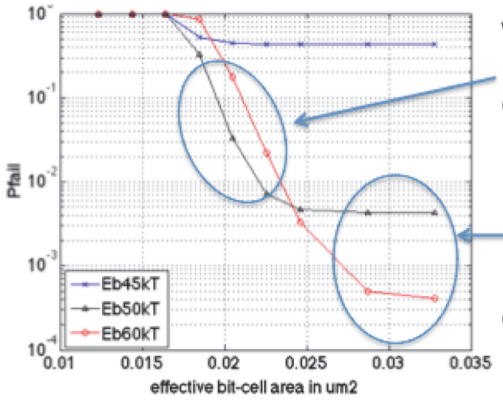


Fig. 7. Word Probability of Error vs. bit-cell area-no ECC.

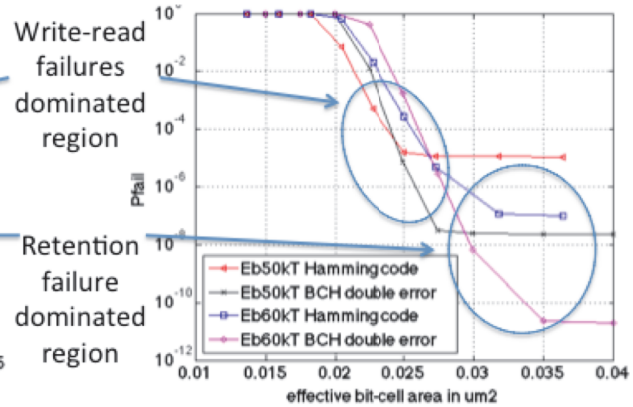


Fig. 8. Word Probability of Error vs. bit- cell area with ECC.

since BCH coding is used, the write power increased by 30%-40%. On the other hand, if Hamming code is utilized instead of BCH code, the failure rate would increase to 4e-5 and the power overhead would be reduced to 5%.

Let us now consider the case when the design is constrained by the desired failure rate instead of the effective bit-cell area. For a target failure rate of 4e-4, the barrier height needed to achieve the target failure rate without ECC is $60k_BT$ with an effective bit-cell area of $0.0325\mu m^2$ (see Fig. 7). If ECC is used, the minimum area that achieves the target failure rate is $0.0262\mu m^2$ if BCH code is used and is $0.025\mu m^2$ if Hamming code is used. However, the effective bit-cell area to achieve the same target failure rate may reduce further by reducing the MTJ barrier height to $50k_BT$. The minimum effective bit-cell area ($0.0228\mu m^2$) is achieved using Hamming code instead of BCH code. This is because the area overheads for Hamming code is less than that of BCH code.

From the two aforementioned design examples, we can observe that the STT-MRAM design needs to be optimized by jointly analyzing the device, circuit and architecture level considerations. The conventional wisdom of optimizing the STT-MRAM design separately at each level of design abstraction may lead to significant over-design. Using our proposed approach, the array failure rate may be reduced by two orders of magnitude as compared to the conventional design at iso-array area. Moreover, for a given target failure rate, our approach achieves 13% smaller array area as compared to the conventional approach.

V. Conclusion

In this paper we proposed a device/circuit/architecture simulation framework and co-design methodology for STT-MRAM. Our simulation framework consists of a MTJ device level simulator, a bit-cell failure analysis model, and an array level ECC simulator. We first calibrated our simulation framework to device characteristics that were experimentally obtained and published in the literature before using it to evaluate a 64MB STT-MRAM array with 64-bit word length. The memory array was optimized by varying bit-cell parameters in conjunction with different ECC schemes. In our analysis, we found that the conventional design methodology where the bit-cell and array level designs are separately optimized yield sub-optimal designs. We found that significant improvements to the array design may be obtained using our proposed device/circuit/array co-design methodology. At iso-array area, our methodology achieved two orders of magnitude reduction in total failure rates. Moreover, our methodology can achieve 13% smaller array area at the same total array failure rate. Hence, device/circuit/array co-design is crucial for achieving dense, energy efficient and robust STT-MRAM arrays.

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