High Performance Single Supply CMOS Inverter Level up Shifter for Multi–Supply Voltages Domains

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***Abstract*—A single supply CMOS inverter level shifter (ssqc–ls) for upconverting signals from 0.4V–1V logic level range up to 1.1V power supply domain is introduced. For guaranteing a low energy consumption, the proposed shifter is based on topological modifications of the structure qc–level shifter reported in [1]. For 0.5V input square wave switching at 500MHz, the inverter level shifter ssqc–ls using 1.2V of power supply voltage achieves a 60% of Figure of Merit improvement in comparison against jy–ls [8] with a dual power supply voltage of 0.6V and 1.2V. Post–layout simulation results shown that ssqc–ls reaches a propagation delay of 0.75ns, an energy consumption of only 2.3pJ, and an energy–delay product of 1.73pJns for a capacitive loading condition of 950fF.**

I. Introduction

In digital CMOS technology, the dynamic energy consumption is proportional to the square of the power supply voltage, and therefore, the supply voltage reduction offers the most effective way of obtaining high performance portable electronic systems. As the device density in a die increases, multiple–supply voltage design technique is normally used in high–end low–energy Systems on Chips (SoCs). Performance–critical devices use higher supply voltages while other devices operate at low supply voltage. However, in multiple dynamic supply voltage designs, the supply voltage of each power domain dynamically changes according to the energy mode, even some power domains may be shut down completely. At the interface between multiple supply voltage schemes a level shifter is used to convert the signal levels. The power overhead of these circuits is taken into account at the design planning stage.

Voltage stress between any two terminals of the transistor degrades the performance, significantly. This includes hot carrier degradation, negative bias temperature instability and gate oxide damage. In addition, the problem of stress on the switching transistors becomes greater at increasing speeds. Therefore, conventional voltage level shifter is not suitable for high voltage power supply due to the reduced breakdown voltage of the devices (NMOS and PMOS transistors). Although stacked high voltage devices are used to solve this issue, the level shifter will have DC leakage current and internal high voltage swing problems. For averting the hot carriers and gate–oxide breakdown of devices, as long as technology process shrinks, demands that voltage of the core logic drops off too.

Developing strategies to significantly reduce the energy consumption of the level shifters is necessary, since this will lead to a major reduction in the overall dissipation of the chip. In [2] a Symmetrical Dual Cascode Voltage Switch which improves speed of operation and reduces power consumption as compared to the traditional level converter was proposed. A dynamic logic–level converter was presented in [3] which is very insensitive to the variation in fabrication process, and has fast transition time in converting the logic–level. Also in [3] a dynamic logic–level converter for duty ratio conserving was shown.

Typically, level converters are important building blocks in power management systems. Two fast level shifters used for controlling the output stage of 5V DC–DC buck converters were presented in [4]. They are very robust against power supply ringing. Dhruva et al. has proposed the application of a dual–oxide thickness (DOXCMOS) technique for level–up/down conversion and blocking of the input signal [5].

Multiple Dynamic Supply Voltage is a technique that assures high performance whilst changing the supply voltage dynamically—between nominal supply, reduced supply, and turned off—for a circuit clustered in a power domain. The insertion of level up shifters is necessary and impacts on energy consumption and delay in the design [6] and [7]. Thus, in this paper, we present a voltage level converter for high capacitive load (950fF) in order to minimize the energy consumption in an integrated circuit using UMC L65N Logic/Mixed–Mode/RF–LL CMOS technology.

The remainder of this work is organized as follows. Section II describes the circuit structure for the proposed single supply CMOS inverter level up shifter (*ssqc–ls*). Performance is discussed and evaluated in Section III. Moreover, Section IV consideres the post–layout analysis for *ssqc–ls*. Finally, Section V draws the conclusions based on previously presented results.

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II. The Single Supply Inverter Level Up Shifter Circuit Topology

Level shifters account for a significant fraction of the energy consumption of a multiple supply voltage chip and are critical for high performance designs. They are used to interface blocks operating at different supply domains.

A low power and high speed level converter using extra cross–coupled pair as the conventional level shifter is shown in Fig. 1. Resistance R1 and R2 and the gate capacitance of MP3 and MP4 delay the switching time of MP3 and MP4 in respect to MP1 and MP2, respectively [8]. However, this feedback–based level converter consumes significant short–circuit and dynamic switching energy.

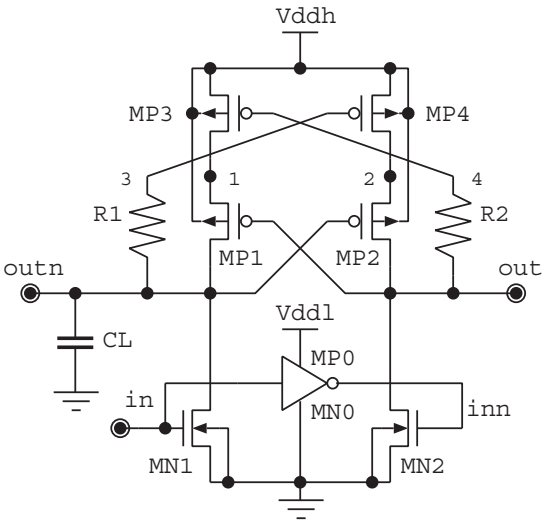

Fig. 1. The circuit diagram of *jy–ls*.

The main objective of this paper is to improve the energy consumption, and reduce complexity by employing a single supply inverter up converter. Fig. 2 shows *ssqc–ls* for high performance application, this converter has fast transition time in converting the logic level, and its energy consumption is smaller than that of *jy–ls* [8]. It is remarkable to realize this topology is obtained by making some modifications of that reported in [1] and also considering the proposed circuit in [9].

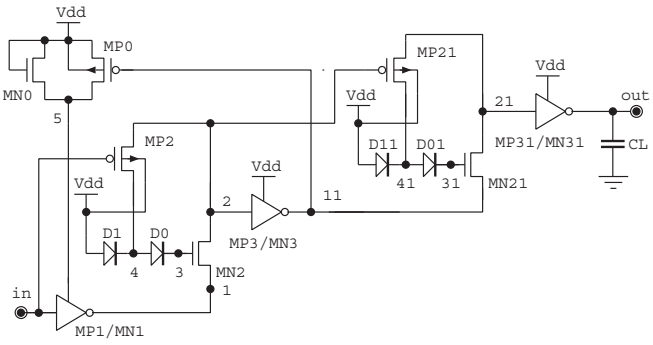

Fig. 2. Schematic for *ssqc–ls* inverter level up shifter.

In Fig. 2, inverter low–to–high converter is a circuit that converts the incoming square wave signal from a low–voltage swing to a higher–voltage swing, which is the voltage at which it is used by its load —Vdd domain. Our *ssqc–ls* minimizes area, energy consumption, and delay penalties caused by level converters in a multiple–supply system.

The operation principle is understood by observing that *ssqc–ls* uses a cascade design with two conversion stages, each of which requires the same supply voltage (Vdd). The first stage, between node in and node 11, facilitates a low–to–high transition; and the second one, between node 11 and node out, makes a high–to–low transition ensuring reliable, fast, and energy efficient operation from UMC $65nm$ CMOS low threshold voltage transistors.

The required voltage output level is generated as follows. When node in is at high level, transistor MP2 is turned off and inverter MP1/MN1 switches node 1 to low. Initially, transistors MN0 and MP0 are in on state connecting node 5 to almost Vdd. As MN2 is turned on due to the positive voltage applied to diode–connected transistors D0 and D1, it sets node 2 to low, and inverter MP3/MN3 switches node 11 to high (MP0 is turned off).

Note that node 11 does not achieve the high voltage level Vdd for a high capacitive load CL. Thus, an auxiliary level shifting is necessary, as shown in Fig. 2, where node 21 is fixed to high logic level through MP21 (MN21 is in off state) and node out is switched to ground by inverter MP31/MN31, discharging the capacitive load CL.

If node in is set to low logic level, inverter MP1/MN1 switches node 1 to high. In that case, MN2 is turned off and node 2 is fixed to high logic level due to MP2 is set on. Since inverter MP3/MN3 switches node 11 to low, the voltage at node 21 is pulled down to ground through MN21 (MP21 is in off state) and transistor MP0 is set on. Due to proper biasing of inverter MP31/MN31, node out is pulled up to Vdd.

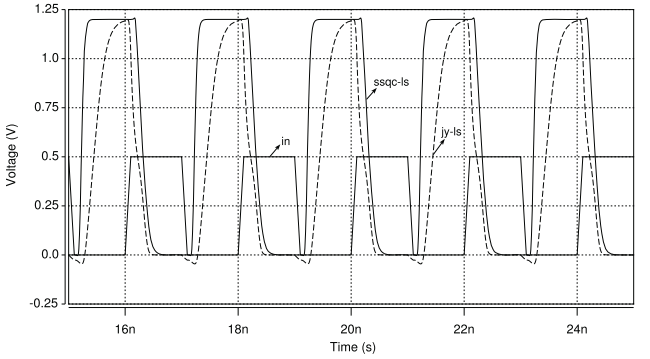

Fig. 3. Pre–layout simulation waveforms for *jy–ls*, and *ssqc–ls*. A 950fF load capacitance is attached to the output.

Fig. 3 shows the pre–layout simulation waveforms of both level shifters *ssqc–ls* and *jy–ls* at 500MHz with 950fF load on the output port for Vddl=0.6, and Vddh=1.2V=Vdd. The

input signal is a 0.5V square wave. Our level converter (*ssqc–ls*) upconverts a 0.4V–1V input range to 1.2V and inverts it.

III. Performance Analysis

Both circuits were designed using 65nm CMOS technology from UMC, and the layout for *ssqc–ls* was implemented. For the sake of a fair comparison, we optimized the two level converters in the energy–delay design space. Table I shows the transistor dimensions and types. The multiplier factor indicates the number of transistors in parallel connection. Note that the sizing for *jy–ls* is different with respect to the dimensions used in [8], because it has been designed in order to show the lowest delay and energy per transition.

TABLE I
Channel widths for transistors in *jy–ls*, and *ssqc–ls*.

jy–ls (Active area=42.25μm^2)		
Transistor(s)	Type	Width (μm)
MP0	P	5 × 10.0
MP1 and MP2	P	4 × 10.0
MP3 and MP4	P	2 × 10.0
MN0	N	6 × 10.0
MN1 and MN2	N	21 × 10.0
ssqc–ls (Active area=35.71μm^2)		
Transistor(s)	Type	Width (μm)
MP0	P	1 × 0.4
MP1 and MP21	P	2 × 0.25
MP2 and MP31	P	5 × 10.0
MP3	P	2 × 10.0
MN0, MN2, MND1 and MND11	N	1 × 10.0
MN1	N	5 × 10.0
MN3	N	3 × 10.0
MND0 and MND01	N	8 × 10.0
MN21	N	14 × 10.0
MN31	N	2 × 4.0

The channel length for all transistors is 65nm.

As shown in Table I, our circuit *ssqc–ls*, provides a 21% saving in active area in respect of *jy–ls*. MND0, MND1, MND01, and MND11 represent the diode–connected transistors D0, D1, D01, and D11, respectively for *ssqc–ls*. Core area for *ssqc–ls* is approximately 22.41μm × 10.87μm. Our level converter reduces the complexity in physical design. Simulation results illustrate that as capacitive load CL increases delay and energy also increases. The speed for *ssqc–ls* is a 23.4% higher at 950fF load compared to *jy–ls* with R1 and R2 equal to 10Ω.

The energy consumption is decreased in *ssqc–ls* up to a 48% (see Fig. 4), and energy–delay product is optimized by a 60% (see Fig. 5) at 950fF. The pre–layout results for *ssqc–ls* have confirmed the successful operation at 500MHz with 950fF load on output port, and a wide input voltage range. Nevertheless, for determining the circuit performance and robustness the layout was implemented and the parasitic components extracted. It is advisable not to set the input signal lower than 0.5V for *jy–ls* because it does not work. In the case of *ssqc–ls*, when the input signal is a square wave of 0.4V, it achieves 1.2V at the output with a maximum capacitive load of 950f. The value of propagation delay time obtained is 0.3ns, energy 2.15pJ, and energy–delay product 0.64pJ×ns. Performance for *jy–ls* gets worse as the value of R1 and R2 increases over 10Ω.

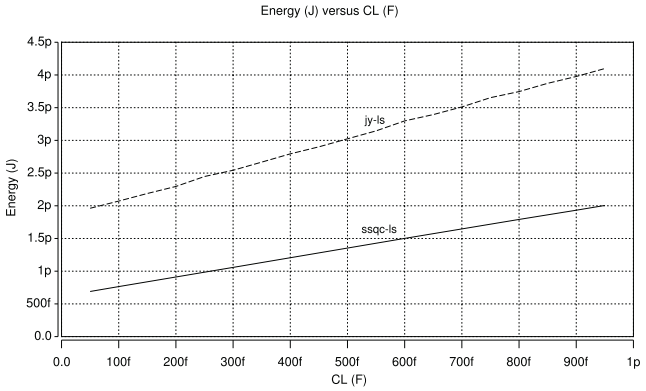

Fig. 4. Energy versus capacitive load CL variations for upconverting 0.5V to 1.2V domain.

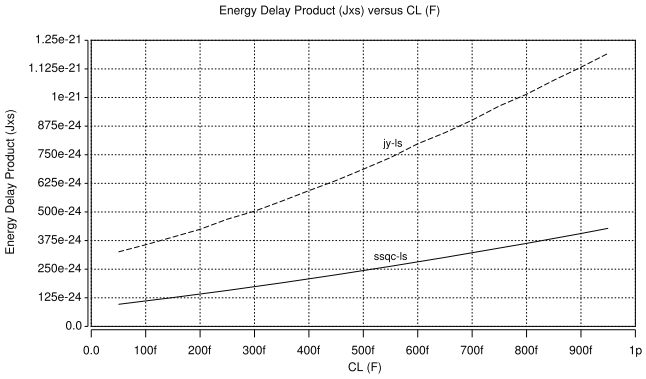

Fig. 5. Energy–delay product versus capacitive load CL variations for upconverting 0.5V to 1.2V domain.

IV. Post–layout analysis for *ssqc–ls* circuit

Energy consumption reduction in a level shifter is the most demanding issue for present integrated circuit design. In order to reduce static DC current *ssqc–ls* is proposed between a low voltage driver circuit and a full voltage level receiver circuit. To verify its effectiveness and capabilities, we implemented the layout for *ssqc–ls*. Thus, the simulated post–layout results of *ssqc–ls* for Vdd=1.2V, and the input signal at 500MHz with a load capacitance CL ranging from 50fF to 950fF are shown in Fig. 6.

To see how input signal range and capacitive load affect the overall performances for *ssqc–ls*, Fig. 7 is introduced. The charging and discharging current of parasitic capacitances in *ssqc–ls* dominates both propagation delay and energy consumption, as is shown in Fig. 7. In addition, energy–delay product becomes largely dependent of the voltage shift.

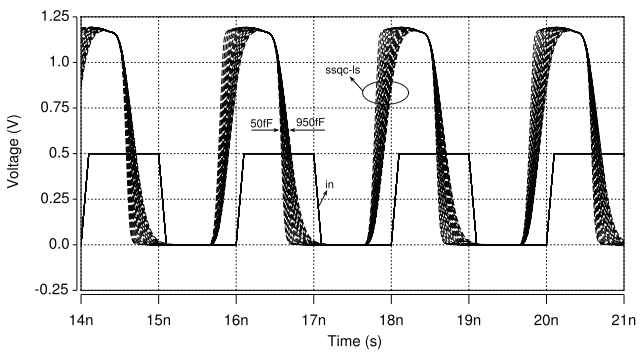

Fig. 6. Output waves obtained with 0V–0.5V input voltage for post–layout simulation of *ssqc–ls* versus CL from 50fF until 950fF, adding steps of 50fF, respectively.

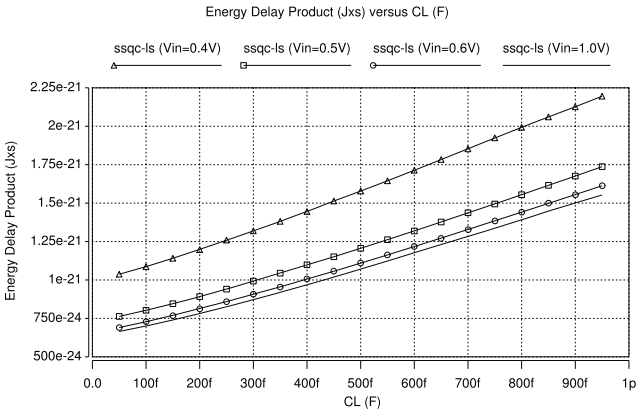

Fig. 7. Energy–delay products versus loading for post–layout simulation of *ssqc–ls* converting 0.4V, 0.5V, 0.6V, and 1V inputs into 1.1V output signal, respectively.

It is worth remembering that better energy–delay product than that shown in Fig. 5 for *ssqc–ls* would not have been posible to achieve due to the significant value of parasitic capacities. The conversion for 0.7V–0.9V input range is not shown in Fig. 7 for clarity, the result for these inputs is very close to that for 1V. The worst case measured energy–delay product is for a square wave input of 0.4V. Results show that *ssqc–ls* interfaces low to high voltage domains, i.e. from 0.4V–1V input signal voltage range to 1.1V output signal voltage.

The robustness of *ssqc–ls* was evaluated under process variations. As is illustrated in Fig. 8, Monte Carlo simulations with 30 samples were run to produce the histogram of the energy–delay product for each CL between 50fF and 950fF. The energy–delay product distribution is wider as the value of CL is increasing. By adjusting of the input signal voltage range to the operating power supply voltage domain and the threshold voltage of the devices, the proposed circuit is scaled with the technology process.

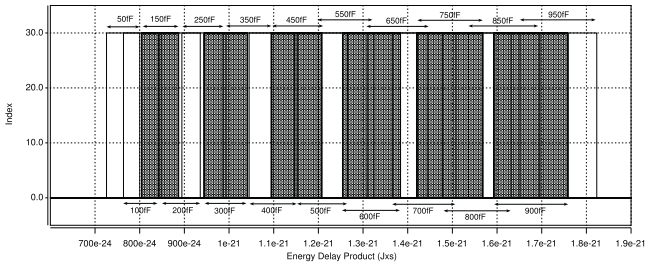

Fig. 8. Histogram for each energy–delay product of *ssqc–ls* converting 0.5V input into 1.1V output signal and CL ranging from 50fF to 950fF.

V. Conclusions

A new single supply level up shifter for high capacitive load (950fF), termed *ssqc–ls*, is proposed to address the important limitation on energy consumption for a System on Chip. Pre–layout simulation results in UMC CMOS 65nm process demonstrate that using an input signal amplitude of 0.5V our proposed *ssqc–ls* achieves a 60% reduction in Figure of Merit at 950fF capacitive load as compared to *jy–ls* [8]. Post–layout simulations show *ssqc–ls* is capable of shifting a 0.4V–1V input logic range up to 1.1V. In addition, the robutness of *ssqc–ls* was evaluated under process variations by Monte Carlo analysis when the capacitive load CL changes from 50fF to 950fF. Therefore the proposed level up shifter is suitable for using in low energy consumption and high speed applications.

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