Operational Fault Detection and Monitoring of a Memristor-Based LUT

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***Abstract*— This paper presents a method for operational testing of a memristor-based memory look-up table (LUT). In the proposed method, the deterioration of the memristors (as storage elements of a LUT) is modeled based on the reduction of the resistance range as observed in fabricated devices and recently reported in the technical literature. A quiescent current technique is used for testing the memristors when deterioration results in a change of state, thus leading to an erroneous (faulty) operation. An equivalent circuit model of the operational deterioration for a memristor-based LUT is presented. In addition to modeling and testing, the proposed method can be utilized also for continuous monitoring of the LUT in the presence of memristor deterioration in the LUT. The proposed method is assessed using LTSPICE; extensive simulation results are presented with respect to different operational features, such as LUT dimension and range of resistance. These results show that the proposed test method is scalable with LUT dimension and highly efficient for testing and monitoring a LUT in the presence of deteriorating multiple memristors.**

Keywords—Memristor, testing, deterioration, monitoring, quiescent current.

I. INTRODUCTION

Non-Volatile (NV) flash memories have been used as external storage to Field Programmable Logic Gates (FPGA) for storing the configuration bits, because Static Random Access Memory (SRAM) based FPGAs are unable to retain the configurations bits when power is lost [1]. However CMOS-based flash memories incur in a large cost, extensive area overhead and low data retrieving time; these issues can be overcome by utilizing NV memories, such as the memristor. Among emerging NV memories, the memristor is considered to be a promising candidate due its fast speed, small area, technology scalability and low power consumption [2]. However, endurance is very problematic; experimental data from HP [3][4] shows that as the number of switching cycles increases, the high value of the resistance of a memristor reduces until it becomes equal to the lowest value. Thus if used in a LUT [5] [6], resistance deterioration of the memristors (as resistive elements for storage) may affect the correct functionality at operational time. A proper circuit-level modeling of the deterioration process and test of the memristors are required, because at operational time, the LUT may undergo significant changes in functionality (this is of course compounded by the possible process variability in the resistances of the memristors following manufacturing).

A memristor can be affected by manufacturing as well as operational faults. Manufacturing faults are mostly caused by imperfection in the fabrication process, such as stuck-at and bridging faults. Fault detection and location are then used for yield improvement. At the nanoscales, faults occurring during the operational lifetime are usually identified with the changing characteristics of devices, such as associated with aging and variations. It is well known that nanoscaled MOSFETs are affected by so-called PVT (process/voltage/temperature) variations that may alter the operation of a circuit; experimental data has shown that a variation in resistance of a memristor occurs when the number of switching cycles increases [3] [4].

Fault detection of hybrid CMOS memristor memories for manufacturing faults has been presented in [7]-[9]. Defect-oriented testing is pursued by electrical stimulation; faults such as open, short, bridging and the undefined-state are considered in [7]. An approach based on the Bose–Chaudhuri–Hocquenghem (BCH) codes has been presented in [9] and allows taking into account a wide range of defects and permanent/transient faults; however, the hardware overhead is significant if a large number of faults/errors must be detected.

To the best knowledge of the authors, deterioration of memristors and the resulting operational faults in a circuit (such as a LUT) have not been addressed in the technical literature. The recent endurance trials performed at HP Labs has shown that after a few thousand switching cycles, a memristor degrades significantly and its behavior resembles a stuck-at fault [3][4]. Fig.1 shows the deterioration of the resistance of a memristor [3]; R_{OFF} (the high resistance value of a memristor in the off state) is reduced to the R_{ON} value (the low resistance value of a memristor in the on state) following a number of switching cycles. As result of the resistance deterioration, the switching behavior of the memristor is permanently lost (this is therefore referred to as a *faulty memristor)*. So, detection of faulty memristors is needed at operation time, i.e. when the memristor-based LUT is operating within an FPGA.

This paper focuses on testing, monitoring and modeling the operational deterioration of a memristor-based LUT; a quiescent current technique is proposed for testing the LUT in the presence of variation of the resistances. In this paper,

testing is accomplished by observing the output pattern of a current comparator; the conditions by which either deterioration, or variation of the resistance allow detection of the erroneous state of at least a memristor, are established. Furthermore, extensive results are presented with respect to different operational features, such as LUT dimension (hence the number of inputs in the LUT) and range of resistance. These results show that the proposed method is scalable with LUT dimension and efficient for testing/monitoring at operational time a LUT in which the memristors undergo a resistance deterioration.

This paper is organized as follows. Section II outlines the principles behind the proposed testing approach, while Section III deals with the scenario of single memristor deterioration (inclusive of additional features such as monitoring), Section IV describes the effect of global deterioration (i.e. multiple memristors); Section V concludes this manuscript.

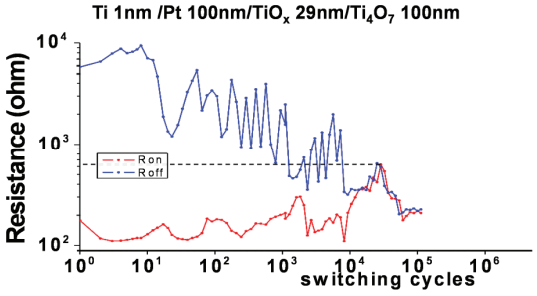

Fig. 1 Memristor endurance experiment (resistance vs number of switching cycles) by HP labs, [3]

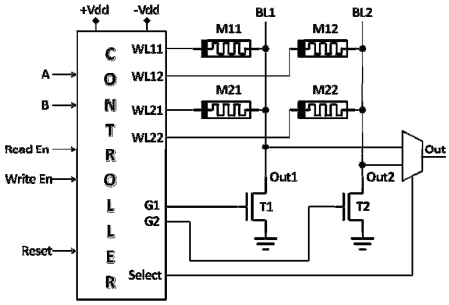

Fig. 2 LUT architecture (two-input) implemented using memristors as proposed in [6].

II. Test Principles

The approach proposed in this paper is based on the quiescent current measurement of a LUT in an FPGA; this type of testing has been already successfully applied to FPGAs in the past [13]. Different from [13], only the operational deterioration of the memristors for the LUT architecture of [6] (Fig. 2) is considered in this paper. The LUT architecture of [6] consists of an array in which all memristors in a column are connected to a load (given by a controlling MOSFET); a memristor in a column is connected to no memristor in different columns, i.e. the memristors are not connected row-wise. Also in this architecture, it is possible to write to all cells (memristors) of the LUT at once. The interested reader should refer to [5] [6] for more details about this memristor-based LUT. The write and read operations for the selected memristor (in this case M11) require different voltages to be applied; they are shown in Table 1.

Table 1 Voltage requirements for the write and read operations on the selected memristor (M11) using the method of [6].

	WL11	WL12	WL21	WL22	BL1 Voltage	BL2 Voltage
Write 1	V_{dd}	*Floating*	*Floating*	*Floating*	*GND*	*Floating*
Write 0	$-V_{dd}$	*Floating*	*Floating*	*Floating*	*GND*	*Floating*
Read	$\pm V_{dd}$	*Floating*	*Floating*	*Floating*	*GND*	*Floating*

To illustrate the proposed approach, consider the first column of cells in the LUT of Fig.3 with three memristors (M1, M2, and M3) connected to the load NMOS transistor (T_1). Assume that all memristors are fault free (no deterioration) and they are in the R_{OFF} state; a write 0 operation to all memristors is executed. A read pulse is then applied to the inputs of the memristors (WL1, WL2 and WL3) simultaneously; this results in a current (denoted by I_{NF}) passing through T_1. Let the voltage generated across T_1 due to I_{NF} be denoted by V_{NF}. If the resistance of each of the memristors is $R_{offstate}$ and the voltage of the read pulse is V_{read}, then,

$$I_{NF}=3\ V_{read}/\ R_{offstate} \quad (1)$$

$$V_{NF}=I_{NF}\ \ R_{ds} \quad (2)$$

where R_{ds} is the drain-source resistance of T_1. So, V_{NF} and I_{NF} depend on the memristors connected along a column. The current through the load T_1 can be compared (using a current comparator) with the current generated by a reference voltage source; the reference voltage is equal to the correct (fault free) value, i.e. V_{NF}. The output of the current comparator produces a digital output, i.e. this output is low when the memristors operate correctly. This output remains high once deterioration causes at least one memristor to show a faulty behavior in its resistance.

Consider the scenario in which memristor M2 is in the R_{ON} resistance state (instead of R_{OFF}). A write 0 operation to all memristors is required for testing; this has no effect on M2 due to its erroneous state. By applying a read pulse, the current through T_1 is greater than I_{NF}; the newly measured current is given by:

$$I_{MEAS}=2V_{read}\ /R_{offstate}+V_{read}/R_{onstate} \quad (3)$$

where $R_{onstate}$ is the resistance of M2. Thus, the current through T_1 is greater than the reference current generated by V_{NF} and hence, the comparator output is high, indicating the presence of a memristor in the column whose deterioration has resulted in an erroneous resistance. Consider next as an example the detection of faults in a 3x3 LUT (Fig. 3). For LUT test, the inputs of all memristors in a row are connected together by using a controller circuit, thus for testing purposes all memristors in a row are driven by a single pulse. The load current across each column is compared sequentially with the current generated by the reference voltage; the column that

has at least a memristor with an erroneous resistance, is then determined depending on the output pattern of the comparator.

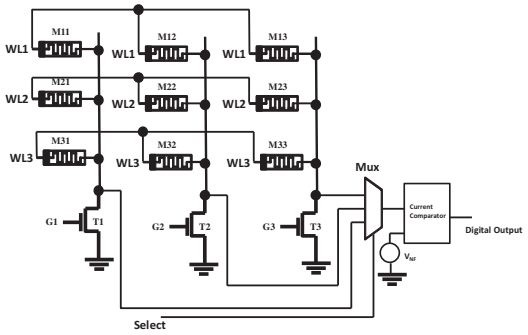

Fig. 3. Fault detection in a 3x3 LUT.

Following a write 0 operation and the simultaneous application of the read pulse to all rows, the current through each load (T1 or T2 or T3) is given by I_{NF} (and the output pattern of the comparator is "000") when all memristors are fault free (i.e. with correct resistance). Assume next that for example M11, M21 and M13 are faulty; then following the write 0 operation on all memristors, the resistances of M11, M21 and M13 remain at R_{ON}, thus causing more current to flow through the first and third columns. This yields a higher load voltage across T1 and T3, thus the output pattern of the comparator is "101", indicating the presence of faults in the memristors located in the first and third columns. Hence, the proposed test technique takes advantage of the homogeneous nature of the LUT and makes possible to detect faulty memristors by measuring the quiescent current.

III. Single Memristor Deterioration

B To better illustrate the proposed test process, this section presents the scenario in which only a memristor in the LUT has deteriorated; this assumption is made only for a better understanding of the test process and will be removed in subsequent sections of this manuscript. The parameters of the memristors (R_{OFF}, R_{ON} and its length D) are changed to study their effect on the performance of the LUT. The default values of a memristor in the LUT are given by R_{OFF}=19kΩ, R_{ON}=100Ω, and D=10nm [6]; the modified memristor model of [10] is used for the simulation; the default values are assumed unless otherwise specified.

A. Quiescent Current

Two cases are initially considered for the evaluation of the measured test current I_{MEAS}. Fig. 4(a) shows the value of the measured test current I_{MEAS} (equal to I_{NF}) versus deterioration (in %) of the R_{OFF} resistance in a memristor for different LUT dimensions, i.e. at 0% deterioration, R_{OFF}=19kΩ. As described previously, the measured current through the load (i.e. T) increases as the % deterioration increases. Once a memristor value deteriorates to $R_{ON,}$ then the comparator changes its state from 0 to 1 indicating the presence of a fault in the LUT. The difference between the measured and the reference currents (shown in Fig. 4(b)) increases as the deterioration increases, so this makes possible to detect the erroneous behavior of a single memristor as storage element in the LUT.

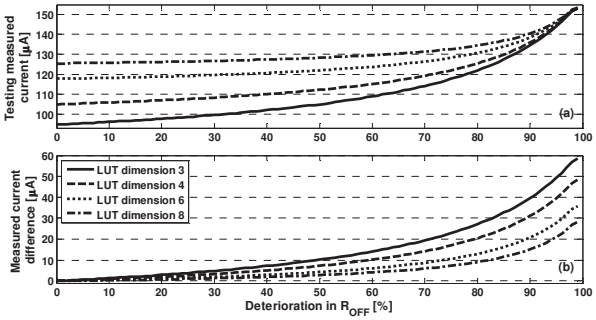

Fig. 4 Current vs. deterioration of the R_{OFF} resistance of the default memristor for different LUT dimensions; (a) Measured test current, and (b) Change (%) in measured current with respect to a memristor with no deterioration.

B. Least Detectable Deterioration (LDD)

The deterioration in the resistance of a memristor is detected using a current comparator; in this paper, the current comparator of [11] is utilized. This comparator is capable to measure an input current difference of 1μA with a response time of 0.2ns[11]; the performance of this current comparator allows for the response time of the LUT to reach a steady state and the measured current to settle. Fig.5 shows the result of changing R_{OFF} of the upper memristor (from 6kΩ to 258Ω in steps of 580Ω) for a LUT of dimension 3 with the memristor of [3]; a steady state is reached at 10ps (so 5% of the 0.2ns delay time of the current comparator).

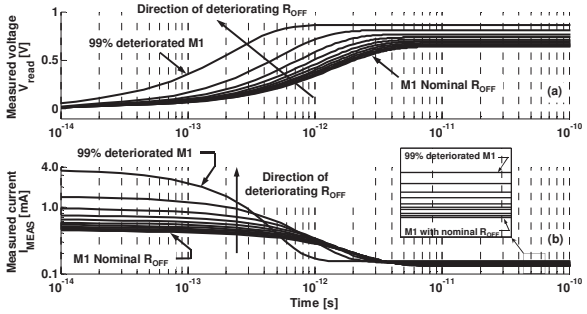

Fig. 5 Testing results for a LUT of dimension 3 using the memristor of Fig.1 and changing R_{OFF} of the upper cell from 6kΩ to 258Ω in 11 steps; (a) Testing measured voltage, and (b) Testing measured current.

Table 2 LDD of [3] and default memristor of this paper using the current comparator of [12].

LUT dimension	LDD [%]		R_{OFF} at LDD [kΩ]		Offset in current [μA]	
	[3]	Default memristor	[3]	Default memristor	[3]	Default memristor
3	14	9	5.16	17.29	1.047	1.052
4	20	12	4.80	16.72	1.013	1.022
6	34	19	3.96	15.39	1.027	1.029
8	47	26	3.18	14.06	1.026	1.010

The least value of deterioration (as the closest percentage integer value) that can be detected by the current comparator in a LUT made of memristors (the memristor of [3] is used as

default device in this paper), is shown in Table 2; this is referred to as the *Least Detectable Deterioration* (LDD). LDD effectively is the extreme value for detecting the gradual deterioration of the memristors in a LUT. The measured current for detection is given by the sum of the current in the fault free case (I_{NF}) and the difference current threshold (I_{DTH}) that determines LDD by the current comparator, i.e.

$$\text{Fault exists iff} \quad I_{MEAS} \geq I_{NF} + I_{DTH} \tag{4}$$

Additional simulation results (not reported here due to lack of space) show that R_{ON} and D have no significant effect on the testing process; this is due to the small sampling time (0.2ns), so unable to change the R_{OFF} state of the memristor.

C. Memristor Range

Data from previous presented simulation suggests a strong relation with R_{OFF} in the testing process; this is also related to the resistance range and the high to low state resistance ratio. So, an evaluation is pursued next; R_{OFF} is varied from 6kΩ to 384kΩ (while keeping R_{ON} at the constant default value), i.e. these values reflect an increase in the high to low state resistance ratio from 30 to 1920. The results are plotted in Fig.6; the value of R_{OFF} significantly affects LDD, however LDD is not significantly affected by the resistance ratio.

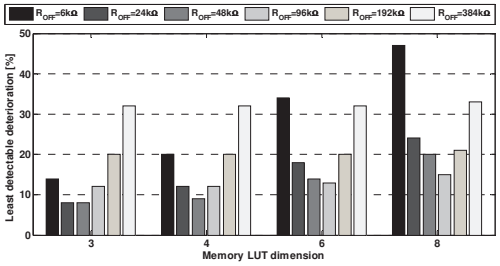

Fig. 6 LDD for various R_{OFF} and fixed R_{ON}=200Ω and D=29nm.

Fig.6 show two trends: 1. LDD decreases as R_{OFF} increases from 6kΩ to 96kΩ, but it increases with an increase in LUT dimension; 2. LDD increases as R_{OFF} increases, but it remains almost constant when the LUT dimension is increased. When R_{OFF} increases, the contribution of each memristor to the total measured current in a column decreases. The model of Fig. 7 is used to further validate the trend of Fig. 6. R_{Mj} denotes the resistance of memristor M_j (j=1,2,...,n), R_T is the ON resistance of the column transistor, V_{CMN} is the output voltage at the common node to which all memristors are connected, i_{Mj} denotes the current through memristor M_j, and V_{WL} is the applied read pulse voltage. For simplicity but with no loss of correctness and generality, assume that the transistor ON resistance R_T is constant and does not change when R_{M1} varies due to the deterioration in the high resistance R_{OFF} of M1. If R_{M1} denotes the resistance of the deteriorating memristor, then

$$I_{MEAS} = i_{M1} + \sum_{j=2}^{n} i_{Mj} = i_{M1} + i_{rest} \tag{5}$$

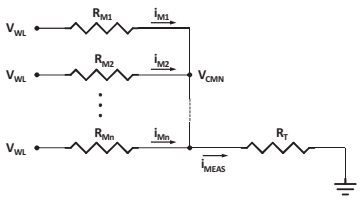

Fig. 7 Approximate equivalent circuit model of the detection circuit for a LUT of dimension n.

The applied voltage V_{WL} is constant and the current is reciprocal to resistance, so i_{rest} decreases as R_{OFF} increases. Therefore, at very large values of R_{OFF} (96kΩ to 384kΩ), the current that each branch contributes to I_{MEAS}, decreases and the only current affecting I_{MEAS} is the one that passes through the deteriorating memristor, i_{M1}. This effect also explains the small dependency on LUT dimension for the considered R_{OFF} values, i.e. when R_{OFF} has a large value, a substantial deterioration in R_{OFF} is needed to generate the required difference current threshold (I_{DTH}) to trigger the current comparator.

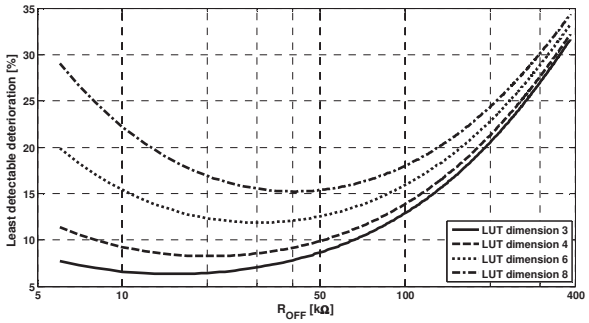

Fig. 8 LDD for the approximated equivalent circuit case for various LUT dimensions. The horizontal axis is logarithmic.

LDD is now plotted in Fig. 8 (with a logarithmic x-axis); this plot confirms the trend found in Fig. 6, thus confirming the validity of the proposed equivalent circuit model as well as the previous simulation results.

D. Monitoring

In addition to testing, the proposed method can be used to monitor the continuous deterioration of the memristors in a LUT. Digital-based testing provides only a Boolean outcome and notification occurs only once the deterioration of the memristors results in a faulty behavior (stuck-at fault in this case) and the LUT ceases to function correctly. Therefore, it is important to continuously gather information on the deterioration of the memristors in a LUT, such that an early notice of at least an incumbent fault can be provided and preventive measures can be undertaken. To continuously monitor the deterioration of the LUT, a Differential Current Amplifier (DCA) is connected to the load T using the proposed method (the DCA replaces the current comparator in Fig. 3). The DCA compares I_{NF} and I_{MEAS}, but its output (analog) value is an amplified value of the difference between I_{NF} and I_{MEAS},(as in Fig. 4(b)) and therefore, the deterioration can be monitored periodically for each column of the LUT.

E. Complexity

The testing process using the proposed method is also efficient in terms of complexity; the number of test (programming) phases required for detecting stuck-at faults in a nxn LUT using the proposed method is significantly less than the number of phases required by the method presented in [8]. The proposed method required only two phases (write 0 and write 1) to detect stuck-at-1 and -0 faults, so independent of array size (constant-testability); the method of [8] requires a number of phases that is linear with array dimension, i.e. n. This reduction in the number of phases comes however at the higher test time per phase as required in a current-based scheme versus the voltage-based approach of [8]; however, the constant number of phases required by the proposed scheme makes it attractive for application to integrated circuits with a homogeneous layout of LUTs such as FPGAs.

IV. Global Deterioration

A Next, a different scenario from the one dealt in the previous section is considered, namely all memristors experience deterioration. This scenario is referred to as *global deterioration* and reflects the more realistic case. The LUT is modeled as a resistive circuit and the current is measured under steady state conditions for the memristors. Consider the circuit of Fig. 3, this can be approximated by the equivalent circuit of Fig.7 by assuming n= 3 and one column of memristors. Using this equivalent circuit, the worst case in global deterioration is found to determine the suitability of the proposed current-based test method.

Let R_{M1} (Fig. 7) be the deterioration value of R_{OFF} and R_{M2} and R_{M3} vary within a bound (in this case ±10% [4]) of the designated default value of R_{OFF}. Detection occurs when I_{MEAS} is larger than a specified value (given by I_{NF} +I_{DTH}); under the global deterioration scenario, $I_{DTH\text{-}PRCT}$ must take a value greater than the largest additional current due to the deterioration of the memristors, therefore

$$I_{NF-PRCT} = \sum_{j=1}^{3} \max(i_{Mj-NF}) \quad (6)$$

where $i_{Mj\text{-}NF}$ is the current passing through memristor M_j in the fault-free case. Since the current is inversely proportional to resistance ($i_{Mj}=(V_{WL}-V_{CMN})/R_{Mj}$), the largest current occurs at the least resistance value, i.e. when R_{M2} and R_{M3} take values of 90% of R_{OFF}; so, (8) includes the largest fault-free currents of all memristors to account for the deterioration of M1 (as the memristor under test).

Simulation is then pursued with all memristors (except the one under test) having a 90% R_{OFF} value (as result of deterioration). The results are depicted in Fig.9. The percentage deterioration in R_{OFF} is plotted in the x-axis while the y-axis plots the test measured current difference, i.e. $I_{NF\text{-}PRCT}$ is now the value of the current at 10% deterioration (so no longer a value of 0%, as assumed previously). The current when the 10% deterioration occurs, is critical to the memristor test process. Fig.9 shows that the difference in measured current increases as the percentage deterioration in R_{OFF} increases. Also, as expected, LUTs with lower dimension have higher difference in measured current. With an increase in deterioration, the difference in the measured current of a LUT compared to the ideal (no-deterioration) case increases, thus yielding a very effective detection criterion. The measured current reaches a steady state at around 10ps irrespective of the R_{OFF} value of the memristor and hence, it is possible to test the LUT with a 10ps test time (provided a current comparator with a delay less than 10ps is also utilized, as in the case of this paper).

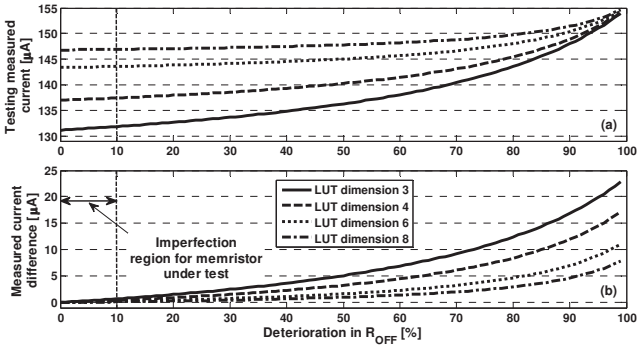

Fig. 9 Current vs. deterioration of the R_{OFF} resistance of the memristor used in Fig.2 for different LUT dimensions; (a) Testing measured current, and (b) Change (%) in measured current with respect to a memristor with no deterioration

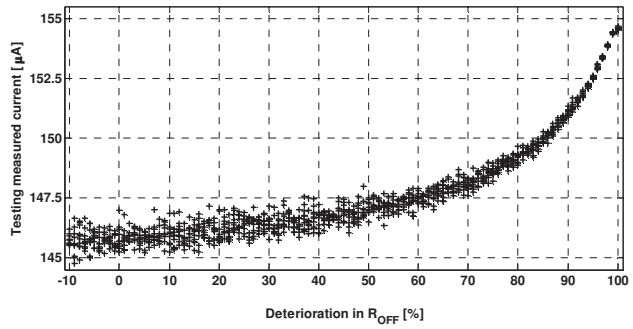

Fig. 10 Current vs. deterioration of the R_{OFF} resistance of the memristor under test (using a Gaussian distribution of deterioration variation for all memristors in a LUT of dimension 8)

Next, consider a LUT of dimension 8; the current is measured under deterioration of R_{OFF} for all memristors with a Gaussian distribution (the mean is equal to the nominal value (i.e. R_{OFF}=6kΩ) value and the standard deviation is 0.1). Each simulation is repeated randomly ten times (for the Gaussian distribution) at each level of deterioration (x-axis). Fig. 10 shows the result of the measured current; as expected, the mean value of the measured current occurs near the nominal value of R_{OFF}. A Gaussian simulation cannot precisely establish the worst case scenarios unless the simulated sample size is very large, thus incurring in a considerable overhead in terms of computation and simulation time. Therefore, only boundary cases (i.e. so without simulating the intermediate cases) are assessed; three values are considered: the nominal, +10% off the nominal value, and -10% off the nominal value.

Fig.11 shows the results of measuring the quiescent current in a LUT of dimension 8 by considering only boundary cases (i.e. without simulating the intermediate cases) and R_{OFF}=6kΩ; three values are considered: the nominal, +10% off the nominal value, and -10% off the nominal value.

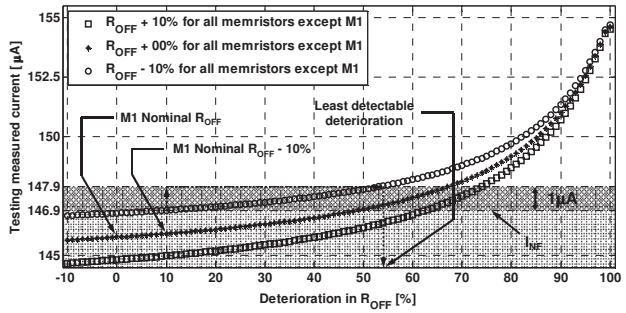

Fig. 11 Current vs. deterioration of the R_{OFF} resistance of the memristor under test (considering the worst case deterioration variation of ±10% in all memristors in a LUT of dimension 8).

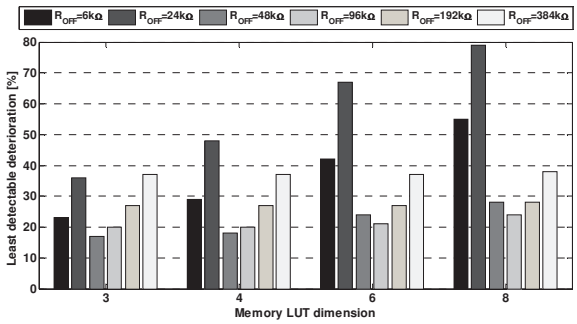

Fig. 12 Least detectable deterioration vs LUT dimension at various high state resistance values under worst case deterioration variation.

The ideal current has a value at 10% deterioration (plotted on the x-axis) of memristor M1, while all other memristors have a high resistance value at 90% of R_{OFF}; the measured current during test is plotted on the y-axis. This assessment is then repeated at different R_{OFF} values (6kΩ, 24kΩ, 48kΩ, 96kΩ, 192kΩ, and 384kΩ); the results are shown in Fig. 12. LDD (in %) is plotted versus the LUT dimension at different R_{OFF} values. Fig. 12 shows that LDD increases by increasing the dimension of the LUT, while R_{OFF} at a specific LDD value decreases; this feature shows that the proposed approach is scalable to LUTs of dimension larger than 8. Also, for a given R_{OFF} and transistor size, LDD increases as the dimension of the LUT increases (this is more evident at low R_{OFF} values). However as the value of R_{OFF} increases, the change in LDD initially decreases and then, it remains almost constant; this occurs due to the low current when using high R_{OFF} values. This is not significant with a change in transistor size and LUT dimension, thus further enforcing the scalable nature of the proposed approach.

V. Conclusion

This paper has proposed a testing scheme and model for the operational deterioration of a memristor-based LUT. A quiescent current technique has been utilized for diagnosing the LUT in the presence of variation of the resistances. A current comparator has been utilized for observing the output pattern; the conditions by which either deterioration, or variation of the resistances allow detection have been established. A simple equivalent circuit model has also been proposed for LTSPICE simulation. Extensive results have been presented with respect to different operational features, such as LUT dimension and range of resistance. The deterioration of the memristor against the measured current has been studied in detail; the results confirm that the proposed current-based scheme is scalable with LUT dimension and very effective in assessing the correct operation of a memristor-based LUT in the presence of deterioration.

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