

ACM SIGDA / EDAA PhD Forum at DATE 2015 in Grenoble

The ACM SIGDA / EDAA PhD forum is part of the DATE Conference and hosted by ACM SIGDA and the European Design Automation Association (EDAA). It offers the opportunity for PhD students to present their thesis work to a broad audience in the design, automation and test community from academia and industry. During the presentation at the DATE Conference, it helps students to establish contacts. Also, representatives from industry and academia get a glance of state-of-the-art research in design, automation and test. The review process resulted in the selection of the PhD students listed below. We thank ACM SIGDA, EDAA, and DATE for making this Forum possible.

Rolf Drechsler, University of Bremen/DFKI GmbH, DE (Chair, ACM SIGDA / EDAA PhD Forum 2015)

PhD Forum Committee

Walter Anheier, University of Bremen, DE
Laleh Behjat, University of Calgary, CA
Davide Bertozzi, Università degli studi di Ferrara, IT
Anupam Chattopadhyay, Nanyang Technological University, SG
Giorgio Di Natale, LIRMM, FR
Helmut Graeb, TU München, DE
Shiyan Hu, Michigan Technological University, US
Younghyun Kim, Purdue University, US
Xin Li, Carnegie Mellon University, US
Gi-Joon Nam, IBM, US
Sander Stuijk, Eindhoven University of Technology, NL
Daniel Tille, Infineon, DE
Miroslav N. Velev, Aries Design Automation, US
Natarajan Viswanathan, IBM, US
Robert Wille, University of Bremen/DFKI GmbH, DE

Admitted Presentations

- 1. Selective Transistor-Redundancy Based Fault Tolerance Technique for Combinational Circuits**
Ahmad Sheikh, King Fahd University of Petroleum & Minerals, SA
- 2. Definition of Methods and Tools for an Effective Smart Buildings Deployment**
Alessandro Antonio Nacci, Politecnico di Milano, IT
- 3. Design Methods for Reliable Quantum Circuits**
Alexandru Paler, University of Passau, DE
- 4. Energy Efficient Cache Memories in Deeply-Scaled Technologies**
Alireza Shafaei Bejestan, University of Southern California, US
- 5. Hybrid Wire and Surface-wave Communication Fabrics for Future NoC-based Chip Multiprocessors**
Ammar Karkar, School of Electrical and Electronic Engineering, Newcastle University, Newcastle upon Tyne, GB
- 6. High-level Constructive Synthesis of Domain-Specific Kernels of Cryptography**
Ayesha Khaild, RWTH Aachen, DE
- 7. Safety-Assured Model-Based Implementation of the GPCA Infusion Pump Software**
BaekGyu Kim, University of Pennsylvania, US
- 8. Improved Test Techniques for Network-on-Chip Based Memory Systems**
Bibhas Ghoshal, IIT, Kharagpur, IN
- 9. Dedicated Hardware Accelerators for High Efficiency Video Coding Standard**
Cláudio Diniz, UFRGS, BR
- 10. Heat Dissipation and Thermal Analysis for 3D ICs**
Cristiano Santos, PGMICRO-UFRGS / CEA-Leti, BR
- 11. Fault Tolerance for Real-Time Systems: Analysis and Optimization of Roll-back Recovery with Checkpointing**
Dimitar Nikolov, Lund University, Department of Electrical and Information Technology, SE
- 12. SyntHorus2: A Tool for Assertion-based Synthesis**
Fatemeh JAVAHERI, TIMA Lab, FR

- 13. Multilevel Modeling, Formal Analysis, and Characterization of Soft Errors in Digital Systems**
Ghaith Bany Hamad, Polytechnique Montréal, CA
- 14. RHetOS: A Reconfigurable and Heterogeneous Operating System**
Gianluca Durelli, Politecnico di Milano, IT
- 15. Path-Based Program Repair**
Heinz Riener, University of Bremen, DE
- 16. Theory and applications of quantum process calculus**
Ittoop Puthoor, University of Glasgow, GB
- 17. Non-Invasive Extraction of SystemC Meta Data**
Jannis Stoppe, DFKI GmbH, DE
- 18. Synthesis and Optimization of Reversible Logic Circuits**
Kamalika Datta, National Institute of Technology, Meghalaya, IN
- 19. Optical Interconnects for Computing Systems: a Formal Study on Signal-to-Noise Ratio**
Mahdi Nikdast, Polytechnique Montréal, CA
- 20. NoC-Centric Partitioning and Reconfiguration Technologies for the Efficient Sharing of Many-Core Platforms**
Marco Balboni, University of Ferrara, IT
- 21. Post-Manufacturing One-Shot Calibration of RF Circuits Based on Non-Intrusive Sensors**
Martin Andraud, TIMA Laboratory, FR
- 22. Range Based Analysis of Inner Systems Characteristics**
Michael Rathmair, Institute of Computer Technology, Vienna University of Technology, AT
- 23. Making Homogeneous the Platform-Based Design of Heterogeneous Cyber-Physical Systems**
Michele Lora, University of Verona, IT
- 24. Power Aware Test and Test of Low Power Devices**
Miroslav Valka, Post-Doc, FR
- 25. Run-Time Resource Management of Networked Many-Core Systems**
Mohammad Fattah, University of Turku, FI
- 26. Thermal Management Using Thermoelectric Coolers**
Mohammad Javad Dousti, University of Southern California, US
- 27. Yield and Cost Analysis for 3D Stacked ICs**
Mottaqiallah Taouil, Delft University of Technology, NL
- 28. Hardware-Software Co-Design for Next Generation Dark Silicon Multimedia Systems**
Muhammad Usman Karim Khan, Karlsruhe Institute of Technology (KIT), DE
- 29. Design Space Exploration of Thread vs. Arithmetic Level Parallelism to Design a Computation Unit of the Multi-chip eBrain Supercomputer**
Nasim Farahini, KTH, SE
- 30. Towards High Performance and Efficiency of Heterogeneous Systems**
Sam Skalicky, Rochester Institute of Technology, US
- 31. Power: Its Manifestations in Digital Systems Testing**
Seetal Potluri, Indian Institute of Technology Madras, IN
- 32. Managing the Complexity in Embedded and Cyber-Physical System Design - System Modeling and Design-Space Exploration**
Seyed-Hosein Attarzadeh-Niaki, KTH Royal Institute of Technology, SE
- 33. Logic Rewiring: a Practical Bridging Technique between VLSI Logical and Physical Syntheses**
Xing Wei, Chinese University of Hong Kong, HK
- 34. Distributed Thermal Management for Large-Scale Chip-Multiprocessors**
Yingnan Cui, Nanyang Technological University, SG
- 35. High-level Modeling, Estimation and Exploration of Reliability for MPSoC**
Zheng Wang, RWTH-Aachen University, DE
- 36. Modeling, Analysis and Exploration of Layers: A 3D Computing Architecture**
Zoltán Endre Rákossy, Institute for Communication Technologies and Embedded Systems (ICE), RWTH Aachen, DE