Testing for SoCs with Advanced Static and Dynamic Power-Management Capabilities*

Xrysovalantis Kavousianos[1,2]
[1]Department. of Computer Science
University of Ioannina, Greece

Krishnendu Chakrabarty[2]
[2]Department of Electrical and Conputer Engineering
Duke University, USA

***Abstract*—Many multicore chips today employ advanced power management techniques. Multi-threshold CMOS (MTCMOS) is very effective for reducing standby leakage power. Dynamic voltage scaling and voltage islands which operate at multiple power-supply voltage levels, minimize dynamic power consumption. Effective defect screening for such chips requires advanced test techniques that target defects in the embedded cores and the power management structures. We describe recent advances in test generation and test scheduling techniques for SoCs that support power switches, voltage islands, and dynamic voltage scaling schemes.**

***Index Terms*—Dynamic power, dynamic voltage scaling, power switches, SoC test scheduling, static power.**

I. Introduction

As chip density increases relentlessly along Moore's law, power consumption is emerging as a major burden for contemporary systems. Dynamic power has been effectively attacked by decreasing the power supply voltage level, while at the same time, the degradation in circuit performance has been avoided by reducing the transistor threshold voltage (V_t). However, as the transistor threshold voltage (V_t) decreases, the sub-threshold leakage current increases exponentially. In sub-90 nm technologies, leakage (static) power has become a significant portion of total power consumption.

The adverse effects on system performance set a lower limit on the power supply voltage that can be used during normal operation. Further reduction in the power supply voltage can be achieved by exploiting performance slack during SoC operation. *Dynamic Voltage Scaling (DVS)* is a widely adopted technique that reduces the power supply-voltage level during periods of relatively light workload; therefore it reduces dynamic power consumption without affecting performance. DVS is usually combined with the partitioning of the system into voltage islands, which are logic and/or memory regions with separate supply rails and unique power characteristics [25], [30]. By adapting DVS to the specific requirements of each voltage island, performance objectives can be met while dynamic power savings are maximized [26]. Dynamic voltage scaling has been implemented in several state-of-the-art processors [1], [2], [3], [4].

DVS is very effective but it can only reduce dynamic power during periods of system activity. Further power reductions can be achieved by reducing static power during idle periods of operation. Many techniques have been presented in the literature for reducing leakage current, e.g., digital logic synthesis using dual-V_t libraries [13], and input vector control [5], [7], [27]. A very effective technique is the use of high-V_t power switches between the circuit and the power supply or the ground rail [8], [9], [13], [16], [28], which are turned off during long periods of inactivity, thereby suppressing leakage current. There are also techniques that offer one or more intermediate power-off modes to reduce static power in short periods of inactivity too [11], [23], [31], [33].

Even though the design of SoCs that support DVS and multiple intermediate power-off modes has been comprehensively addressed in the literature, testing of such systems has received relatively less attention. Advanced test techniques are required for effective defect screening for these chips, including their power management strucures. In this paper, we describe recent advances in test scheduling for DVS-based SoCs that support voltage islands, as well as test generation, diagnosis and repair mechanisms for SoCs that support multiple power-off modes.

The organization of this paper is as follows: Section II presents recent techniques for modeling the test scheduling problem for DVS-based SoCs. Section III presents a time-division-multiplexing scheme for DVS-based SoCs. Section IV presents recent advances in designing and testing of power-off management structures. Finally, Section V concludes the paper.

II. Test Scheduling for DVS-Based SoCs

Fault-free behavior of SoCs that support DVS must be ensured at each voltage/frequency setting because defects are manifested in different ways at various voltage levels. For example, it was shown in [6], [20], [21] that certain resistive bridging faults can be detected only at specific supply voltage levels. However, testing at different voltage levels increases the test time because test patterns have to be applied at multiple power supply-voltage levels. In addition, the scan clock frequency is reduced at low voltage levels while the switching between different voltage levels and the need to carry out state-retention tests incur additional test costs.

*This research has been co-financed by the European Union (European Social Fund – ESF) and Greek national funds through the Operational Program "Education and Lifelong Learning" of the National Strategic Reference Framework (NSRF) - Research Funding Program: Thales. Investing in knowledge society through the European Social Fund.

978-3-9815370-0-0/DATE13/©2013 EDAA

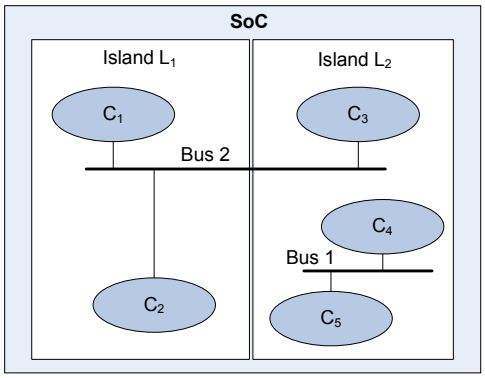

Fig. 1. An example SoC with multiple voltage islands.

As shown in [18], test scheduling for multi-V_{dd} SoCs with multiple voltage islands, is considerably more challenging than traditional test scheduling for single-V_{dd} designs. At first, testing at multiple voltage levels increases considerably the test time and the complexity of the test scheduling problem. Second, similar to the case of testing single-V_{dd} SoCs, the scheduling of tests for multi-V_{dd} SoCs must satisfy all the constraints imposed by the sharing of test resources among different cores, as well as additional constraints that include: (a) Test Access Mechanisms (TAMs) that span different voltage islands, (b) cores that share the same power network whenever they belong to the same island and (c) state retention tests that need to preceed any other test whenever the voltage switches between different levels.

The first approach to formulate the above optimization problem was presented in [17], [18]. In this formulation it was assumed that every island is tested at all or a subset of power supply voltage levels of the chip and all cores in a voltage island are tested at all or a subset of the power supply-voltage levels of that island. Furthermore it was assumed that every island (and every core in that island) must be tested for correct transition between voltage levels using state retention tests. Testing at each power supply-voltage level precludes the use of a scan frequency that is higher than the maximum scan frequency that can be used at that voltage level (high scan frequencies can only be used at high voltage levels).

Another assumption in [18] is that TAM resources in a multi-core SoC can be shared between different cores and may span different islands. In that case, the otherwise independent tests of these islands becomes dependent, and thus additional constraints arise in test scheduling. In addition, the constraint of setting each island at one voltage level at a time imposes the requirement to apply certain tests that correspond to different voltage levels during non-overlapping time periods. The following example sheds light into the optimization problem.

Example 1. Fig. 1 shows an SoC consisting of five cores C_1, C_2, ..., C_5, which belong to two voltage islands, L_1 and L_2. There are three voltage levels for the entire SoC: V_1, V_2, and V_3. The TAM resources in this SoC consist of two buses *Bus1, Bus2* which are shared among the five cores. Every core has to be tested at all three voltage levels. Therefore, there is one task associated with each core-voltage level pair and in total there are 15 (5×3) different tasks for this SoC. In addition, the transition between voltage levels is tested for every core using appropriate state retention tests. Note that the sharing of *Bus2* between cores C_1, C_2 and C_3 prohibits independent and parallel execution of the tasks for L_1 and L_2. In addition, even though core C_3 does not share resources with cores C_4, C_5 various constraints arise due to the common island that they reside to. For example, the test of C_3 at V_1 cannot be executed concurrently with the test of C_4 at V_2, V_3 or the test of C_5 at V_2, V_3 due to the requirement that each island can operate at a single voltage level at a time. ■

It is obvious that additional restrictions (besides the trivial ones that arise from the sharing of resources) are imposed on the testing of multi-V_{dd} SoC. For solving this optimization problem, an ILP model was proposed in [18]. This model is based on the concept of test sessions, which are voltage-specific non-overlapping test periods for each island. Each test session is associated with one island and one voltage level, and every task that uses any particular voltage level for any core in the island is scheduled during the respective test session that is associated with that voltage level. Test sessions of different islands that do not share resources are independent. Therefore, at each time instance, as many test sessions as the number of different islands can be scheduled in parallel provided that they do not share TAM resources. To minimize the overall time overhead due to the switching between different voltage level, and yet thoroughly test all cores at every voltage level, the minimum number of test sessions are applied, that is equal to the number of voltage levels. Moreover, the supply voltage was assumed to change between adjacent levels in the set of available voltages, resembling the adaptive operation of SoCs, where the voltage levels change successively from higher levels to the lower levels, and vice versa.

The ILP model proposed in [18] includes two main constraints. The first constraint is a set of relations that ensures that every task must be applied during the session that sets the island to the same voltage level that the task is using. Additionally, it ensures that state-retention tests preceed any other core test. The second constraint is a set of relations that ensure that any two tasks for any two cores that share a resource never overlap when: (a) the cores belong to different voltage islands or (b) the cores belong to the same voltage island and they use the same voltage level. The complexity of this model in terms of number of constraint is upper bounded by $O(N^2 \times n^2)$.

The authors in [18] proposed also two LP-relaxation heuristics, namely recursive rounding and randomized rounding, as well as a greedy heuristic that performs very well as compared to the ILP method. The greedy approach schedules the tasks in a priority-based manner that aims to minimize the test time of the most heavily-loaded test resources i.e., the resources that constitute the bottleneck in the testing of the SoC. Specifically, the test-scheduling algorithm first schedules all the tasks of the first session of each island, then it schedules all tasks of the second session of each island, and so on, until all tasks of all

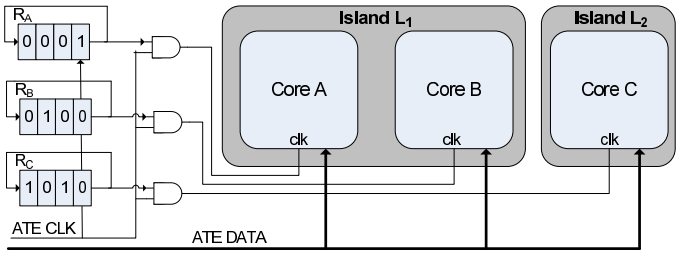

Fig. 2. Proposed TDM scheme.

sessions are scheduled. During the scheduling of each session it selects one task corresponding to the TAM resource with the latest expected time to finish delivering all test data to its attached cores, and it schedules this task as early as possible. When multiple cores at different islands are connected to that TAM resource the algorithm selects a core on the island that the next session can begin sooner than the others. Experimental results on two industrial SoCs, show that both the ILP and the greedy approaches provide significantly lower test time as compared to traditional test scheduling approaches.

III. Time Division Multiplexing for Multicore SoCs

The testing time for both single-V_{dd} and multi-V_{dd} SoCs is dominated by the process of serially loading test data into the cores through scan chains, which is usually very slow. In multi-V_{dd} SoCs however, this problem is exacerbated when cores are tested at the low power-supply voltages, where the maximum allowable scan frequency is very low. In addition, testers usually conduct SoC testing using a single scan frequency over the duration of the test period. Thus, to avoid scan violations at any voltage setting, the lowest frequency for shifting test data that corresponds to the lowest voltage level is used, and the test time of the SoC increases even more.

To overcome the above limitation, a time-division multiplexing (TDM) approach was proposed in [19]. By using TDM, the test data are transmitted by the tester at a high frequency, while at the same time, they are shifted into the scan chains of multiple cores at those frequencies that are permited by the voltage setting used. The TDM approach exploits the gap between the shift frequency of the ATE and the cores as well as the gap between the shift frequencies of different cores at different islands which are concurrently tested at different voltage settings. A very interesting observation reported in [19] was that, counter-intuitively and in contrast to what is expected, shifting test data into the scan chains at lower than the nominal frequencies may be beneficial in terms of ATE-channel-frequency utilization when TDM is available and this strategy may reduce the overall SoC test time.

A TDM scheme and an ILP-based test scheduling approach was proposed in [19]. Fig. 2 presents the proposed TDM scheme for an SoC consisting of cores A, B, C, and a test bus shared between them. Cores A, B belong to island L_1 and core C belongs to L_2. Both islands support voltage settings V_1, V_2, V_3 and the nominal scan frequencies at each voltage setting are $F, F/2$ and $F/4$, respectively. ATE_CLK is the clock signal generated from the ATE and it has frequency F for loading the scan chains (the same frequency is used for loading the test data on the bus). Each core is assigned one cyclical shift register with length equal to 4, which divides the scan frequency by a value equal to 1, 2 or 4. Every shift register is clocked with the fast ATE_CLK (frequency F) and in turn provides a clock signal with frequency equal or smaller to F. The following example illustrates this method.

Example 2. Let us assume that at a specific time instance, cores A and B are tested at voltage V_3 and C is tested at voltage V_2. The highest frequencies that can be used for A, B, C at those voltage levels are $F/4, F/4, F/2$, respectively. In order to provide scan frequency of $F/4$ to core A, register R_A in Fig. 2 is loaded with the pattern "0001". Then, during every 4 successive cycles of ATE_CLK, the rightmost cell of R_A receives the value '1' only once and permits the application of one out of the four active edges of signal ATE_CLK to the core A. In this case the scan clock frequency for this core is equal to $F(ATE\_CLK)/4 = F/4$. Register R_B is loaded with the pattern "0100", which sets the scan frequency of core B equal to $F/4$ too. Register R_C is initialized with pattern "1010" and thus core C sees one active clock edge every two ATE_CLK cycles. Therefore, the scan clock frequency for core C is set to $F/2$. The patterns loaded into R_A, R_B, R_C have non-overlapping '1' logic values to ensure that test data are delivered at the appropriate core at the right time. ■

An ILP model was also proposed for the above TDM scheme that is based on the assumption that N_F frequencies are supported by the TDM scheme and that testing a core at a particular voltage setting involves different completion time for each one of them. This is due to the fact that every shift frequency cannot be supported at every voltage setting as the high frequencies can be only supported at the high voltage settings to avoid timing violations in scan chains. Four constraints comprise the ILP model. The first constraint ensures that any test for a core at any voltage setting is applied using a single scan frequency that is equal or lower than the maximum shift frequency at the respective voltage level. The second constraint ensures that any two cores in the same island cannot be concurrently tested at different voltage settings due to the sharing of common power network. The third constraint determines the concurrency between different tests and the final constraint bounds the number and type of tests that can concurrently use the same TAM resource. Results show that the method proposed in [19] outperforms the approach proposed in [18] by offering further test time reduction, as high as 86.1% as compared to [18].

IV. Power Switches

Even though DVS is very effective for reducing dynamic power during normal operation, it cannot reduce static power. Static power can be completely eliminated during idle periods by putting the cores into sleep using power switches. Power switches are large transistors that connect the core to the power supply and/or ground rail. They are turned off during

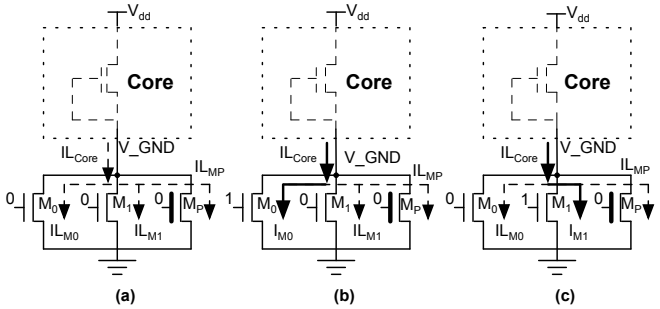

Fig. 3. Multimodal Power Gating Scheme

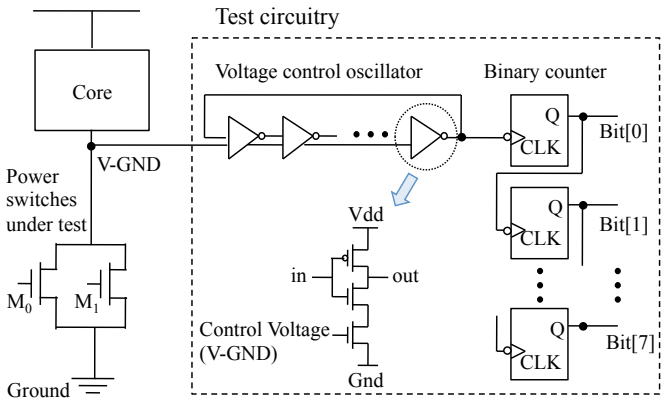

Fig. 4. Proposed test circuitry for the multi-mode power gating architecture.

idle mode, thereby suppressing leakage current, and they are turned-on again to re-activate the core.

A major problem of using power switches is the long time required for recovering from the idle mode, referred to as the wake-up time, which prohibits the use of power switches during short periods of inactivity. A very effective technique to reduce wake-up time is to use an intermediate power-off mode [11], [14], [15], [23], [24], [29] that comes at the expense of a small increase of leakage power dissipation. The authors of [31] extended this capability into a trade-off between wake-up overhead and leakage power savings by offering two power-off modes. Depending on the length of the period of inactivity, a different power-off mode can be used and the static power savings are maximized (the longer this period is, the more deeply the core can be put into sleep). In [33], [34] a reconfigurable power gating scheme was presented that offers more than two intermediate power-off modes and that is also tolerant to process variations enabling thus the utilization of the proposed architecture for newer and less mature technologies.

Fig. 3 presents the design proposed in [34]. It consists of the main power switch transistor M_P that is used to activate or put the core into the complete power-off mode, and two small transistors M_0 and M_1, each corresponding to an intermediate power-off mode (M_0 corresponds to the dream mode and M_1 corresponds to the sleep mode). Transistor M_P is a high-V_t transistor and it remains on only during the active mode. Transistors M_0 and M_1 are small low-V_t transistors that are turned on only during the corresponding power-off mode.

This scheme operates as follows. In snore mode, all transistors M_P, M_0 and M_1 are off as shown in Fig. 3(a) and the voltage at the $V-GND$ node increases to a level close to V_{DD}. In dream mode, only M_0 is on as shown in Fig. 3(b). In this mode, the current flowing through transistor M_0 sets the virtual ground node at a voltage level that is lower than V_{DD} and higher than 0. In dream mode, the static power consumed by the core is higher compared to the snore mode, but the wake-up time is less. In sleep mode, only M_1 is turned-on; see Fig. 3(c). Transistor M_1 has larger aspect ratio than M_0 and thus the aggregate current flowing through the $V-GND$ node increases even more in this case. Consequently, the voltage level at the virtual ground node is further reduced compared to the dream mode and the wake-up time decreases at the expense of increased power consumption.

A. Testing of Power Switches

Even though power switches offer significant benefits in reducing static power, their adoption in practice depends on the availability of test and diagnosis methods that can guarantee their correct operation in the field. In prior work, test methods have been presented for power switches that support complete power-off mode [12], [22], [32]. In [10], [35], a test scheme and a signature analysis method for the testing and diagnosis of power switches with multiple intermediate power-off modes was presented. The test scheme is shown in Fig. 4 and it consists of a voltage control oscillator (VCO) and a counter. The VCO consists of current-starved inverters, with $V-GND$ as control signal, and it converts the voltage at $V-GND$ into a signal toggling with a frequency that depends on this voltage. The VCO output triggers a binary counter that provides a quantification of the frequency, the signature, which is directly proportional to the voltage at $V-GND$ and depends on the power-off mode applied.

As shown in [35], the power switches are defect-free if the voltage at $V-GND$ lies between an upper bound and a lower bound. These bounds correspond to digital signature ranges which are calculated using simulation. However, excess process variations affect the operation of VCO and shift the signature out of the nominal range of acceptable signature values even when the power switches are defect-free. In order to reduce the effects of process variations, a calibration strategy was adopted in [35] to adjust the die signatures in such a way as to remove the process variation effects as much as possible. The signature ranges calculated using calibration are refered to as Test-AARs (Test Adjusted Acceptable Ranges) and they are different for each power-off mode.

B. On-Line BIST/BISR Scheme

In [36], a BIST/BISR scheme was proposed for testing and repairing multi-mode power switches in the field, which completely eliminates the need for external ATEs. It computes the signature for every power-off mode and confirm if the

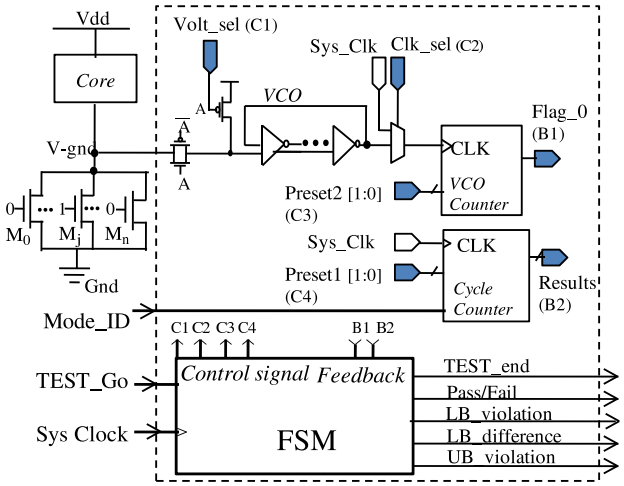

Fig. 5. BIST unit for testing power switches

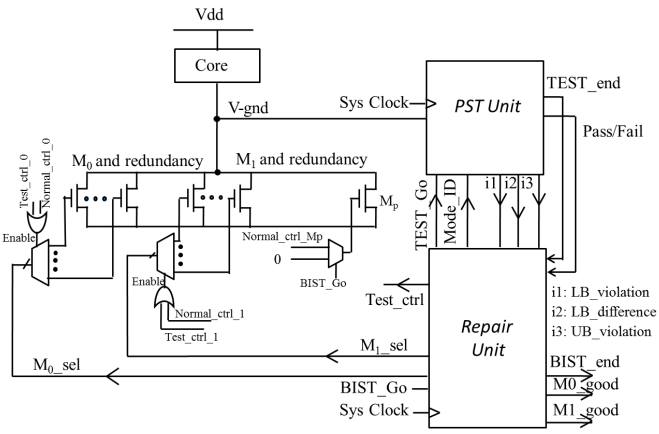

Fig. 6. The complete BIST scheme with built-in self-repair.

signature lies into the respective Test-AAR or not. The block diagram is shown in Fig. 5. This scheme requires the trigger signal TEST_Go to start testing power switch M_j as well as the signal Mode_ID, which indicates the power-off mode that corresponds to M_j. It generates the signal Test_end to indicate when the test ends as well as the signal Pass/Fail to indicate whether the switch under test is good or not. When the power switch fails the test, signals LP_violation, LP_difference and UB_violation are also generated to provide the exact cause of the failure offering thus diagnosis capabilities. LB_violation is asserted when the signature violates the lower bound and LB_difference is equal to the difference of the signature from the lower bound. UB_violation is asserted when the signature violates the upper bound.

The BIST circuitry presented in Fig. 5 consists of four main modules: VCO, VCO Counter, Cycle Counter, and FSM (finite state machine). The Cycle Counter is used to control the test periods that VCO counter counts up or down. The FSM is used to synchronize the operation of all units during BIST and to carry out the test operations for each power switch. VCO counter is initialized to a golden reference value, which can be computed via simulation, is the same for all dies and therefore can be hardwired on chip. Then the VCO input is connected to V_{dd} and the VCO unit triggers the VCO counter which counts down for a predetermined number of clock cycles. At the end of this counting period the VCO counter holds a value that is representative of process variations affecting the die, and it is used later to generate signatures.

At the second step, the VCO input is connected to the virtual ground node and the power switch under test is turned-on to put the core into the respective power-off mode (power switch M_p is turned off). The VCO counter is again triggered by the VCO unit and it begins to count up now starting from its current value for the same number of clock cycles as before. During this period the VCO counter will be triggered a number of times that is equal to the signature value at this power-off mode. When this counting period ends, the VCO-counter value is equal to the adjusted signature of the power switch.

At the third step, the adjusted signature is compared to the lower bound of the Test-AAR. For this purpose, the VCO counter counts down for a number of cycles equal to the lower bound of the Test-AAR. Then, the VCO counter contains the difference of the adjusted signature and the lower bound of the Test-AAR. If during the VCO-count down the VCO counter reached the value 0 then the adjusted signature is lower than the lower bound and hence the power switch is defective. If the lower bound was not violated, the VCO counter continuous to count down again at the fourth step for a number of clock cycles equal to the difference between the upper and the lower bound. At the end of the counting period, the value stored in the VCO counter is equal to the difference between the adjusted signature and the upper bound. If during this period, the VCO counter reached zero at any point, the signature is smaller than the upper bound, thus the power switch is defect-free; else the upper bound is violated and the power switch has to be replaced with a spare one.

The complete BIST/BISR scheme is shown in Fig. 6. When the BIST_Go signal is asserted, the BISR unit selects the first power-off mode and it sets the Mode_ID signal accordingly. Then, it selects one of the power switches corresponding to this mode, it turns this switch on to put the core into the respective power-off mode, and it tests this power switch by asserting the TEST_Go signal of the BIST unit (note that the BIST_Go signal is used to turn-off the main power switch M_p during the whole testing period). When the test finishes (the signal TEST_end is asserted) the status of the signal Pass/Fail is checked to verify whether the power switch passed the test. If the power switch passed the test, it is selected as the power switch of the respective power-off mode and the rest of the power switches for the same power-off mode are not further exercised. If the power switch failed the test then the next available switch for the current power-off mode is selected and it is tested. When all power switches corresponding to a power-off mode are tested, the BISR unit continuous with the next batch of power switches for the next power-off mode. Results presented in [36] show that the BIST/BISR structure has very small hardware overhead while it effectively tests power switches at a very short time.

V. Conclusions

Advanced power management techniques employed by multicore chips necessitate the use of advanced test techniques to ensure defect-free operation in the field. In this paper, we presented recent advances in DVS-based test scheduling, as well as in testing of SoCs supporting multiple power-off modes. Results have shown that DVS-based test scheduling offers significant test time benefits, especially when a TDM-based approach is employed. In addition, we presented an effective test generation and diagnosis method for the testing of multi-modal power switches that can overcome manufacturing process variations. Finally, an on-line mechanism was presented that alleviates the need for a tester and repairs defects in the power switches in the field.

References

[1] ARM 1176JZ(F)-S documentation, http://www.arm.com/products/CPUs/ARM1176.html.

[2] Intel Corp, "Intel XScale Core Developer's Manual, 2003", http://developer.intel.com/design/intelxscale/.

[3] Transmeta Corporation. "Crusoe processor documentation 2002" http://www.transmeta.com.

[4] *Intel: PXA270 Processor Datasheet, Nov. 2007. [Online]. Available: http://www.phytec.com/pdf/datasheets/.*

[5] A. Abdollahi, F. Fallah, and M. Pedram, "Leakage Current Reduction in CMOS VLSI Circuits by Input Vector Control," *IEEE Transactions on VLSI Systems*, vol. 12, no. 2, pp. 140–154, Feb. 2004.

[6] N. B. Z. Ali, M. Zwolinski, B. M. Al-Hashimi, and P. Harrod, "Dynamic Voltage Scaling Aware Delay Fault Testing," in *11th IEEE European Test Symposium,*, May 2006, pp. 15–20.

[7] Y. Alkabani, T. Massey, F. Koushanfar, and M. Potkonjak, "Input Vector Control for Post-Silicon Leakage Current Minimization in the Presence of Manufacturing Variability," in *45th ACM/IEEE Design Automation Conference*, June 2008, pp. 606 –609.

[8] M. Anis, S. Areibi, and M. Elmasry, "Design and Optimization of Multithreshold CMOS (MTCMOS) Circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 22, no. 10, pp. 1324 – 1342, Oct. 2003.

[9] M. Anis and M. Elmasry, *Multi-Threshold CMOS Digital Circuits – Managing Leakage Power*. Kluwer Academic Publishers, 2003.

[10] K. Chakrabarty, X. Kavousianos, and Z. Zhang, "Power Switch Design and Method For Reducing Leakage Power In Low-Power Integrated Circuits," US Patent Application no. 12/882,776, filed by Semiconductor Research Corporation, Sept. 2010.

[11] M. Chowdhury, J. Gjanci, and P. Khaled, "Innovative Power Gating for Leakage Reduction," in *Proceedings of IEEE International Symposium on Circuits and Systems*, May 2008, pp. 1568 –1571.

[12] S. K. Goel, M. Meijer, and J. de Gyvez, "Testing and Diagnosis of Power Switches in SOCs," in *Proceedings of 11th IEEE European Test Symposium*, May 2006, pp. 6 pp. –150.

[13] S. Idgunji, "Case Study of a Low Power MTCMOS based ARM926 SoC: Design, Analysis and Test Challenges," in *Proceedings of IEEE International Test Conference*, Oct. 2007, pp. 1–10.

[14] H. Jiao and V. Kursun, "Ground-Bouncing-Noise-Aware Combinational MTCMOS Circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 8, pp. 2053 –2065, Aug. 2010.

[15] ——, "Ground Bouncing Noise Suppression Techniques for Data Preserving Sequential MTCMOS Circuits," *IEEE Transactions on Very Large Scale Integration Systems,*, vol. 19, no. 5, pp. 763 –773, May 2011.

[16] J. Kao and A. Chandrakasan, "MTCMOS Sequential Circuits," in *Proceedings of the 27th European Solid-State Circuits Conference*, Sept. 2001, pp. 317 –320.

[17] X. Kavousianos, K. Chakrabarty, A. Jain, and R. Parekhji, "Test Scheduling for Multicore SoCs with Dynamic Voltage Scaling and Multiple Voltage Islands," in *20th Asian Test Symposium,*, Nov. 2011, pp. 33–39.

[18] ——, "Test Schedule Optimization for Multicore SoCs: Handling Dynamic Voltage Scaling and Multiple Voltage Islands," *IEEE Transactions on CAD of Integrated Circuits and Systems*, vol. 31, no. 11, pp. 1754 –1766, Nov. 2012.

[19] ——, "Time-Division Multiplexing for Testing SoCs with DVS and Multiple Voltage Islands," in *17th IEEE European Test Symposium*, May 2012, pp. 1–6.

[20] S. Khursheed, B. M. Al-Hashimi, S. M. Reddy, and P. Harrod, "Diagnosis of Multiple-Voltage Design With Bridge Defect," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 28, no. 3, pp. 406–416, March 2009.

[21] S. Khursheed, U. Ingelsson, P. Rosinger, B. Al-Hashimi, and P. Harrod, "Bridging Fault Test Method With Adaptive Power Management Awareness," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 27, no. 6, pp. 1117–1127, June 2008.

[22] S. Khursheed, S. Yang, B. Al-Hashimi, X. Huang, and D. Flynn, "Improved DFT for Testing Power Switches," in *16th IEEE European Test Symposium*, May 2011, pp. 7 –12.

[23] S. Kim, S. Kosonocky, D. Knebel, and K. Stawiasz, "Experimental Measurement of a Novel Power Gating Structure with Intermediate Power Saving Mode," in *Proceedings of International Symposium on Low Power Electronics and Design*, Aug. 2004, pp. 20–25.

[24] S. Kim, S. Kosonocky, D. Knebel, K. Stawiasz, and M. Papaefthymiou, "A Multi-Mode Power Gating Structure for Low-Voltage Deep-Submicron CMOS ICs," *IEEE Transactions on Circuits and Systems II: Express Briefs,*, vol. 54, no. 7, pp. 586 –590, July 2007.

[25] D. Lackey, P. Zuchowski, T. Bednar, D. Stout, S. Gould, and J. Cohn, "Managing Power and Performance for System-on-Chip Designs using Voltage Islands," in *Proceedings of IEEE/ACM International Conference on Computer Aided Design*, Nov. 2002, pp. 195–202.

[26] Magklis, G. and Semeraro, G. and Albonesi, D.H. and Dropsho, S.G. and Dwarkadas, S. and Scott, M.L., "Dynamic Frequency and Voltage Scaling for a Multiple-Clock-Domain Microprocessor," *IEEE Micro,*, vol. 23, no. 6, pp. 62–68, Nov.-Dec. 2003.

[27] S. Mukhopadhyay, C. Neau, R. Cakici, A. Agarwal, C. Kim, and K. Roy, "Gate Leakage Reduction for Scaled Devices using Transistor Stacking," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 11, no. 4, pp. 716–730, Aug. 2003.

[28] S. Mutoh, T. Douseki, Y. Matsuya, T. Aoki, S. Shigematsu, and J. Yamada, "1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 8, pp. 847 –854, Aug. 1995.

[29] E. Pakbaznia and M. Pedram, "Design and Application of Multimodal Power Gating Structures," in *International Symposium on Quality Electronic Design*, March 2009, pp. 120–126.

[30] R. Puri, L. Stok, J. Cohn, D. Kung, D. Pan, D. Sylvester, A. Srivastava, and S. Kulkarni, "Pushing ASIC Performance in a Power Envelope," in *Proceedings of Design Automation Conference*, June 2003, pp. 788–793.

[31] H. Singh, K. Agarwal, D. Sylvester, and K. Nowka, "Enhanced Leakage Reduction Techniques Using Intermediate Strength Power Gating," *IEEE Transactions on VLSI Systems*, vol. 15, no. 11, pp. 1215–1224, Nov. 2007.

[32] L. Souef, C. Eychenne, and E. Alie, "Architecture for Testing Multi-Voltage Domain SOC," in *Proc. of International Test Conference*, Oct. 2008, pp. 1 –10.

[33] Z. Zhang, X. Kavousianos, K. Chakrabarty, and Y. Tsiatouhas, "A Robust and Reconfigurable Multi-mode Power Gating Architecture," in *Proc. of 24th Int. Conf. on VLSI Design*, 2011, pp. 280 –285.

[34] ——, "Static Power Reduction using Variation-Tolerant and Reconfigurable Multi-Mode Power Switches," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, to appear.

[35] Z. Zhang, X. Kavousianos, Y. Luo, Y. Tsiatouhas, and K. Chakrabarty, "Signature Analysis for Testing, Diagnosis, and Repair of Multi-mode Power Switches," in *Proc. of 16th IEEE European Test Symposium*, May 2011, pp. 13 –18.

[36] Z. Zhang, X. Kavousianos, Y. Tsiatouhas, and K. Chakrabarty, "A BIST Scheme for Testing and Repair of Multi-mode Power Switches," in *Proceedings of IEEE 17th International On-Line Test Symposium*, July 2011, pp. 115 –120.