EDAA / ACM SIGDA PhD Forum at DATE 2012 in Dresden

The EDAA / ACM PhD forum is part of the DATE Conference and hosted by ACM SIGDA and the European Design Automation Association (EDAA). It offers the opportunity for PhD students to present their thesis work to a broad audience in the design, automation and test community from academia and industry. During the presentation at the DATE Conference, it helps students to establish contacts. Also, representatives from industry and academia get a glance of state-of-the-art research in design, automation and test. The review process resulted in the selection of the PhD students listed below. We thank the EDAA, ACM SIGDA and DATE for making this Forum possible.

Peter Marwedel (Chair, EDAA / ACM SIGDA PhD Forum at DATE 2012)

PhD Forum Committee

P. Marwedel (Chair), TU Dortmund, Germany

M. Balakrishnan, Indian Institute of Technology, Delhi, India

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U. Rückert, University of Bielefeld, Germany

S. Stuijk, TU Eindhoven, Netherlands

N. Wehn, TU Kaiserslautern, Germany

Admitted Presentations

1. **Aleksejev**, Igor (Tallinn UT, Estonia): Reconfigurable Hardware Based Testing of Complex Electronic Boards
2. **Anagnostopoulos**, Iraklis (ICCS NTU Athens, Greece): Run-time Data Management Services for Many-core Systems
3. **Arjomand**, Mohammad (Sharif UT, Tehran, Iran): Non-Volatile Memory Hierarchy for Chip-Multiprocessors Toward Normally-Off Instant-On Computing
4. **Bi**, Yu (Delft UT, Netherlands): Fast Capacitance Modeling Subject to Manufacturing Variations
5. **Bortolotti**, Daniele (U Bologna, Italy): Instruction Caching Strategies for Tightly-Coupled Shared-Memory Clusters
6. **Cederstroem**, Love (ZMD AG, Dresden, Germany): Methodologies for Co-Development and Joint Simulation of Mixed Co-Development and Joint Simulation of Mixed Signal PBCs and ICs
7. **Daneshtalab**, Masoud (U Turku, Finland): Efficient Multicast Routing Protocols for Networks-on-Chip
8. **Eslami Kiasari**, Abbas (KTH Stockholm, Sweden): Integrated Performance Model of NoCs
9. **Fasthuber**, Robert (KU Leuven, Belgium): A Highly-Efficient Processor Template For Wireless Communication Systems
10. **Fischbach**, Robert (TU Dresden, Germany): Layout Representations for 3D Physical Design Optimization
11. **Gladigau**, Jens (U Erlangen, Germany): Model-Based Virtual Prototyping—Generation, Verification, and Acceleration
12. **Guderian**, Falko (TU Dresden, Germany): The Lambda-Chart Approach: Advancing Methodology for System-Level Design and Exploration
13. **Heinig**, Andreas (TU Dortmund, Germany): Transient Fault-Aware Embedded System Software Design
14. **Jafari**, Fahimeh (KTH Stockholm, Sweden): QoS Aware Communication Management in Networks-on-Chip

15. **Kakoe**, Mohammad (U Bologna, Italy): A Resilient Architecture for Low Latency Communication in shared-L1 processor clusters
16. **Maftei**, Elena (TU Denmark, Denmark): Synthesis of Digital Microfluidic Biochips with Reconfigurable Operation Execution
17. **Meister**, Tilo (TU Dresden, Germany): Pin Assignment Optimization for Improved Routability in Hierarchical Physical Design Flows
18. **Mendoza**, Francisco (FZI Karlsruhe, Germany): Scalable Problem-Oriented Approach for Dynamic Verification of Embedded Systems
19. **Minhass**, Wajid Hassan (TU Denmark, Denmark): System-Level Modeling and Synthesis Techniques for Flow-Based Microfluidic Large-Scale Integration Biochips
20. **Mitea**, Oliver (U Frankfurt, Germany): A Deterministic Automatic Flow for the Synthesis of Analog Circuits
21. **Müller**, Dirk (TU Chemnitz, Germany): Improved Heuristics for Partitioned Multiprocessor Scheduling Based on Rate-Monotonic Small Tasks
22. **Naeem**, Abdul (KTH Stockholm, Sweden): Shared Memory Consistency Models Evaluation in NoC based Multicore Systems
23. **Paterna**, Francesco (U Bologna, Italy): Variability-Aware Task Allocation for Energy-Efficient Quality of Service Provisioning in Embedded Streaming Multimedia Applications
24. **Pinto**, Christian (U Bologna, Italy): GPGPU-Accelerated Parallel and Fast Simulation of Thousand-Core Platforms
25. **Singh**, Amit Kumar: (NTU Singapore, Singapore): Run-Time Mapping Techniques for NoC-based Heterogeneous MPSoC Platforms
26. **Stattelmann**, Stefan (FZI Karlsruhe, Germany): Hybrid Source-Level Timing Simulation
27. **Strano**, Alessandro (U Ferrara, Italy): Exploiting Structural Redundancy of SIMD Accelerators for their Built-In Self-Testing/Diagnosis and Reconfiguration
28. **Tang**, Qin (TU Delft, Netherlands): New Statistical Timing Analysis Method Considering Process Variations and Crosstalk
29. **Thaden**, Eike (U Oldenburg, Germany): Semi-Automatic Optimization of Hardware Architectures in Embedded Systems
30. **Tripathi**, Jai Narayan (IIT Bombay, India): Nonlinear Modeling and Optimization of Analog/RF Circuits by Design of Experiments
31. **Vinco**, Sara (U Verona, Italy): UNIVERCM: a Formal Computational Model for Correct Manipulation and Transformation of Heterogeneous Embedded Systems
32. **Wang**, Chao (U Suzhou, China): Service-Oriented Reconfigurable Multi-Processor System on Chip
33. **Wist**, Dominic (U Potsdam, Germany): Logic Synthesis of Complex Asynchronous Circuits
34. **Yang**, Yang (TU Eindhoven, Netherlands): Exploring Resource/Performance Trade-Offs for Streaming Applications on Embedded Multiprocessors
35. **Yu**, Heng (U Erlangen, Germany): Dynamic Scheduling Techniques for Adaptive Applications on Real-Time Embedded Systems