Estimation Based Power and Supply Voltage Management for Future RF-Powered Multi-Core Smart Cards

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Abstract—**RF-powered smart cards are constrained in their operation by their power consumption. Smart card application designers must pay attention to power consumption peaks, high average power consumption and supply voltage drops. If these hazards are not handled properly, the smart card's operational stability is compromised.**

Here we present a novel multi-core smart card design, which improves the operational stability of nowadays used smart cards. Estimation based techniques are applied to provide cycle accurate power and supply voltage information of the smart card in real time. A supply voltage management unit monitors the provided power and supply voltage information, flattens the smart card's power consumption and prevents supply voltage drops by means of a dynamic voltage and frequency scaling (DVFS) policy.

The presented multi-core smart card design is evaluated on a hardware emulation platform to prove its proper functionality. Experimental tests show that harmful power variations can be reduced by up to 75% and predefined supply voltage levels are maintained properly. The presented analysis and management functionalities are integrated at a minimal area overhead of 10.1%.

I. INTRODUCTION

A smart card system is generally divided into two components: A reader device and the smart card itself. The reader device generates an RF field, which is used for both power supply and communication purposes. This RF field induces an electrical current in the smart card's antenna to power the smart card's electronics. Fig. 1 illustrates this principle. In order to ensure a reliable operation of the smart card, the following aspects need to be considered.

The available electrical power is very limited and depends on the distance between smart card and reader device, antenna design and orientation, etc. Attention must be paid to high average power consumption, high power peaks and card movements within the RF field. These issues may cause the processor's supply voltage to fluctuate. In case the supply voltage drops below a certain threshold, the system's operational stability can not be guaranteed anymore. Fig. 2 shows the severe impact of high power consumption changes on the smart card's supply voltage: The greater the power consumption increase, the more severe the supply voltage drops. A smart card power management system must consider the following crucial points:

- The power consumption needs to be flattened to reduce the possibility for supply voltage drops.
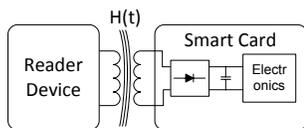
Fig. 1. Principle of a smart card system consisting of the smart card and a reader device, which generates a RF field for power supply and communication purposes.
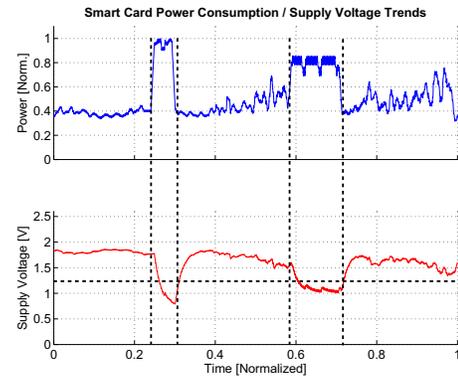
Fig. 2. This graph shows the influences of power consumption changes on the smart card system's supply voltage. The greater the power consumption increases, the more severe the supply voltage drops. If the supply voltage drops below the threshold, operation stability is lost.

- The processor's supply voltage must not drop below a certain threshold to avoid malfunctions.

This paper makes the following contributions. It presents a novel multi-core smart card design, which is enhanced with estimation based power and supply voltage analysis capabilities to detect hazards, such as high average power consumption, power consumption peaks and supply voltage drops. Furthermore, a supply voltage management unit is used to dynamically adapt the smart card processor cores' clock frequency and voltage parameters. With the help of a dynamic voltage and frequency scaling (DVFS) policy, the smart card's power consumption is being flattened and supply voltage drops are avoided. Thus, the stability of the smart card is improved.

II. RELATED WORK

A. Power Analysis

Power analysis is a technique to determine the power consumption of electric circuits. It is basically done either *measurement based* or *estimation based*. Power estimation is conducted at any abstraction level and can be further subdivided into *simulation based* and *hardware accelerated* techniques. Depending on the abstraction level and the circuit size, simulation based approaches can consume a significant amount of calculation time. Hardware accelerated power estimation is performed to speed up the complex and time intense calculations. It is achieved by integrating synthesizeable power simulation algorithms and estimation algorithms in hardware. Implementations are presented in [1] and [2]. Coburn et al. coined in [3] the term *Power Emulation* by integrating a design-under-test as

well as register transfer level power macromodels into an FPGA to estimate the power consumption of the design-under-test. A system-level power emulation implementation is presented in [4].

B. Power Management

Dynamic power management describes techniques to save power in integrated circuits according to their states of operation. Tiwari et al. describe in [5] several methodologies like clock gating, guarded evaluation, bus deactivation, etc. In contrast to other dynamic power management methods, DVFS offers an elegant way for power consumption adjustments of integrated circuits according to the CMOS dynamic power consumption equation. Multi-core DVFS approaches can be divided into per-core and chip-wide DVFS. Investigations regarding these two strategies are conducted in [6] and show that power saving improvements of up to 21% can be achieved if per-core DVFS strategies are applied in a four-core processor system. Various DVFS policy implementations are evaluated in [7] and [8].

C. Supply Voltage Analysis

Supply voltage analysis covers methodologies to determine the supply voltage of electric circuits. Supply voltage analysis is either done at design time or at run time. A simulation based approach, which models a power supply network, is presented in [9]. Voltage drops are detected in [10] with the help of on-die circuits. Analog-to-digital converters [11] and voltage comparators [12] are further possibilities to detect hazardous supply voltage levels. A supply voltage emulation approach is suggested in [13]. In this estimation based method, the design-under-test as well as a supply voltage analysis unit are integrated into an FPGA. Supply voltage estimates are performed in hardware and in real time.

D. Supply Voltage Management

Supply voltage management methods are based upon supply voltage analysis techniques and are applied to control an electric circuit's supply voltage level. On-die circuits are presented in [10] to compensate supply voltage drops. Up to 100 mA are injected into specific nodes. In [14], supply voltage drops are prevented by shaping the electrical current with the help of a semi-asynchronous architecture. A predictive approach is presented in [15]. Signatures of the running program are compared to hazardous patterns. In case of a match, the processor is throttled and the supply voltage regenerates. Supply voltage emulation approaches, as presented in [13], are also used in conjunction with DVFS techniques to prevent supply voltage hazards.

III. Estimation Based Power / Voltage Analysis and Management

The proposed novel smart card design consists of a symmetric dual-core processor, which is enhanced with estimation based power consumption and supply voltage analysis units as well as a supply voltage management unit. In the following paragraph, each smart card component will be described in detail.

A. Power Estimation Unit

The used power estimation unit is based upon an approach from [4]. Its task is to derive power consumption information of the smart card processor cores based on their internal system states. The basic functionality is depicted in Fig. 3. The power estimation unit features a linear regression based smart card power model, which is based
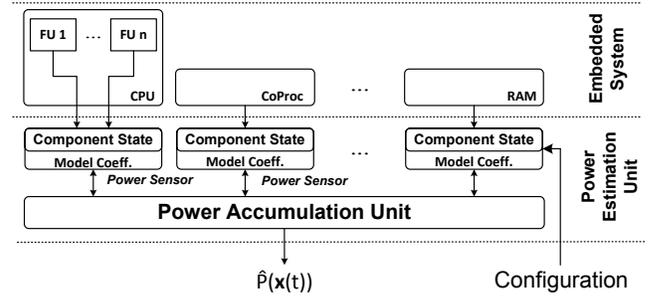
Fig. 3. Power estimation unit gathering power information by observing the system activity, obtained with changes from [4].

upon [16]. This hardware integrated power model is defined by (1) and (2).

$$\widehat{P}(\mathbf{x}) = \widehat{P}_{stat} + \widehat{P}_{dyn} = c_0 + \sum_{i=1}^{n} c_i \cdot x_i = c_0 + \mathbf{c^T} \cdot \mathbf{x} \quad (1)$$

$$P(\mathbf{x}) = \widehat{P}(\mathbf{x}) + \epsilon \quad (2)$$

$\mathbf{x} = [x_1, x_2, x_3, ...]$ is a vector, whose elements specify a certain system state (e.g., memory read, memory write, CPU running, etc). Every system state x_i has a model coefficient c_i from the vector $\mathbf{c^T} = [c_1, c_2, c_3, ...]^T$ assigned to itself. A model coefficient c_i defines how much power is dissipated while being in the corresponding system state x_i. These model coefficients c_i and the leakage power consumption c_0 are obtained from a power model characterization process. The linear combinations of x_i and c_i plus c_0 form the power estimates $\widehat{P}(\mathbf{x})$. The difference between the estimated value $\widehat{P}(\mathbf{x})$ and the real value $P(\mathbf{x})$ is given by the error ϵ. A time dependency is introduced by $\widehat{P}(\mathbf{x}(t))$, because system states may change at any clock cycle.

B. DVFS Scaling

Power estimates $\widehat{P}(\mathbf{x})$ are based upon a smart card processor core, which is operated at a clock frequency f of 1 MHz. To respect the possibility of operating a processor core at various clock frequencies and voltage parameters, a DVFS scaling unit is introduced. This unit scales the 1 MHz based power estimates $\widehat{P}(\mathbf{x}(t))$ according to (3).

$$\widehat{P}(\mathbf{x}(t), f(t), V_{DD}(t)) = \widehat{P}(\mathbf{x}(t)) \cdot f(t) \cdot V_{DD}^2(t) \quad (3)$$

A lookup table (LUT) approach is used in this unit, which maps each supported processor clock frequency $f(t)$ to a dedicated voltage $V_{DD}(t)$. The architecture of the hardware integrated DVFS scaling unit is depicted in Fig. 4.

C. Supply Voltage Estimation Unit

According to [17], an equivalent electrical circuit of a contactless smart card power supply network can be drawn as depicted in Fig. 5. $v_i(t)$ represents the rectified voltage, which is supplied by the RF
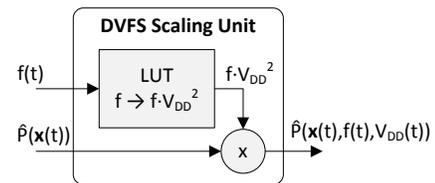
Fig. 4. Architecture of the DVFS scaling unit.
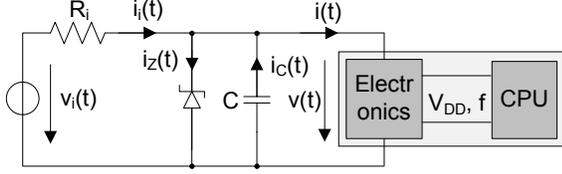
Fig. 5. Equivalent circuit of a smart card power supply network, obtained with changes from [17]. $v(t)$ represents the crucial supply voltage, which is applied to the smart card's electronics.

field to the smart card's antenna. A voltage sensor is typically used to retrieve the voltage level of $v_i(t)$. Capacitor C buffers electrical charges and is charged / discharged depending on the processor's power consumption. The charge level of this capacitor C defines the supply voltage $v(t)$ of the smart card's electronics according to (4).

$$v(t) = \frac{Q_C(t)}{C} \qquad (4)$$

$i(t)$ is derived from the power consumption information, which is estimated and delivered by the power estimation unit. An electrical charge based mathematical model computes the crucial supply voltage $v(t+1)$ according to (5). Δt represents the reciprocal value of the currently set processor clock frequency. The presented calculations can be implemented in hardware easily. Modeling the transient behavior of a switching capacitor is normally expressed by an exponential based function. With the help of the introduced charge based approach, an expensively hardware integrated exponential function is bypassed.

$$v(t+1) = \frac{Q_C(t) + \frac{v_i(t) - v(t)}{R_i} \Delta t - i(t) \Delta t}{C} \qquad (5)$$

The functionality of the hardware integrated supply voltage estimation unit has been verified with SPICE simulations of the underlying model. A mean squared error in the range of only 10^{-5} is detectable. Fig. 6 illustrates the results. Note, according to [17], the maximum error between physical measurements and the smart card's power supply network model is as high as 2%.

D. Supply Voltage Management Unit

The DVFS technique is used to modify the power consumption of each smart card processor core by modifying voltage V_{DD} and
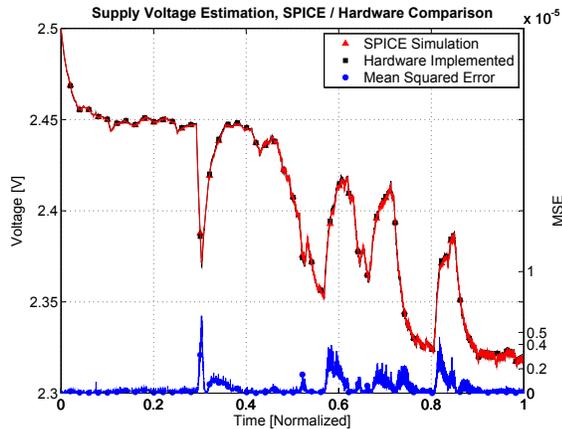
Fig. 6. Accuracy comparison of the hardware integrated supply voltage estimation unit and SPICE simulations of the underlying model.
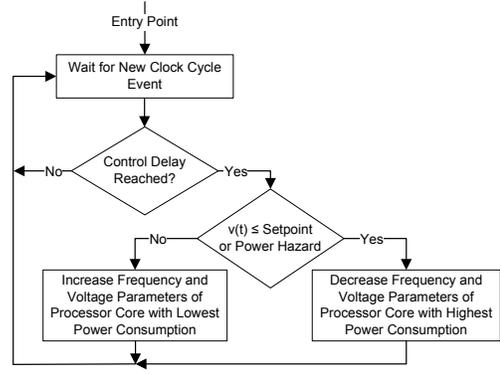
Fig. 7. Flow chart of the proposed per-core DVFS policy dealing with supply voltage and power consumption hazards.

frequency f parameters. DVFS has a cubic impact on the power consumption but a linear impact on the performance. Fig. 7 illustrates the per-core DVFS policy, which is optimized for multi-core smart cards. This policy uses the provided supply voltage and power consumption estimates for DVFS control decisions. Therefore, fast power consumption changes as well as slightly slower and delayed supply voltage variations are handled simultaneously. The DVFS policy supports a user defined supply voltage setpoint.

- For the case where the instantaneous supply voltage $v(t)$ is lower than the supply voltage setpoint or a power consumption hazard is detected, the processor core with the highest power consumption has its clock frequency f and voltage level V_{DD} decreased.
- Otherwise, if the instantaneous supply voltage $v(t)$ is higher than the supply voltage setpoint and no power consumption hazard is detected, the processor core with the lowest power consumption is accelerated and its voltage level is increased.

A control delay is added to cope with the switching delays and settling times of on-chip voltage and frequency regulators. This DVFS policy is designed to flatten the smart card's power consumption and to prevent supply voltage drops simultaneously. Furthermore, the performance of the smart card is optimized regarding the defined supply voltage setpoint constraint.

E. Power and Supply Voltage Aware Smart Card

Fig. 8 shows the proposed architecture of the novel power and supply voltage aware multi-core smart card. The processor cores' system states $\mathbf{x}_i(t)$ are monitored and their associated power consumption information $\widehat{P}(\mathbf{x}_i(t))$ is delivered by power estimation units. Then, $\widehat{P}(\mathbf{x}_i(t))$ is scaled according to the currently set voltage V_{DDi} and frequency f_i parameters. The results, $\widehat{P}(\mathbf{x}_i(t), f_i(t), V_{DDi}(t))$ are summed up and form the power consumption value $\widehat{P}_S(t)$. $\widehat{P}_S(t)$ is then forwarded to the supply voltage estimation unit. The supply
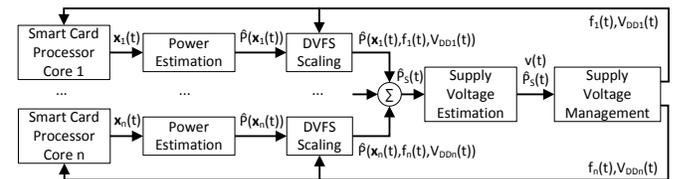
Fig. 8. Architecture of the proposed power and supply voltage aware multi-core smart card.

voltage estimation unit delivers the supply voltage $v(t)$ information of the smart card's electronics by means of the presented power supply network model. The supply voltage $v(t)$ and power consumption $\widehat{P}_S(t)$ information is then forwarded to the supply voltage management unit. This unit controls the smart card processor cores' DVFS parameters V_{DDi} and f_i according to the proposed per-core DVFS policy.

IV. HARDWARE EMULATION

Experimental results are gained by performing functional emulation as well as power and supply voltage emulation of the proposed future multi-core smart card. Fig. 9 illustrates the basic concept of this emulation approach. The emulation system is built by integrating the smart card processor cores as well as the power estimation, supply voltage estimation and management units into a Xilinx Spartan 3 FPGA. Relevant trace information is generated and transmitted with the help of an Ethernet interface to a host PC. The data is collected by the PC and further analysis and verification tasks are performed. This method allows power consumption and supply voltage analysis of a design-under-test early in its design stage. Power bugs within the smart card design can be found and corrected before the tape-out.

V. EXPERIMENTAL RESULTS

The smart card's power estimation and supply voltage estimation units are used to survey the power consumption and supply voltage behavior while executing various benchmarks. The supply voltage management unit is used during these tests to monitor and control the stability of the smart card. A supply voltage setpoint of 1.7 V is defined and DVFS techniques are applied to maintain it. MiBench [18], a representative benchmarking suite for embedded systems, is used for reproducible testing purposes. Table I explains the shown parameters of the following figures.

The left subplots of Fig. 10 and Fig. 11 illustrate the unmanaged curves of FFT and Quicksort benchmarking tests while operating the
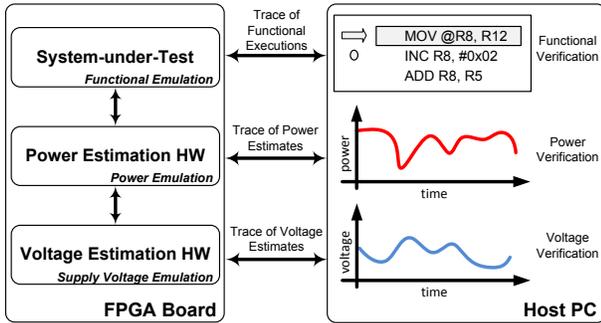
Fig. 9. Principle of the emulation system, obtained with changes from [4].

TABLE I
DESCRIPTION OF THE USED FIGURE PARAMETERS

Parameter	Description
$\widehat{P}_S(t)$	Processor cores 1 and 2 power consumption summation.
$v(t)$	Supply voltage, which is applied to the smart card's electronics.
$v_i(t)$	Rectified supply voltage, which is generated by the RF field.
f_{Ci}	Clock frequencies, which are applied to processor cores 1 and 2.
VDD_{Ci}	Voltage values, which are applied to processor cores 1 and 2.
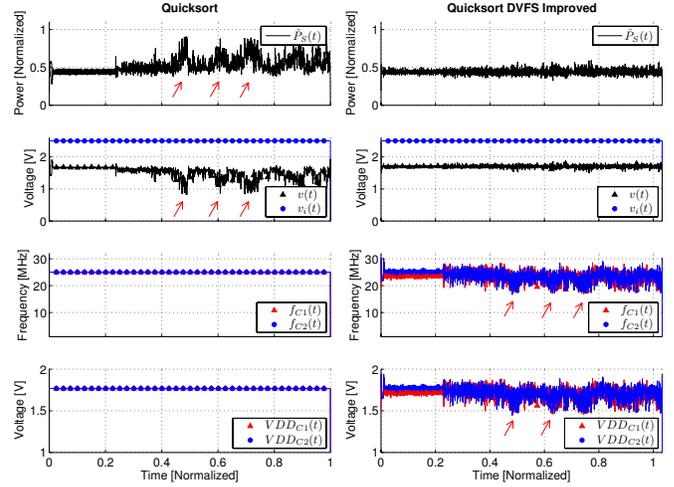
Fig. 10. The left subplots show the unmanaged behavior of the smart card while performing a Quicksort benchmark and applying a fixed clock frequency of 25 MHz. $v(t)$ drops below 1 V. The right subplots show the DVFS managed smart card behavior. The power consumption $\widehat{P}_S(t)$ is flattened and $v(t)$ supply voltage drops are avoided.
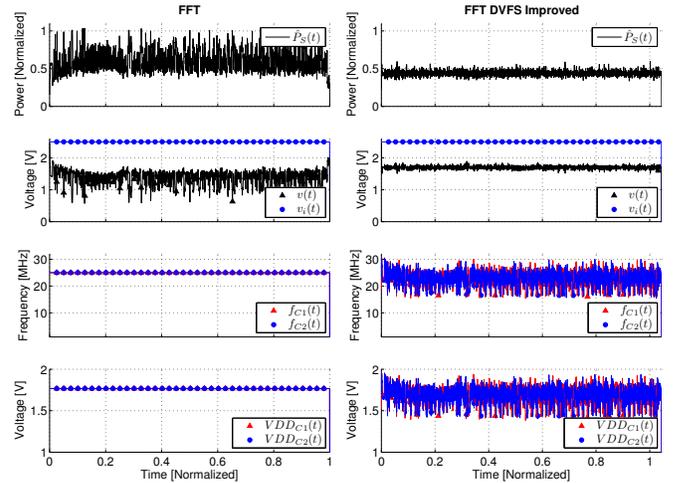
Fig. 11. The left subplots show the unmanaged behavior of the smart card while performing an FFT benchmark and applying a fixed clock frequency of 25 MHz. $v(t)$ drops below 1 V. The right subplots show the DVFS managed smart card behavior. The power consumption $\widehat{P}_S(t)$ is flattened and $v(t)$ supply voltage drops are avoided.

smart card at a fixed clock frequency of 25 MHz. Arrows mark significant $\widehat{P}_S(t)$ power consumption increases. These power consumption hazards cause supply voltage drops below 1 V. Thus, the operational stability of the smart card is compromised. The right subplots of Fig. 10 and Fig. 11 show the curves of the smart card's behavior while taking advantage of the supply voltage management unit. The user defined supply voltage setpoint of 1.7 V is maintained and the power consumption $\widehat{P}_S(t)$ is flattened simultaneously. Arrows mark significant DVFS parameter reductions when $v(t)$ supply voltage hazards are recognized. Thus, the smart card's operational stability is provided. Due to the DVFS interventions, the total runtime of Quicksort and FFT benchmarks are increased by 3.3% and 4.4%, respectively.

Table II shows standard deviation delta values of the total power

TABLE II
COMPARISON OF STANDARD DEVIATION AND PERFORMANCE VALUES

Benchmark	Setpoint	$\Delta\sigma(\widehat{P}_S(t))$	$\Delta\sigma(v(t))$	Perf. Degrad.
Quicksort	1.70 V	-69%	-72%	3.3%
Basicmath	1.70 V	-75%	-78%	13.6%
FFT	1.70 V	-75%	-76%	4.4%
Quicksort	1.66 V	-68%	-72%	0%
Basicmath	1.50 V	-62%	-67%	0%
FFT	1.61 V	-71%	-74%	0%

consumption $\widehat{P}_S(t)$ and the supply voltage $v(t)$ as well as performance degradation values of three selected benchmarks. The standard deviation metric is an indicator for the severity of power consumption peaks and supply voltage drops. The higher the power consumption standard deviation, the higher the possibility for severe supply voltage drops, and consequently the lower the smart card's stability. Comparisons are done between an unmanaged smart card running at 25 MHz and the DVFS managed smart card, which is controlled at a supply voltage setpoint of 1.7 V. Furthermore, results of benchmarks with supply voltage setpoints are presented, which do not cause any performance degradation compared to the 25 MHz reference. This is achieved by reducing a supply voltage setpoint, which speeds up the processor cores. According to the presented results, power consumption standard deviation reductions of up to 75% can be obtained during the FFT benchmark while degrading the performance by only 4.4% . If the FFT benchmark's supply voltage setpoint is reduced by 0.09 V, a power consumption standard deviation reduction of 71% can still be accomplished without degrading the performance.

A. Performance Degradation Investigations

If DVFS modifications are conducted, then the runtime of the executed program can be influenced. Fig. 12 illustrates the performance degradation trend of the FFT benchmark depending on the selected supply voltage setpoint. Results are obtained from hardware emulations. A smart card constantly running at 25 MHz is used as performance reference. The higher the supply voltage setpoint, the lower the power dissipation, but the higher the performance degradation.

If the smart card's electronics allow a supply voltage setpoint reduction, then the processor cores can be operated at a higher clock frequency than the 25 MHz reference. According to Fig. 12, a FFT benchmark performance increase is detectable if supply voltage setpoints of less than 1.61 V are applied.
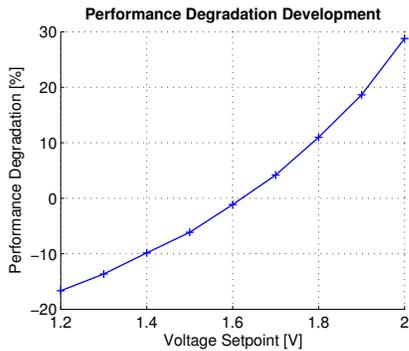
Fig. 12. FFT benchmark performance degradation, compared to a reference smart card running at 25 MHz. The higher the supply voltage setpoint, the higher the performance degradation.

B. Accuracy of the Results

The accuracy of the proposed smart card's analysis and management units is mainly controlled by the power estimation unit: Supply voltage estimates are based upon power consumption estimates and DVFS decisions are based upon supply voltage estimates. According to [4], the maximum average error of the power estimation unit is as high as 8.4%. Comparisons are conducted between power consumption estimates and gate-level power simulations. The power estimation unit's accuracy can be improved easily by considering more signals of the smart card's processor during the power model characterization process.

[17] shows that the model of the smart card's power supply network, which is implemented in the supply voltage estimation unit, accounts for an average error of 2%. The difference between SPICE and hardware integrated power supply network model is in the range of only 10^{-5} and can therfore be neglected.

C. Area Overhead

The proposed enhanced smart card design requires only an additional area overhead of 10.1%. Table III shows a detailed area breakdown of each smart card component. These results are gained from synthesis on a Xilinx Spartan 3 FPGA platform. There is still optimization potential available. For example, the size of the power and supply voltage estimation units can be reduced significantly if less accuracy would be sufficient or if only one processor core would be supported.

VI. CASE STUDY: SMART CARD MOVEMENTS

In the following case study, a reader device generates an RF field and the smart card is moved within this field. Fig. 13 depicts the case study's setup. Due to the smart card movement, the smart card is exposed to a varying RF field strength. A varying RF field strength induces a varying electrical current in the smart card's antenna. Consequently, the supply voltage $v_i(t)$, the charge level $Q_C(t)$ of the capacitor C as well as the smart card electronics' supply voltage $v(t)$ are affected. The smart card movement is modeled by a triangular characteristic of $v_i(t)$. The aim of this case study is to verify if the proposed power and supply voltage aware smart card is able to cope with such instable environmental conditions.

The left subplots of Fig. 14 illustrate the unmanaged power consumption, supply voltage and DVFS parameter curves of the Quicksort benchmark while $v_i(t)$ changes. As a result, the crucial

TABLE III
AREA CONSUMPTION BREAKDOWN OF THE PROPOSED POWER AND
SUPPLY VOLTAGE AWARE MULTI-CORE SMART CARD

Component	Area Overhead
Two-Core Smart Card Processor	-
Power Estimation Units	4.8%
Supply Voltage Estimation Unit	3.8%
Supply Voltage Management Unit	1.4%
Total Area Overhead	10.1%
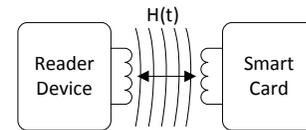
Fig. 13. Illustration of the case study's setup. The smart card is moved within the RF field. Therefore, a varying amount of electrical power is drawn from the RF field.
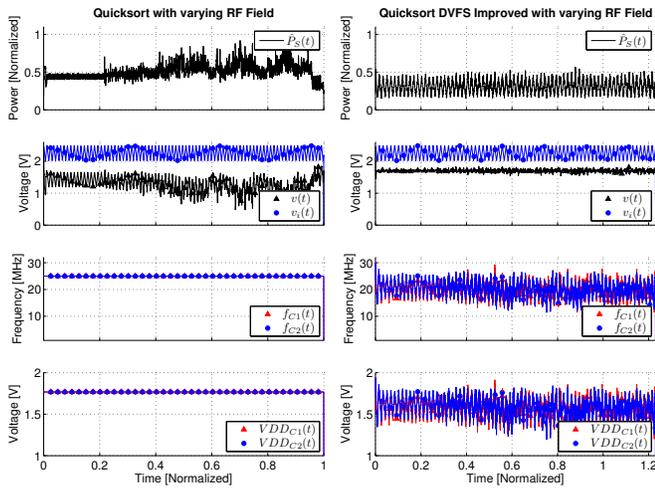
Fig. 14. The left subplots show the unmanaged smart card behavior while moving the smart card within the RF field and performing a Quicksort benchmark. No $v(t)$ stability is given. The right subplots show the same test but with activated DVFS management. $v(t)$ stability is provided properly.

supply voltage $v(t)$ shows a high amount of instability and drops several times down to 0.5 V. The operational stability of the smart card is compromised. The right subplots of Fig. 14 show the behavior of the DVFS enhanced smart card. It is able to stabilize the supply voltage $v(t)$ at the predefined setpoint of 1.7 V properly. No hazardous supply voltage drops are detectable, even under these challenging environmental conditions. Thus, the smart card's operational stability is given. As a further consequence of DVFS interventions, a performance degradation of 22% is observable.

VII. Conclusion

RF-powered smart cards are constrained in their operation by their power consumption. At the time a smart card and its corresponding application is designed, attention must be paid to high average power consumption, power peaks and supply voltage drops. If these power and supply voltage variations are not handled properly, the operational stability of a smart card can be compromised.

This paper proposes a novel multi-core smart card design, which is enhanced with analysis and management functionalities to cope with power consumption and supply voltage hazards. Power estimation and supply voltage estimation units are used to provide cycle accurate power consumption and supply voltage information of the smart card in real time. This information is passed to a supply voltage management unit. The supply voltage management unit flattens the smart card's power consumption, prevents supply voltage drops and optimizes the smart card's performance for a predefined supply voltage setpoint by means of a DVFS policy. Experimental results show that the smart card's power consumption standard deviation can be reduced by up to 75%. The enhanced smart card design also copes with varying RF field strengths and maintains a predefined supply voltage threshold properly. The suggested analysis and management units can be integrated into a smart card design with an additional needed area overhead of only 10.1%.

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