

2011 EDAA / ACM SIGDA PhD Forum at DATE in Grenoble

The EDAA / ACM PhD forum is part of the DATE Conference and hosted by ACM SIGDA and the European Design Automation Association (EDAA). It offers the opportunity for PhD students to present their thesis work to a broad audience in the design, automation and test community from academia and industry. During the presentation at the DATE Conference, it helps students to establish contacts. Also, representatives from industry and academia get a glance of state-of-the-art research in design, automation and test. The review process resulted in the selection of the PhD students listed below. We thank the EDAA, ACM SIGDA and DATE for making this Forum possible.

Peter Marwedel (Chair, 2011 EDAA / ACM PhD Forum at DATE)

PhD Forum Committee

P. Marwedel (Chair), TU Dortmund, Germany
W. Anheier, Bremen University, Germany
M. Balakrishnan, Indian Institute of Technology, Delhi, India
D. Bertozzi, University of Bologna, Italy
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P. Puschner, TU Wien, Austria
U. Rückert, University of Bielefeld, Germany
M. Schimmler, University of Kiel, Germany
S. Stuijk, TU Eindhoven, Netherlands
T. Vierhaus, TU Cottbus, Germany
N. Wehn, TU Kaiserslautern, Germany

Admitted Presentations

1. **Abel, Nobert** (University of Heidelberg): Design and Implementation of an Object-Oriented Framework for Dynamic Partial Reconfiguration
2. **Akesson, Benny** (TU Eindhoven): Predictable and Composible System-on-Chip Memory Controllers
3. **Akkouche, Nouredine** (TIMA, Grenoble): Optimization of production test of analog and RF circuits using statistical modelling techniques
4. **Anwar, Al-Khateeb** (Politecnico di Torino): Model-Based Design of Low-Energy Wireless Sensor Networks
5. **Bako, Laszlo** (Sapientia – Hungarian University of Transylvania): Hardware Implementations of Artificial Neuromorphic Neural Network Systems using Reconfigurable Digital Devices
6. **Bartolini, Andrea** (University of Bologna): Thermal and Energy Management for High-Performance Multicores
7. **Bhasin, Shivam** (Telecom-Paristech): Logic Level-Countermeasures to Secure FPGA-based Designs
8. **Calimera, Andrea** (Politecnico di Torino): Design Techniques and EDA Tools for Reliable and Aging-Free, Low-Power Digital Systems
9. **Tsertov, Anton** (Tallinn University of Technology): Modeling Framework for Beyond the SoCs Test Automation
10. **Daneshtalab, Masoud** (University of Turku): Efficient Multicast Routing Protocols for Networks-on-Chip
11. **Dubois, Matthieu** (TIMA, Grenoble): Test metrics estimation of complex analog and mixed-signal circuits at the design stage
12. **Ebrahimi, Masoumeh** (University of Turku): Unicast and Multicast Communication Protocols in Networks on Chip
13. **Elm, Melanie** (University of Stuttgart): Built-In Self-Diagnosis for Ultra-Large Scale Integrated-Circuits
14. **Facchini, Marco** (IMEC, Leuven): Configurable low-latency 3D-memory dies, integrated using through silicon VIAs

15. **Fazeli, Mahdi** (Sharif University, Tehran): Soft Error Rate Estimation and Mitigation in Digital Circuits
16. **Foroutan, Sahar** (TIMA, Grenoble): An Analytical Method for the Performance Evaluation of Networks-on-Chip
17. **Gaillardon, Pierre-Emmanuel** (CEA, LETI, Minatec Campus, Grenoble): Resistive-memory-based architectures for configurable logic circuits
18. **Gaspar, Lubos** (Université de Lyon): Cryptographic NIOS II extension with secure key management
19. **Gentile, Guiseppe** (European Space Research and Technology Centre, Noordwijk): Study and design of decoder architectures of Low-Density Parity-Check and Turbo Codes for high-rate flexible communication systems
20. **Ghavami, Behnam** (Amirkabir University, Tehran), High Yield Design of Carbon Nanotube-based Digital Circuits in the Presence of Large Variation
21. **Di Guglielmo, Luigi** (University of Verona): Discrete Code Generation from Hybrid Automata
22. **Hanumaiah, Vinay** (ASU, Tempe): Different aspects of dynamic thermal management (DTM)
23. **Hartmann, Philipp A.** (OFFIS, Oldenburg): Application-driven Design for Efficient Simulation of Complex Hardware/Software Systems
24. **Huang, Huang** (Florida International University): Leakage Conscious Power and Thermal Aware Scheduling Techniques for Real-Time Computing Systems
25. **Jose, Bijoy** (Fermat Lab, Blacksburg): Formal model driven software synthesis for embedded systems
26. **Kakoei, Mohammad** (University of Bologna): Automatic Synthesis of Near-Threshold Circuits with Fine-Grained Performance Tunability
27. **Kostin, Sergei** (Tallinn University of Technology): Macro Level Defect-Oriented Diagnosability of Digital Circuits
28. **Langer, Jan** (TU Chemnitz): High-Level Synthesis Using Operation Properties
29. **Lin, Lang** (University of Massachusetts): Cryptographic Circuit Design in Nanometer CMOS Technologies
30. **Ludovici, Daniele** (University of Ferrara): Technology Aware Network-on-Chip Connectivity and Synchronization Design
31. **Ma, Kun** (University of Illinois at Chicago): Concurrent Error Detection Techniques: Countermeasures for Fault Attacks on Cryptosystems
32. **Obien, Marie Engelen** (NAIST, Nara): Studies on F-Scan: A Design for Testability Method for Functional RTL Circuits
33. **Ost, Luciano** (University of York): Abstract Models of NOC-Based MPSoCs for Design Space Exploration
34. **Paolieri, Marco** (University of Catalunya): A multicore architecture for safety critical real-time embedded systems
35. **Paterna, Francesco** (University of Bologna): Variability-tolerant High-reliability Multicore Platforms
36. **Rahman, Mohammad** (University of Texas): Power and Leakage Minimization for Digital ICs
37. **Salimi Khaligh, Rauf** (University of Stuttgart): Transaction Level Modeling and High Performance Simulation of Embedded Systems
38. **Schröder, Christian** (TU Braunschweig): Configuration Interoperability of Hardware-Software-Models in SystemC
39. **Shafique, Muhammad** (Karlsruhe Institute of Technology): Architectures for Adaptive Low-Power Embedded Multimedia Systems
40. **Sotiriou-Xanthopoulos, Efsthios** (University of Athens): A Bottom-Up Methodology for Run-Time Reconfigurable RTL Components
41. **Spies, Christopher** (TU Darmstadt): Model-Based Feasibility Analysis for Digital Beam Phase Control in a Heavy-Ion Synchrotron
42. **Suelflow, Andre** (University of Bremen): WoLFram - A Word Level Framework for Formal Verification and its Application
43. **Trouve, Antoine** (Kyushu University): A Fast, Flexible and Portable Design Space Exploration Tool for DR-ASIP
44. **Wang, Zhonglei** (TU München): Software Performance Estimation Methods for System-Level Design of Embedded Systems
45. **Xue, Bing** (Fermat Lab, Blacksburg): Formal Approach for Latency Insensitive Design Optimization
46. **Zaourar, Lilia** (Laboratoire G-SCOP INP, Grenoble): Optimizing Design For Test Techniques