3D-ICML: A 3D Bipolar ReRAM Design with Interleaved Complementary Memory Layers

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***Abstract*— Resistive random access memory (ReRAM) has been demonstrated as a promising non-volatile memory technology with features such as high density, low power, good scalability, easy fabrication and compatibility to the existing CMOS technology. The conventional three-dimensional (3D) bipolar ReRAM design usually stacks up multiple memory layers that are separated by isolation layers, e.g. Spin–on–Glass (SOG). In this paper, we propose a new 3D bipolar ReRAM design with interleaved complimentary memory layers (3D-ICML) which can form a memory island without any isolation. The set of metal wires between two adjacent memory layers in vertical direction can be shared. 3D-ICML design can reduce fabrication complexity and increase memory density. Meanwhile, multiple memory cells interconnected horizontally and vertically can be accessed at the same time, which dramatically increases the memory bandwidth.**

I. Introduction

Nowadays, the traditional data storages, i.e., hard disk drive (HDD) and Flash memory, are facing great challenges as technology node scales beyond 22nm and below. Various emerging non-volatile memory devices have been investigated by industry and academia institutes. In particular, resistive random access memory (ReRAM) is expected to be a promising candidate to traditional data storage for its promise of high density, low power and fine scalability [1].

ReRAM can generally denote all the memory technologies that rely on resistance change to store information. Many ReRAM technologies with various storage mechanisms have been extensively studied [2]. In this work, we focus on only bipolar ReRAM memory design and use Cu-$Ge_{0.3}Se_{0.7}$-SiO_2-Pt [3] as an example for demonstration purposes. The proposed design concept can be easily extended to the other bipolar ReRAM devices.

The most popular array structure used in ReRAM design is called the crossbar architecture, within which each memory device is built at the cross point of two metal wires. Because of its simple structure, the crossbar array can provides a high device density and quadratic scalability in the advanced technologies [4].

Conventional 3D ReRAM is constructed by stacking up multiple memory arrays. Isolation between two adjacent memory layers is needed to access multiple cells simultaneously and to keep proper functionalities [5]. To prevent the metal wires from melting (or even destructing) during the annealing step, the low thermal budget process, e.g. undoped Methylsilsesquioxane (MSQ) Spin-on-Glass (SOG) technology [6], is required when fabricating the isolation layers, which results in high process complexity and fabrication cost.

In this paper, we propose a new 3D bipolar ReRAM design with Interleaved Complementary Memory Layers (3D-ICML), which avoids the high-cost fabrication process of isolation layers. For a given memory material, two complementary structures can be built: the original memory stack and the one with a reversed material order. We apply these two structures to odd and even layers alternatively. The metal interconnects between neighbor layers can be shared. Read and write operations in 3D-ICML are discussed.

Compared to the conventional 3D ReRAM design, 3D-ICML has three advantages: (1) a lower process complexity; (2) a higher density considering that more memory layers can be stacked up; and (3) a higher bandwidth because multiple cells can be accessed simultaneously during read and write operations.

The rest of the paper is organized as follows: Section II gives a preliminary introduction on ReRAM device, crossbar array and the conventional 3D ReRAM design. Section III explains the design concept of 3D-ICML and the read/write operations. The future work is discussed in Section IV. At the end, Section V concludes the paper.

II. Preliminary

A. Basics of ReRAM

Although ReRAM technology involves many different storage mechanisms, there are only two "conventional" operation types: unipolar switching and bipolar switching. Within this context, unipolar operation executes the programming/erasing by using short and long pulse, or by using high and low voltage with the same voltage polarity. In contrast, bipolar switching is achieved by short pulses with opposite voltage polarity. This work targets on 3D ReRAM structure with bipolar switching devices.

Fig. 1(a) illustrates the structure of Cu-$Ge_{0.3}Se_{0.7}$-SiO_2-Pt [3], which is used as an example in the paper. It is a programmable metallization cell device formed in sandwich structure with heterogeneous solid metal electrodes at two poles – one is relatively inert Pt and the other is electrochemically active Cu. A thin electrolyte film composed of ternary glass $Ge_{0.3}Se_{0.7}$ with added dissolving active metal Cu is placed between two electrodes. In addition, SiO_2 is used as a buffer layer to improve the endurance in the electrolyte [7]. When a negative bias is applied to the Pt electrode during

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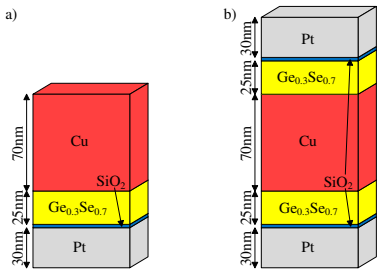

Fig. 1. (a) Structure of Cu-$Ge_{0.3}Se_{0.7}$-SiO_2-Pt. (b) The complementary cell structure.

a SET operation, the added Cu reacts with Se in electrolyte compound to form conducting cations which is a "filament" between two electrodes for electron transportation. As a result, the resistance between two electrodes is dramatically reduced. To RESET the cell, a positive bias is applied on the Pt electrode to remove the random dissolving Cu from Cu-Ge-Se compound filament. The resistance becomes relatively high once the filament disappears in the electrolyte [7].

The device parameters of Cu-$Ge_{0.3}Se_{0.7}$-SiO_2-Pt [3][8] are summarized in Table I. Theoretically, a high R_H/R_L ratio, e.g., $10^4 \sim 10^5$ [7], can be obtained. Here, we conservatively choose R_H/R_L = 25 based on testing conducted under a current stress of 30 μA at room temperature [3].

B. ReRAM Crossbar Array

Crossbar array has been used in telecommunication switching systems since 1939, and the similar structure is utilized in nanometer scale ReRAM design: two layers of metal wires connected by memory devices at cross points. It has been widely used in high density memory systems for the smallest cell area – $4F^2$, where F is the minimum feature size. However, crossbar arrays in bipolar ReRAM usually suffer from sneak paths through neighbor cells. To guarantee proper functionality, the voltage across the selected cell must be much higher than those across the other cells on the sneak path [4].

Recently, a complementary ReRAM cell was proposed [8]. The cell structure which is illustrated in Fig. 1(b) illustrates structure is made of two anti-serial ReRAM devices. Independent of the stored binary information, the complementary cell always has at least one device exhibiting high resistance, and therefore, the static power can be reduced. However, writing a single memory cell involves a multi-step write procedure, which brings in power consumption and reliability issues.

C. Conventional 3D ReRAM Design & Process Difficulties

The simplest way to build a 3D ReRAM structure is to stack multiple memory layers vertically [9]. In conventional bipolar ReRAM design, every memory layer has its own sets of memory elements and interconnects. Isolation is required between two neighboring memory layers to prevent interference in between. An improved design can share wordlines (WLs) between two memory adjacent layers which can be accessed/programmed simultaneously [10]. However, bitlines (BLs) cannot be shared, and hence, an isolation layer is still needed.

SOG with MSQ etc. material shows promise in forming isolation layers. However, it has several critical process difficulties. First, the thermal process has to be well controlled to prevent device degradation [11]. Second, misalignment of vias due to SOG [12] needs to be improved. The adhesion of SOG material is also a critical issue [6]. Moreover, the low conductivity of the isolation layer introduces a heat accumulation issue [11][13]. Thus, a 3D memory design excluding an isolation process can significantly benefit from lower fabrication cost and process complexity.

TABLE I
Cu-$Ge_{0.3}Se_{0.7}$-SiO_2-Pt DEVICE PARAMETERS [3][8]

Parameters	Value	explanation
$R_{\rm H}$	40 kΩ	Resistance at high resistance state (HRS).
$R_{\rm L}$	1.6 kΩ	Resistance at low resistance state (LRS).
$V_{\rm SET}$	0.58 V	Threshold voltage to switch device from $R_{\rm H}$ to $R_{\rm L}$.
$V_{\rm RESET}$	-0.65 V	Threshold voltage to switch device from $R_{\rm L}$ to $R_{\rm H}$.
$R_{\rm H}/R_{\rm L}$	25	The ratio of $R_{\rm H}$ to $R_{\rm L}$.

III. 3D Bipolar ReRAM Design With Interleaved Complementary Memory Layers

A. Design Concept

Fig. 2 illustrates the proposed 3D-ICML structure. For simplicity, it includes only four ReRAM memory layers with a crossbar design structure as an example. The basic design concept is to employ complementary material stack structures, i.e. the regular memory stack and the one with a reversed deposition order. For example, Layer 1 uses the regular deposition process (yellow rectangles), and all the memory cells in Layer 2 are made by reversing the deposition sequence (gray rectangles). We apply these two memory stack structures in odd and even layers alternatively. The metal interconnects between any neighboring layers are shared. The process has been successfully demonstrated by Linn *et al.* and the memory cells made with the regular and reversed depositions showed the same device properties [8].

By observing the 3D-ICML structure in Fig. 2, we note that any two adjacent memory cells at the same x-y location are connected back to back. Pt electrodes are connected to either WLs along the x-axis or BLs along y-axis. We introduce a new set of interconnects called control lines (CLs), which connect to Cu electrodes of ReRAM cells. CLs are along the direction diagonal to x-axis and y-axis.

In this design, memory devices and metal wires form a memory island without isolation layers. Each set of metal in-

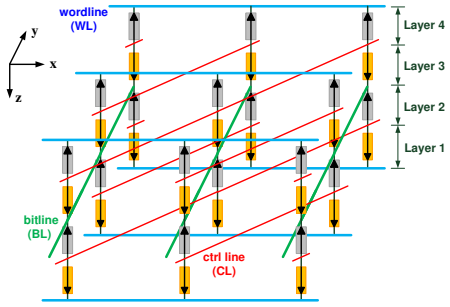

Fig. 2. The proposed 3D-ICML design.

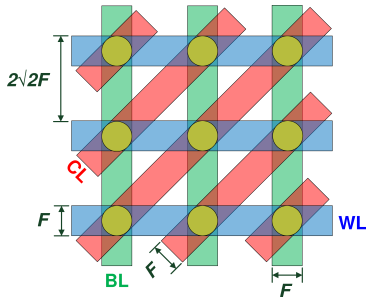

Fig. 3. Layout of 3D-ICML design.

terconnects, including WLs, BLs, and CLs control the memory cells on both upward and downward layers. The capacity of a 3D-ICML memory island is determined by both the dimension of the crossbar array in each layer and the total layer number (H). Assuming the crossbar array has N rows and N columns, memory capacity (MC) can be expressed as

$$MC = N^2 \cdot H \tag{1}$$

In this paper, we call the memory cells connected to a given WL_i as WL_i group memory cells (WL_iGC). Similarly, the memory cells are connected to a given BL_j as BL_j group cell (BL_jGC). WL_iGC and BL_jGC could share the same set of CLs in read/write operations, which will be explained in Section III-C and Section III-D, respectively.

B. 3D Memory Density

Fig. 3 illustrates the layout of 3D-ICML from a top view. To minimize the required space between adjacent CLs, the smallest cell area that can be achieved is $A_{3D-ICML} = [(2\sqrt{2})F]^2 = 8F^2$, which doubles the cell size of the conventional crossbar array $A_{conv} = 4F^2$. However, the density of a 3D memory is determined by not only single memory cell area but also the allowable number of memory layers. By sharing Pt and Cu with neighbor layers, 3D-ICML can reduce the number of conduction layers and remove isolation layers. Therefore, more crossbar arrays can be stacked up vertically for a given height of a 3D structure, which usually is a limitation during fabrication process.

Table II lists the key process parameters of Cu-$Ge_{0.3}Se_{0.7}$-SiO_2-Pt and SOG. In the conventional 3D ReRAM structure a layer of memory array is constructed by one memory device and a SOG layer. The total thickness is approximately 178 nm. The memory layer in 3D-ICML has a thickness of only 78 nm.

We can define the memory density $D = 1/(A \cdot T)$, where, A and T represent a single memory cell area and memory layer thickness, respectively. Accordingly, we have $D_{3D-conv} = 1/(4F^2 \cdot 178nm)$, and $D_{3D-ICML} = 1/(8F^2 \cdot 78nm)$. 3D-ICML can increase memory density by 13.4% even it has a bigger memory cell.

TABLE II
Cu-$Ge_{0.3}Se_{0.7}$-SiO_2-Pt & SOG Process Parameters [6][7]

Material	Thickness (nm)	Material	Thickness (nm)
Cu	70	Pt	30
$Ge_{0.3}Se_{0.7}$	25	SOG	50
SiO_2	3		

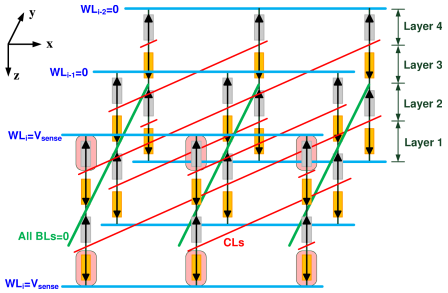

Fig. 4. An example of WL_iGC in read operation.

C. Read Operation

Fig. 4 shows an example of WL_iGC cells in read operation. The target WL_i is raised to V_{sense}. All the other WLs and all the CLs are tied to '0'. The stored data can be detected by measuring the currents through the CLs corresponding to the target memory cells in WL_iGC. To prevent disturbance from the cells on BLs, all the BLs are forced to '0'. Note that the memory cells in WL groups and BL groups have to be accessed separately. Similarly, the read operation of BL_jGC cells on x-y plane can be accessed simultaneously (which is omitted here due to space restriction). For a 3D-ICML memory island with capacity $MC = N^2 \cdot H$, the read bandwidth is $N \cdot H/2$.

The power consumption of a read operation is determined by memory resistance states. The worst or best case happens when all the memory cells are at LRS or HRS, respectively. Theoretically, the boundary conditions of the read power consumption P_{RD} can be represented as

$$\frac{(V_{sense})^2}{R_H} \cdot N \cdot H/2 \leq P_{RD} \leq \frac{(V_{sense})^2}{R_L} \cdot N \cdot H/2 \tag{2}$$

D. Write Operation

As is the same with all bipolar ReRAM crossbar designs, SET and RESET in 3D-ICML have to be separated because the opposite driving polarities are required. Fig. 5 illustrates an example of WL_iGC cells in a SET procedure. Every time, only those memory cells at the same x-y location can be programmed simultaneously. WL_iGC cells have to be written sequentially along x-axis. Similar to read operations, the memory cells in WL groups and BL groups should be programmed separately. The write operation of BL_jGC cells can be executed along y-axis. For a 3D-ICML memory island with capacity $MC = N^2 \cdot H$, the average write bandwidth is $H/4$.

The driving conditions need to be carefully controlled to avoid unnecessary overwriting caused by sneak paths and to minimize the total write current. For instance, to SET some memory cells in WL_iGC, $-V_{\text{SET}}/2$ and $V_{\text{SET}}/2$ are applied to WL_i and the corresponding CL, respectively. Those unselected WLs, BLs, and CLs are tied to '0'. The detailed driving conditions are summarized in TABLE III.

In 3D ReRAM design, power consumption in writing operations usually is a critical factor in limiting the memory island size. For a 3D-ICML memory island with $MC = N^2 \cdot H$,

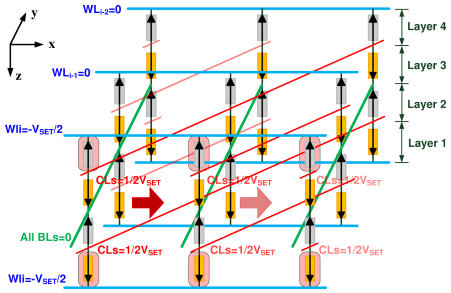

Fig. 5. An example of WL$_i$GC in SET procedure.

the peak write current $I_{WR,max}$ can be obtained when all the memory cells are at LRS and all the H cells in the group are programmed:

$$I_{WR,max} = \frac{|V_P|}{R_L} \cdot \frac{H}{2} + \frac{|V_P|}{2R_L} \cdot (3N-2) \cdot \frac{H}{2} \qquad (3)$$

Here, V_P could be V_{SET} or V_{RESET}. The first term on the right of (3) represents the overall write currents, and the second term is the sum of leakage currents through the unselected cells. Therefore, the effective write factor η_{p} can be expressed as

$$\eta_p = \frac{\frac{|V_P|}{R_L} \cdot \frac{H}{2}}{\frac{|V_P|}{R_L} \cdot \frac{H}{2} + \frac{|V_P|}{2R_L} \cdot (3N-2) \cdot \frac{H}{2}} = \frac{2}{3N} \qquad (4)$$

Equation (4) shows that η_{p} is independent of H but decreases as increasing N. Hence, the effective programming current is dominated only by H. In another words, increasing 3D layer number H is an attractive way to improve programming power efficiency.

IV. Discussion And Future Work

Previously we treat each memory element in 3D-ICML independent of all the others to obtain high memory density. Another possible utilization of the 3D-ICML is writing the complementary data into a pair of memory cells connected back to back. In this way, the capacity of the memory island is reduced by half. However, we could trade-off capacity with higher sense margins in read operations, and hence, increase memory island size.

3D-ICML requires relative alignment only between the adjacent layers because there is no direct path from the cells on the lowest layer to those on the highest layer. In other words, alignment mismatch does not accumulate when stacking up memory layers. The impact of crosstalk is not severe either due to the interleaved structure. However, the sneak path through the cells on the adjacent layer could limit the size of crossbar array on a single memory layer, though the overall capacity of the whole memory island is expected to improved. Moreover, the diagonal CLs can increase the complexity of peripheral circuitry. We plan to address these issues in the future. Also, we will investigate the implementation and explore design implication of 3D-ICML, including performance, power consumption, and architecture-level support.

TABLE III
Driving Conditions in Writing Operations.

Data	Cell Group	Driving Condition
LRS	WL$_i$GC	WL:$-V_{\mathrm{SET}}/2$, CL:$V_{\mathrm{SET}}/2$
LRS	BL$_j$GC	BL:$-V_{\mathrm{SET}}/2$, CL:$V_{\mathrm{SET}}/2$
HRS	WL$_i$GC	WL:$-V_{\mathrm{RESET}}/2$, CL:$V_{\mathrm{RESET}}/2$
HRS	BL$_j$GC	BL:$-V_{\mathrm{RESET}}/2$, CL:$V_{\mathrm{RESET}}/2$

V. Conclusion

In this paper, we propose a new 3D structure for bipolar ReRAM design with interleaved complementary memory layers called 3D-ICML. The advantages of high density, high access bandwidth, and lower process complexity and cost provides the potentials in wide applications.

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