

Two Methods for 24 Gbps Test Signal Synthesis

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Abstract— This paper describes and compares two methods for producing digital test signals up to 24 Gbps. Prototypes are experimentally characterized to determine signal quality, and the two methods are demonstrated and compared. The residual timing errors are dominated by jitter. Typical random jitter (RJ) is about 1.17ps to 1.4ps (RMS) including system measurement errors for the two methods. Deterministic Jitter (DJ) is between 2.4ps and 8.5ps. Total jitter (TJ) ranges between 18.9ps and 28.2ps at a bit-error-rate $BER=10^{-12}$.

Keywords—multi-Gbps; Test Synthesis; Jitter; ATE

I. INTRODUCTION

Automated testing above 10 Gbps presents formidable technical and economic challenges. While laboratory-grade instruments exist that can produce high-quality digital test patterns up to and beyond even 40 Gbps, these instruments are generally too expensive or otherwise not suitable for high-volume production testing of complex devices (with perhaps >100 high-speed signals). As the signal rate exceeds 10 Gbps, the timing requirements (resolution and accuracy) become severe. Jitter tolerance is measured in picoseconds, or even ~100 femtoseconds (for RMS random-jitter). Achieving and maintaining such performance levels across many parallel channels in a realistic ATE environment would be extremely expensive using conventional instruments. Yet, it is just at these frequencies where the need for precision is the greatest. On the other hand, the relentless pressure to lower component cost may preclude the traditional instrument-based approach. Some relief from this dilemma is obtained through the application of design-for-test (DFT) and built-in self-test (BIST) techniques. For example, DFT can be used to re-partition a complex device so that simpler tests can be applied to sub-sections at a lower overall cost. However, eventually the entire device must be demonstrated (usually at the full operating frequency). Effects such as internal crosstalk, and reflected-power induced noise at the DUT I/O are not usually fully-exercised when the device is partitioned. These same effects are also difficult to model, so total reliance upon simulations can be risky. Using BIST, a high-speed device can be used to synthesize its own test stimuli and then compare its own output response to an ideal pattern (or a synthesized pattern). For high-speed serial I/O the device outputs are “looped back” to the inputs, either on-chip or off-chip. Therefore, both DFT and BIST can be used to improve testability and allow at-speed tests for multi-GHz devices.

However, even after these tests are performed, there remains some uncertainty regarding their completeness. Since

most DFT/BIST put the circuit into a different configuration than is actually used in the end application, it is not guaranteed that passing self-tests, even “at-speed,” will ensure performance under normal operating conditions.

Therefore, while DFT and BIST are useful (usually *necessary*) test enhancements, there still remains a need to operate the DUT in full-functional, full-speed mode. Certainly during first-silicon debug this is required. Normally this would lead us back to the use of ATE, which is traditionally designed to do just that. However, the economic realities of today’s ATE industry force a relatively few number of suppliers to address the “mainstream” of the marketplace, which calls for testing most applications well-below 10 Gbps (in fact, most are below 1 Gbps). The very few ATE options that address the >10Gbps band are offered at price levels that are “competitive with” (but not dramatically *lower* than) instrument-based test solution.

Aside from traditional, instrument-based solutions, or expensive ATE-options, two general strategies have emerged, as illustrated in **Fig.1**. One involves addition of customized

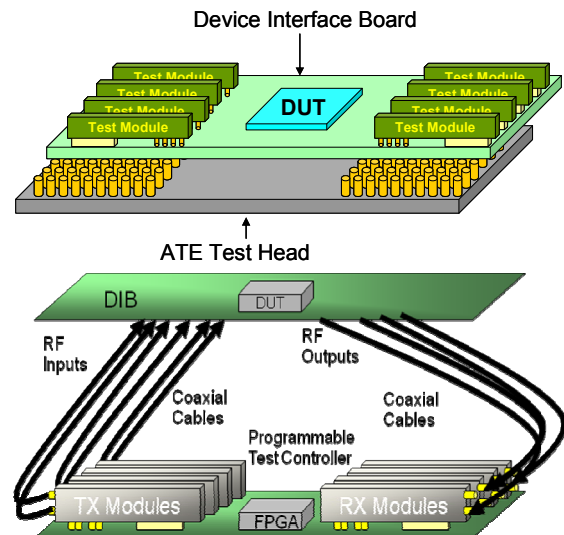


Fig.1 – (Top) Modules used in an ATE enhanced loadboard arrangement. (Bottom) Modules used in a customized, FPGA-based test system.

electronic circuits to the DUT-ATE interface (load-board) in order to obtain advanced test functionality. A common application uses multiplexers/serializers to produce higher-speed data for inputs and deserializer for slowing the DUT output rates down to that of the ATE. The second approach uses specialized electronic “modules” configured to form what

amounts to a “custom” ATE. Both methods have found some degree of success at providing economic test solutions above 10 Gbps.

II. TWO APPROACHES FOR 24 GBPS SIGNAL SYNTHESIS

The first approach uses two SiGe 16:1 serializers to produce two independent 12 Gbps data streams (see **Fig.2**). Since the two serializers are identical, only one is shown in the figure. These are combined using a double-date-rate (DDR) logic design technique by an Indium-Phosphide (InP) exclusive-OR gate. The 750 Mbps x16 parallel data for the serializers are provided either from an ATE system or from a field-programmable gate array (FPGA). The serializer uses an on-chip PLL and VCO to generate a full-rate (12 GHz) low-jitter reference clock for clocking the output data at high-speed. An important advantage of this approach is that the random-jitter (RJ) of the 12 Gbps data signal is primarily determined by this low-jitter clock. It is only indirectly coupled to the slower (750 MHz) reference clock. Therefore the slower clock jitter is “filtered” by the on-chip PLL/VCO. Experimentally, we have verified that the 12 GHz clock has about 1.1ps or less RMS jitter.

The output of the each serializer is passed through a 1:4 fanout buffer to produce 4 identical copies of the 12 Gbps signals. One is used as the “primary” signal, passing through a 2:1 select multiplexer, an adjustable-amplitude differential buffer, and a high-performance DPDT RF relay. The relay provides an alternate direct connection to ATE signals (for lower-speed tests, DC measurements, and calibration). This primary path provides the main connect for testing DUT inputs up to 12 Gps. One of the other fanout copies of the 12 Gbps signal connects to a high-speed InP exclusive-OR gate. The second input to the XOR comes from an adjacent (identical) 12 Gbps serializer module. Another fanout signal is available for calibration purposes.

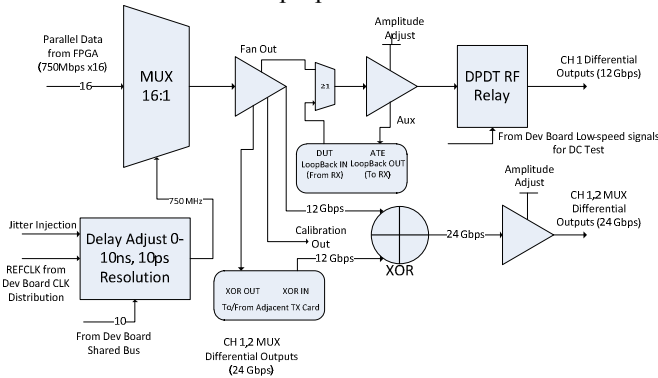


Fig.2 – XOR-multiplexing two 12 Gbps signals for synthesizing 24 Gbps signals. One of the two identical 12 Gbps transmitters is shown.

We have utilized this basic XOR technique at lower rates (<10 Gbps) to obtain the desired data-rate doubling effect, and have even demonstrated prototypes that doubled two 10 Gbps signals to produce a 20 Gbps test signal. In the present work, we extend this to even higher speeds (now up to 24 Gbps) with reduced jitter. The extended support logic provides several alternative signal paths, some of which are available for

calibration purposes, and are optimized for the XOR-multiplexing function. Another new feature is the incorporation of a high-performance “RF” relay in the primary signal path. This is used to selectively connect the DUT inputs to either (a) the serializer output, or (b) direct connects to ATE channels. The serializer output is used for 12 Gbps testing, while the direct ATE connections can be used for standard test functions (functional tests below 10 Gbps, characterization tests, debug, calibration, and DC tests).

Each 12 Gbps TX module includes a very-high performance InP XOR gate, that combines that module’s “Alternate” output with that of an adjacent module. Since each module has an integrated delay-adjustment element in its reference clock path, we can program a desired phase difference between the two channels. This difference is nominally one bit-period (1 UI), i.e. 41.67ps at 24 Gbps. By using a very high-performance InP XOR, unwanted jitter effects can be minimized. The specific device used in the prototype has typical RJ<500fs and DJ<2ps. These tight specifications are critical for obtaining the precise output desired.

In the second approach, a newly-introduced InP 4:1 multiplexer/serializer is used to combine four 6 Gbps signals into a single 24 Gbps channel (see **Fig.3**). The 4:1 MUX uses both rising and falling edges of a half-rate (12 GHz) clock input to define the timing of the serial output signal. Partially due to its simple logic structure the output signal quality is improved (see Section 3). However this device does NOT include an internal PLL/VCO, so the input reference clock directly controls timing of the output transitions, without jitter-filtering.

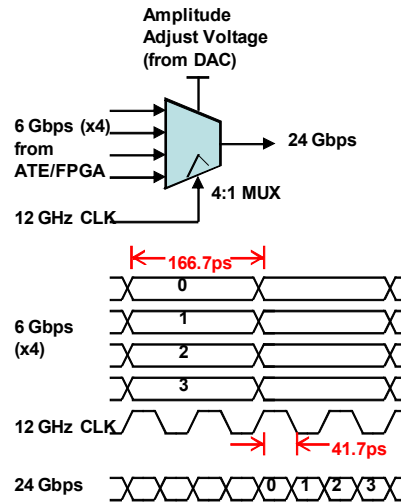


Fig.3 – Second approach for synthesizing 24 Gbps signals, using a 4-to-1 multiplexer and a 12 GHz reference clock.

Another disadvantage of this new approach is its need for high-speed (6 Gbps x4) input data. Unlike the first method that used 750 Mbps data which is readily available from traditional ATE or advanced FPGAs, the need for 6 Gbps pushes the limits of both sources. For the present demonstration, we utilize four of the 12 Gbps channels described in the first method, running at 1/2-rate.

III. MEASUREMENT RESULTS

A. Method 1 – XOR Multiplexing without reclocking

The first method requires two 12 Gbps signals to be combined by an InP XOR gate. Since no further reclocking of the combined signals follows the XOR, the method requires very precise timing of both 12 Gbps signals. An example of one of these is shown in **Fig.4**. Total measured jitter is 20.9ps (for 10^{-4} BER, i.e. 10kHits). This leaves 62.4ps of valid data, or about 0.75UI. In this example, the output amplitude is set at full-scale (about 500mV). The signal is differential, so the effective differential swing is about 1V.

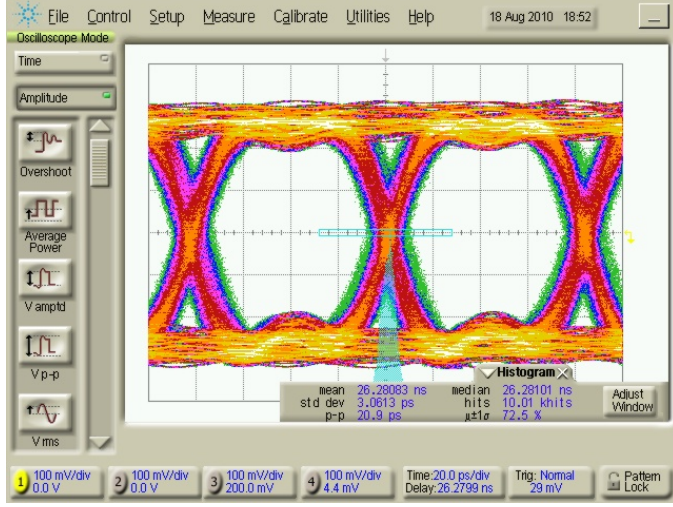


Fig.4 – 12 Gbps data eye from a 16:1 SiGe serializer. Time-base is 20ps/div.

The relative phase of the two 12 Gbps signals is adjusted by programming the delay stage of the reference clocks for the two modules. The amount of phase offset corresponds to one bit period (one U.I.) of the desired output pattern (41.67ps at 24 Gbps). This causes input transitions to the XOR gate to alternate between the two channels, so that only one transition occurs every 41.67ps. If the 12 Gbps signals are encoded properly, then the XOR gate performs real-time decoding to obtain the desired output pattern stream. This encoding scheme has been described in earlier works.

After combining the two 12 Gbps signals in the XOR gate, the resulting signal shows open “eyes” with about 18.9ps (0.45UI.) total jitter (p-p), including RJ=1.4ps (RMS) and DJ=8.5ps (see **Fig.5**). Extrapolating to $BER=10^{-12}$ predicts TJ=28.2ps (0.67UI.). Therefore the first method yields a usable data eye opening of 0.33UI. at $BER=10^{-12}$ including the timing errors of the measurement system (dominated by trigger signal jitter).

The measured total jitter has been separated into its random and deterministic contributions by applying two test patterns. As shown in **Fig.5**, we first measure TJ while applying a PRBS pattern (2^8-1). Next we set the pattern to be a repeating “010101...” sequence (a “clock” pattern) to suppress data-dependent deterministic jitter. The standard deviation of the

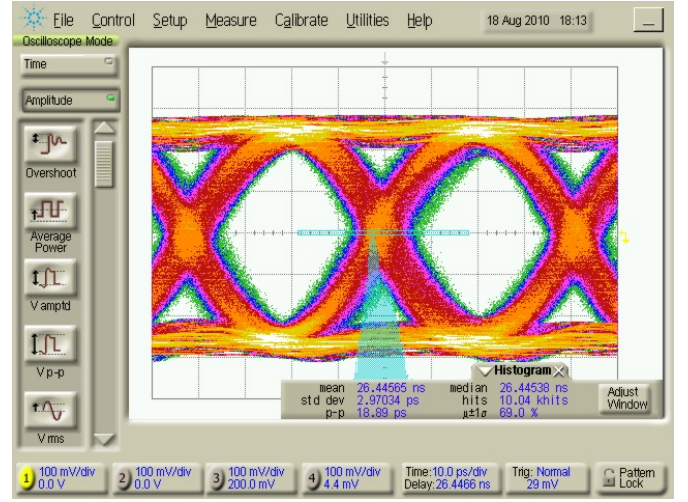


Fig.5 – Full-swing 24 Gbps data eye from the InP XOR output. Time-base is 10ps/div. (Note change in scale).

jitter distribution in the second test gives a close estimate of the random jitter (RJ), which was found to be about 1.4ps in this case. Then we can apply a well-known formula that relates TJ to RJ and DJ:

$$TJ = \alpha * RJ + DJ, \quad (1)$$

where α is determined by the BER of the measurement. For the “10kHits” histograms shown, the effective BER is 10^{-4} and $\alpha=7.438$. BER and α are related through the “complementary error function”. Data dependent jitter, DJ, is found according to:

$$DJ = TJ - (7.438) * RJ \quad (\text{for } BER=10^{-4}). \quad (2)$$

So, in this case, we have:

$$DJ = 18.9ps - (7.438) * (1.4ps) = 8.49ps. \quad (3)$$

At $BER=10^{-12}$ $\alpha=14.069$, so we can estimate total jitter at this lower BER according to:

$$TJ = 14.069 * RJ + DJ \quad (\text{for } BER=10^{-12}) \quad (4)$$

So, for this measurement:

$$TJ \text{ (at } BER=10^{-12}) = 28.2ps (=0.67UI \text{ at } 24 \text{ Gbps}). \quad (5)$$

In order to accurately combine two signals from the two 12 Gbps modules using an InP XOR gate, we must also be able to control the relative timing (skew) to within a picosecond (or less). This is accomplished using variable/programmable delay elements in the reference clock paths. The delay chips used here have roughly 10ps digital resolution, spanning a 10ns range (10-bit binary coding). Additionally, an analog vernier, controlled by a DAC is used for fine adjustment of delay throughout a 40ps range. Examples of adjusting the delay in 2ps increments are shown in **Fig.6**. The desired accuracy (about $\pm 200fs$) is shown at about the limit of the oscilloscope resolution. Note that the time-base is only 2ps/div.

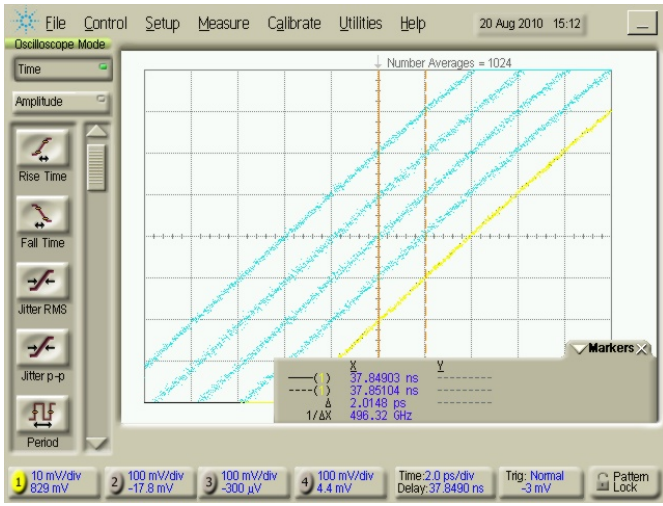


Fig.6 – Demonstration of high-accuracy phase-adjustment (2ps steps ± 0.2 ps). Time-base is 2ps/div.

B. Method 2 – 4-to-1 Multiplexing with re-clocking

The second method uses an InP multiplexer to synthesis 24 Gbps test patterns. This recently-introduced device is intended for applications running up to 28 Gbps, and is “typically” able to operate as high as 30 Gbps. Typical RMS random jitter is specified as RJ=500fs, and DJ=4ps.

There are several critical parameters necessary for 24 Gbps operation. Four 6 Gbps data signals must be aligned to provide an overlap of valid data timing windows. These signals could be provided by advanced ATE or directly from advanced FPGAs. For the present demonstration we utilize four of our 12 Gbps channels, each operating at $\frac{1}{2}$ -rate to produce the parallel data bus.

The most critical, input signal is the half-rate (12 GHz) reference clock. We utilized an optional “full”-rate clock output from one of the 12 Gbps modules. An on-chip PLL and VCO in the SiGe 16:1 serializer locks to a slower reference clock to produce a very low-jitter (~ 1 ps RMS) full-rate output clock. It is inherently phase-locked with the 6 Gbps data signals (necessary for this application).

The resulting multiplexer output (at 24 Gbps, with full-amplitude swing) is shown in **Fig.7**. It exhibits about RJ=1.167ps, DJ=2.44ps, and TJ=11.11ps (0.26U.I.) for 10kHits, leaving a 0.73U.I. eye-opening. The total measured jitter (11.11ps) was separated into the RJ and DJ components using the two-step approach described in Section 3.1. Extrapolating to $\text{BER}=10^{-12}$ yields a usable data-eye opening of about 0.54U.I. (~ 22.5 ps). This value includes the effects (total jitter) of the measurement system.

For direct comparison to the first method (Fig.5), **Fig.8** shows the 4:1 multiplexer output at 24 Gbps on a 10ps/div scale. The signal quality is noticeably improved. Specifically, the reduced DJ for the second method results in a wider data eye opening, and overall reduced jitter and voltage noise. The 4:1 MUX exhibits TJ=11.11ps (**Fig.7**) as compared to 18.89ps for the XOR approach (**Fig.5**). The difference of 7.78ps is mostly due to deterministic jitter (DJ), although the second method has slightly less random jitter as well.

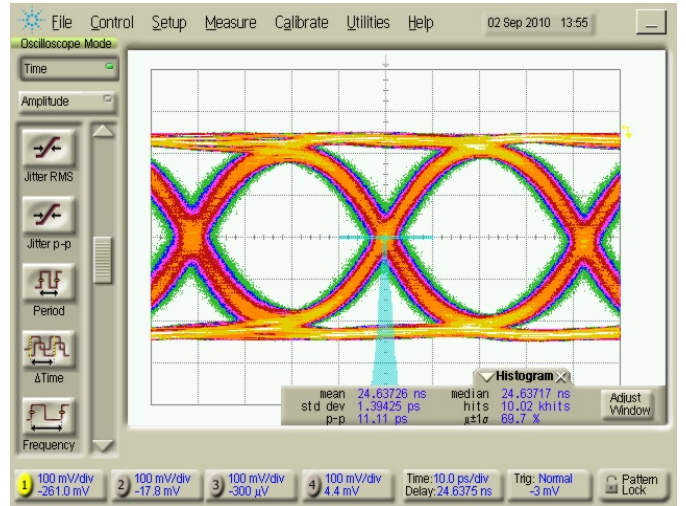


Fig.7 – Full-swing (~ 500 mV), 24 Gbps 4:1 multiplexer data eye. RJ=1.167ps, DJ=2.44ps. TJ=11.11ps at $\text{BER}=10^{-4}$. Time-base is 10ps/div.

To demonstrate amplitude adjustability, **Fig.9** shows the minimum signal swings of 50mV. This value is the single-ended amplitude for one side of the differential signal. Therefore the effective differential swings are 100mV.

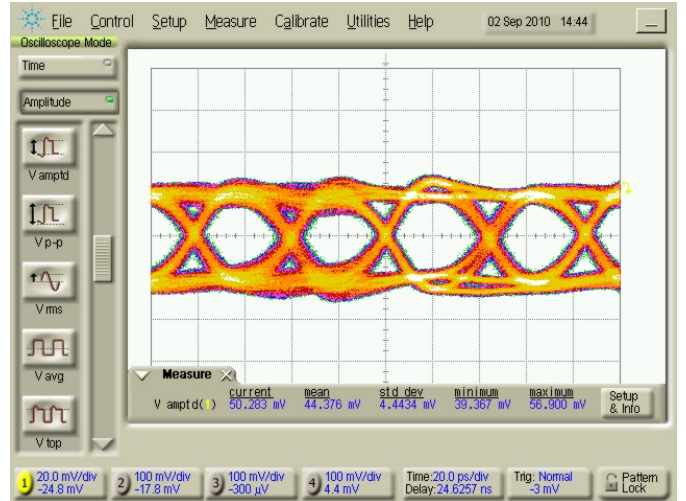


Fig.8 – Small-swing (50mV), 24 Gbps 4:1 multiplexer data eye. Time-base is 20ps/div. Vertical scale is 20mV/div. (Note the change in vertical scale).

IV. CONCLUSIONS

The two methods described in this paper provide the ability to synthesize 24 Gbps test signals. For “short” functional test patterns (i.e. on the order of 10^4 bits), data eyes are obtained with $>73\%$ UI available openings. When extrapolated to $\text{BER}=10^{-12}$ the eye openings are expected to be about 33% UI and 54% for the two methods respectively. The second method produces better-quality signals, at the expense of requiring higher-speed input signals (6 Gbps x4 data, and low-jitter 12 GHz clock).