Circuit and DFT Techniques for Robust and Low Cost Qualification of a Mixed-signal SoC with Integrated Power Management System

Lakshmanan Balasubramanian, Member IEEE, MIET, Puneet Sabbarwal, Rajesh Kumar Mittal, Prakash Narayanan, Ranjit Kumar Dash, Anand Devendra Kudari, Srikanth Manian, Sudhir Polarouthu, Harikrishna Parthasarathy, Ravi C Vijayaraghavan, Sachin Turkewadikar.
Texas Instruments India Private Limited, Bangalore, India.
E-mail: lakshmanan@ti.com

Abstract: **This paper discusses some specific circuit, and analog DFT techniques and methodologies used in integrated power management (PM) systems to overcome challenges of mixed-signal SoC qualification. They are mainly targeted at achieving the following: 1. Enabling the robust digital and system level test and burn-in (BI) with external supplies by disabling the on-chip PM with robust power-on performance, 2. Minimising external on-board active components in BI board and making the whole BI process more robust, 3. Making the I_{DDQ} tests more robust, increasing the I_{DDQ} sensitivity by less error prone design methods and enabling I_{DDQ} tests possible on analog supplies, and 4. Defining separate BI strategy for the whole PM modules on-chip and enabling it by targeted analog test modes.**

Keywords: Burn-in, electrical reliability qualification, I_{DDQ}, analog DFT, power management.

I. INTRODUCTION

Current practices of SoC qualification involve scan and I_{DDQ} tests, and reliability qualification based on burn-in (BI) and high temperature operating life (HTOL), electro static discharge ESD compliance, package pin continuity, package thermal and humidity qualification. These are amongst the basic functional and performance compliance tests. Most of these need the device or chip to be under a specific state to enable required testing and to achieve targeted coverage. There is also a need for parts of internal circuits like the on-chip power supplies and most other analog functions to be turned-off to enable digital scan, I_{DDQ} and BI tests. In addition to the above mentioned varying requirements there is also a strong need to minimise the test cost by enabling the use of simple low cost test equipment with limited resources [1], and minimise the support logistics like the development of number of different test boards. With more analog and PM functionality getting integrated in the SoC, achieving all the requirements mentioned above gets more difficult. While digital DFT techniques to achieve most goals mentioned above are mature, well understood and applied thoroughly, the analog and PM parts of the design limit some of the qualification processes mentioned above and making it costlier and time consuming. This paper discusses specific circuit and analog DFT techniques used in mixed-signal SoC targeted at achieving the following:

978-3-9810801-7-9/DATE11/©2011 EDAA

1. Robust power-on functionality.
2. Robust and low cost BI process.
3. Robust, highly sensitive I_{DDQ} testing with higher defect coverage.
4. Targeted BI strategy for PM and analog contents.

Since there are different distinct requirements being discussed, the paper is organised to discuss each key requirement in a separate sub-section under section II. In each sub-section there is a brief introduction and problem statement followed by a discussion on the corresponding proposed solutions. Section III discusses some key results with a concluding summary in Section IV.

II. CIRCUIT AND DFT TECHNIQUES ENABLING SIMPLER QUALIFICATION

A. *Robust Power-on Functionality*

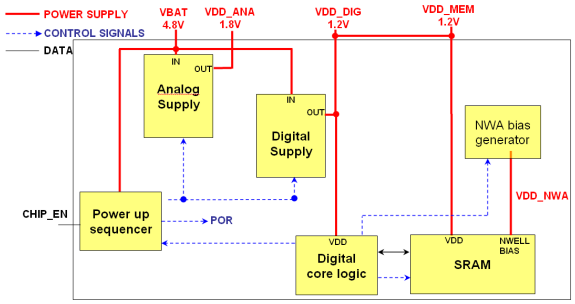

Figure 1. Typical integrated power management system

There is a strong need to integrate on-chip the PM functionalities like the reference voltage and current generators, voltage regulators and the power-on sequencing / reset generator, driven by the need to lower the cost and maximise the platform flexibility of the solutions. The block diagram of a typical PM system is shown in Figure 1. Such a complete integration of PM results in the power-up time of the chip getting longer and complex due to the necessary settling times of the components and finally the power-on reset (POR) de-assertion causing increase in overall test time. There is a definite need to vary the voltage levels of power supplies to

extreme limits beyond the functional requirements for full product timing, functional and reliability qualification. Supporting these requirements on-chip will result in sub-optimal implementation due to severe trade-offs between area, quiescent power consumption, and performance requirements like the transient load regulation and noise [2-3]. Further all the PM circuits need to be designed to meet the extreme input power supply voltage, timing, and temperature requirements to have a robust power-up under all SoC level scan, I_{DDQ} and BI test conditions.

The above bottlenecks are overcome by introducing a shorter power-up mode in which the internal power supplies are disabled and bypassed with application of external power supplies to achieve the following: *a) Fast power-up resulting in lowering of test time and cost, and b) Optimal design of on-chip PM to reduce overall solution cost by dissociating the need for supporting extreme conditions from the on-chip solution*. To enable this functionality there is a need for identification of the test mode. This can be achieved by providing an additional package pin for proper mode identification which results in compromising the functional platform simplicity and package cost.

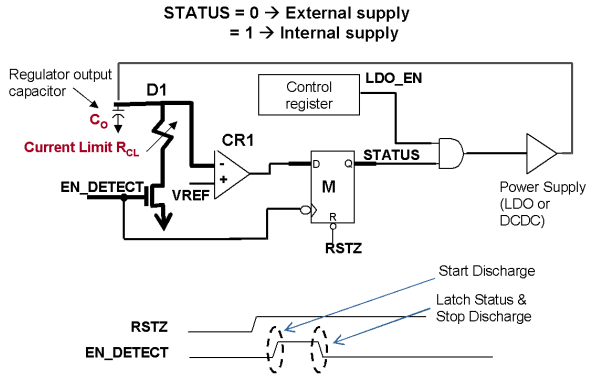

Figure 2. Test mode detection scheme enabled by the timer (T), discharge circuit (D1), a comparator and a reference VREF (CR1)

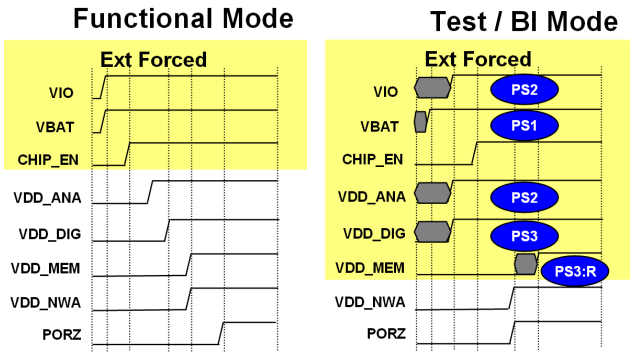

Figure 3. Functional and Test mode power-up timing waveforms

The test mode identification is needed only during the device qualification phase without impacting the actual field application. The digital and SRAM supplies are usually supplied by on-chip components during all functional modes and will be forced from external sources only for the test mode. Hence detection of the floating condition of the VDD_DIG node as shown in Figure 2 is used, with a necessary controlled discharge mechanism to meet the minimum power-up time constraint, for test mode detection. Test mode is implied by external application of VDD_DIG and the detection status is used to disable the on-chip power supply. A time T is used to de-assert EN_DETECT after a predetermined period of discharge based on chosen values of R_{CL}, C_O. The on-chip power supply is enabled in functional mode only after ($\sim R_{CL}.C_O$) the detection sequence is complete and if VDD_DIG is not forced from an external source. This scheme is designed to have power-up sequence for the functional and test modes respectively as shown in Figure 3. The annotations PS1, PS2 & PS3 indicate to which BI power supplies the respective power lines are tied to. PS3:R is a power supply derived on board from PS3 by using a delayed power switch or relay in the path between them. The signal named PORZ is the inverted version of POR with a passive pull-down to keep it always defined including under the system shutdown state.

Even though the on-chip power supplies are disabled during test mode power-up as discussed above, there is still a need for designing the POR controller to meet all the digital and SoC level scan, I_{DDQ} and BI test conditions. Even in an otherwise simpler open-loop configuration there are strong trade-offs in power and area to achieve robustness for BI operation, especially the circuits for delay generation and compensation.

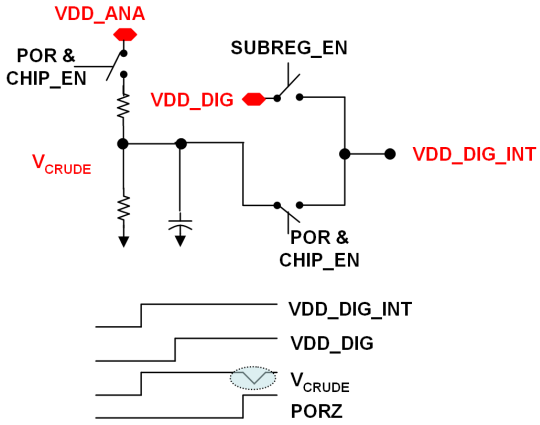

Figure 4. Internal crude power supply with a sub-regulation feature

Minimal area and power can be achieved by making most part of the circuit operate at the lowest possible voltage domain supported by an internal power supply powered by other higher level voltage domains. The internal supply can be as simple as a resistive divider with an output capacitor just to support the transients of the power-on circuit during power-up operation. The area of such a circuit can be kept to a minimum by allowing the power consumption to be as high as possible and the impedance as low as possible. The overall power consumption of the solution can be kept to a minimum by sub-regulating this internal supply with another more efficient power supply available in the system, say VDD_DIG, after the system power-up as shown in Figure 4. The hand-off between the internal supply (V_{CRUDE}) and the VDD_DIG has to be soft with a reasonable overlap time between the sub-regulation enable signal (SUBREG_EN) and the de-assertion of POR to

avoid functional failure as depicted by a dip in V_{CRUDE} in Figure 4.

B. *Robust and Low-cost BI Process*

BI and HTOL qualification of the product usually requires the chip to operate under a certain functional state, with temperature and power supply voltage conditions that are much higher than the system functional requirements to accelerate the stress effects and target the product life-time qualification in a relatively much shorter period. The requirements of power-up are met by the techniques discussed above in Section II A.

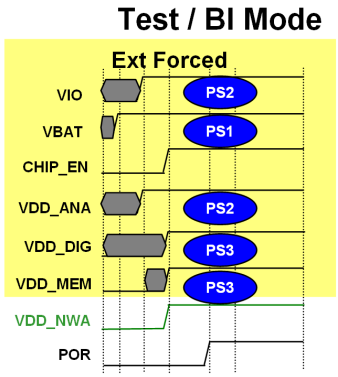

Figure 5. VDD_NWA requirement to enable simultaneous application of VDD_DIG & VDD_MEM during test mode / BI power-up.

There are additional system level constraints that must be addressed to make the whole test and BI process more robust and low cost. For instance, in all the UDSM technologies (<100 nm) there is a need for the embedded, integrated on-chip memory core to have a dedicated substrate/N-well bias (VDD_NWA) to reduce leakage power consumption. For reliability and latch-up requirements VDD_NWA must be applied before the respective power supply (VDD_MEM) to the memory cell can be applied. Such requirements, while are normally taken care of under the functional scenario by the power-up sequencing circuit as shown in Figure 1, pose a cost overhead due to additional external power supplies required under normal test and BI conditions. This problem has been overcome with an implementation, the details which are obvious and hence not dealt with explicitly in this paper for brevity reasons, to meet the requirements shown in Figure 5 to enable a low cost, robust BI by minimising external relay components in the BI board.

C. *Robust, Sensitive I_{DDQ} Testing with Additional Coverage:*

I_{DDQ} tests are usually targeted at finding structural, electrical faults which cause higher than defined power supply currents which are measured at pre-defined static states of the device. When more analog, PM, and I/O functionality is integrated into the system, the sensitivity of I_{DDQ} tests decreases which is causing difficulty in setting right I_{DDQ} screening threshold. Conventionally, such I_{DDQ} measurements are done only for digital logic and memory supplies [4]. This section will enumerate the design, SoC integration and verification methodologies that enable error free integration and robust I_{DDQ} testing. Various issues have been encountered during traditional digital test that are caused by incorrect integration of analog and mixed-signal (AMS) contents in the SoC.

Analog multiplexers using pass transistors used for analog testability should be operated with great care to avoid shorting of unrelated electrical nodes. With integrating AMS contents scan chains must be controlled carefully to avoid functionally unsupported analog conditions to happen during scan chain shifting which may cause a high current scenario. Such issues result in ineffective I_{DDQ} screening as illustrated in Figure 6 which shows the unintended current paths annotated as I1, I2, I3 and I4. I1 is caused by simultaneous logic '0' on gates of M1 and M2; I2 by simultaneous logic '0' on gate of M1 and '1' on gate of M3; I3 and I4 caused when VDDA is not available.

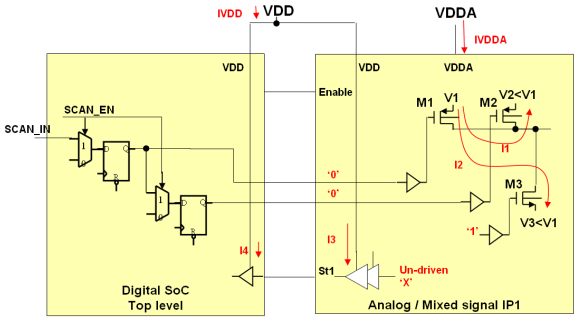

Figure 6. Scan pattern dependent I_{DDQ} current paths.

Following is the summary of such a pattern dependent high current scenario found during I_{DDQ} testing of a UDSM design: 0.22mA of I_{DDQ} with analog power down and 1.26mA under certain patterns found to be due to shorting of analog nodes. Shorting of different nodes or outputs of different analog IPs during ATPG pattern shift can cause a serious reliability concern for device under test, resulting in high yield fallout for the device post BI, though may not interfere with functional mode of operation.

These issues are not caught by system level digital simulations because of inadequacy/inaccuracy of analog models and model validation. Existing verification methodologies like force-sense, only verify the partial signal connectivity. Using AMS co-simulation at SoC level is costly and time consuming.

1) *DFT & Methodology Guidelines for I_{DDQ}*

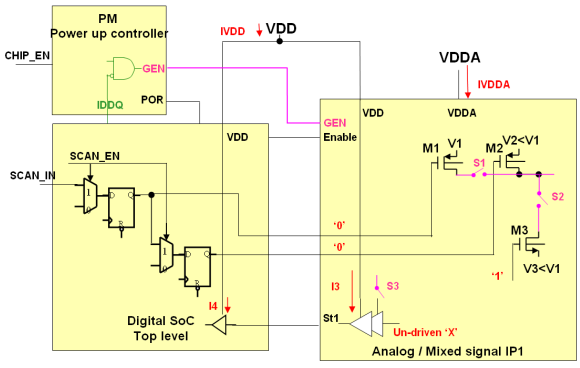

Figure 7. GEN based I_{DDQ} mode gating.

All or identified critical input signals coming from digital logic to analog modules are gated to reset value during scan test mode to avoid issues discussed above. But there can be many signals that need gating resulting in increased area and coverage loss. This process could be error-prone due to the manual effort in identifying critical signals. Such a gating can be done either at the SoC top level or at every analog IP / module level. The SoC level I_{DDQ} gating itself can be done by embedding the functionality of the I_{DDQ} gating with the POR equivalent signal referred to GEN that defines both the POR status and the I_{DDQ} mode indication as shown in Figure 7. GEN signal is usually available in most systems to isolate unintended analog current paths during system shutdown condition.

Defining the I_{DDQ} target, verifying it against SPICE simulations are greatly recommended. The gating implemented at each module level and the GEN based methodology discussed above enable the verification, isolation and validation of the module level I_{DDQ} targets, and seamless SoC integration. In addition, the power supply of the analog circuits can also be gated where possible and necessary. All test mode functionalities are modelled in the analog behavioural model, and validated against module level SPICE simulations [5]. Assertions are embedded in the model to detect unsupported conditions and check power-up default conditions. Such behavioral models of all analog modules greatly help perform test mode simulations at SoC level with insignificant simulation overhead.

D. Targeted PM BI Strategy:

The accelerated stress based qualification (BI, HTOL) of circuits is predominantly done targeting the digital and I/O portion of the chip [6]. The conditions of supply voltage levels, temperature, and the required power-on hours (POH) under various system configurations are derived to meet the target average failure rate (AFR). The fundamental stress mechanisms of such digital and I/O circuits are well understood and such BI process is highly repeatable. These mechanisms for the analog and PM circuits fundamentally differ from those for digital circuits. For SoCs targeting fast moving and performance driven markets, it is necessary not only to move to latest technology nodes (UDSM) quickly but also to define and use new and unqualified devices to achieve critical performance, cost and reliability goals. The circuits that use such new devices need to be qualified for reliability. Hence an independent BI strategy is defined for analog and PM circuits.

Dynamic stress conditions are avoided to make the whole BI process cost effective using low cost test equipments, and to meet the various electrical and mechanical constraints. Specific analog test modes are designed to achieve BI goals with minimal loss of coverage and make the whole BI process low cost and robust. This strategy was applied for a 450mA, direct battery (~5V) DCDC switching regulator integrated into a SoC in a UDSM digital CMOS process. The reasonably high load requirement, the high terminal voltages due to the direct battery operation, with native technology supporting only low voltage transistors (~3V) makes the whole circuit design very challenging. BI and HTOL qualification was done at pre-defined circuit conditions enabled by two additional test modes to apply voltage stress conditions for the NMOS and PMOS power FETs and shutdown condition. During the BI operation the devices are screened at predefined critical time points to gain information on progressive stress / aging effects.

III. RESULTS

All the above techniques discussed are useful and applicable to the UDSM mixed-signal SoC design with integrated PM. Typical application scenario has a direct battery (VBAT) of up to 5V as input supply. The external capacitor on VDD_DIG can be as high as 100µF to support high transients during scan shifting. The respective nominal supply levels are VDD_ANA at 1.8V, VDD_DIG and VDD_MEM at 1.2V. The overall functional, analog power-up time of the chip is about 6 ms to cater to the PM architecture shown in Figure 1. But the test mode power-up time is optimized to less than 400 µS (about 15 times shorter). The test mode detect circuit consumes a maximum of up to 40 mA only during power-up and is disabled after power-up. The internal crude supply is designed to meet a nominal level (V_{CRUDE}) of VDD_DIG and most logic circuit in the POR sequencer circuit is supplied by this during power-up and by VDD_DIG after power-up. During power-up the internal supply consumes up to 200µA from a 1.8V supply while it is switched off after the analog power-up phase. With the proposed VDD_NWA implementation, there was no on-board active component needed for BI and test mode operation hence making the whole qualification process robust and low cost. The I_{DDQ} gating methodology at design and verification levels was implemented and the I_{DDQ} qualification process in silicon was much quicker without any iteration compared to past executions. The targeted PM BI strategy was applied to the switching regulator and several other PM modules in the chip.

IV. CONCLUSIONS

This paper discusses some specific circuit and analog DFT techniques and methodologies used to overcome challenges of mixed-signal SoC qualification that are useful for mixed-signal SoC designs with integrated PM, and in qualifying such products for customer release. Many of these techniques discussed, though applied to PM system, are not limited and can be applied generically to most analog and mixed-signal modules.

REFERENCES

[1] "AEHR Max3 enhanced dynamic burn-in system," http://www.aehr.com/investors/max3.html.

[2] Alan Moloney; "Power Supply Management – Principles, Problems, and Parts," Analog Dialogue, Vol 40, Analog Devices Inc., May 2006.

[3] Mario Manninger; "Power Management for Portable Devices," Proc. Of 33rd ESSIRC, pp. 167-173, 2007.

[4] Ackerman, R.; "Doing more with less: a recipe for rapid IDDQ development," Proc. of IEEE International Workshop on Current and Defect Based Testing, pp. 33- 42, 2004.

[5] S. Steinhorst; L. Hedrich; "Model Checking of Analog Systems Using an Analog Specification". Proc. of Design, Automation and Test in Europe (DATE) Conference, pp. 324 – 320, 2008.

[6] Chin-Long Wey; Meng-Yao Liu; "Burn-in stress test of analog CMOS ICs, " Proc. of 13th Asian Test Symposium, pp. 360 - 365, 2004.