A New Method for Automated Generation of Compensation Networks - The *EDA Designer Finger*

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***Abstract*—In this paper a new frequency compensation method based on automatic topology modification of analog amplifier circuits is presented. Starting from an uncompensated circuit topology in closed-loop configuration, a capacitance is inserted between each pair of nodes. Subsequently, the set of inserted capacitances is reduced to a manageable size using a selection algorithm based on eigenvalue sensitivity calculation. Finally, the remaining capacitances are sized by a numerical optimization method. The presented method is demonstrated on a transimpedance amplifier design for an industrial HDTV application.**

I. Introduction

Frequency compensation is one of the most important and often most difficult tasks in analog circuit design. Especially in integrated circuit design frequency compensation is directly related to stability issues that come into picture by the many transistors, parasites causing lots of local feedback loops. This situation becomes even more complicated in operating or working configuration of the circuit, i.e. for the closed-loop case. Due to the many feedback paths and bidirectional signal-flow standard feedback formulas used in control theory for non-conservative systems may not be valid since it might be very difficult to open the system to just one feed-forward path. This becomes especially evident for circuits that are designed for high performance in bandwidth where classical compensation increasing gain and phase margin will result in significant reduction of bandwidth. This paper takes a different approach to compensate such systems, the direct frequency compensation. To motivate the approach of direct frequency compensation Fig. 1 illustrates an uncompensated circuit in working configuration (i.e. closed loop: right lower corner). The amplifier may show a transient response according to Fig. 2 left. The reason for such "ringing" effects are dominant poles close to the imaginary axis in the complex plane (Fig. 2(right)). How can the circuit now be directly compensated? The answer is to find circuit modifications that allow the poles and zeros to be shifted in such a way that the transient response will show no ringing correlating with a frequency response without peak.

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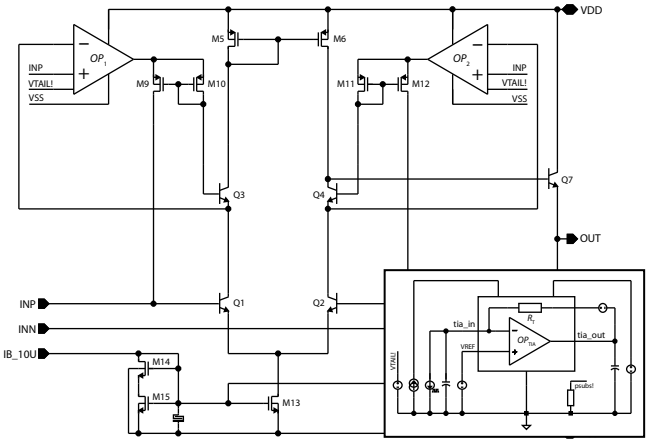

Fig. 1. Amplifier circuit

Section II describes the basics of direct frequency compensation, followed by the algorithm developed to automatically generate a compensation network. Section III demonstrated the developed methodology on an industrial circuit for high speed Blu-ray signal processing.

II. Basic Idea

The novel methodology is not based on the standard control-theory approach using Nyquist criterion [1] by opening the system and subsequently increasing gain and phase margin. The underlying idea is "direct frequency compensation" meaning that compensation is performed in working or closed-loop configuration. The circuit is modified in such a way that poles and zeroes are directly moved to those positions that the circuit will show an optimal frequency behavior. We define such behavior by maximum bandwidth with minimum ringing or overshoot. For a system with two dominant poles this means a conjugate complex pole-pair positioned on the $45°$-axis as illustrated in Fig. 3. The larger the radius of conjugate complex poles the larger the bandwidth of the circuit. How do we obtain

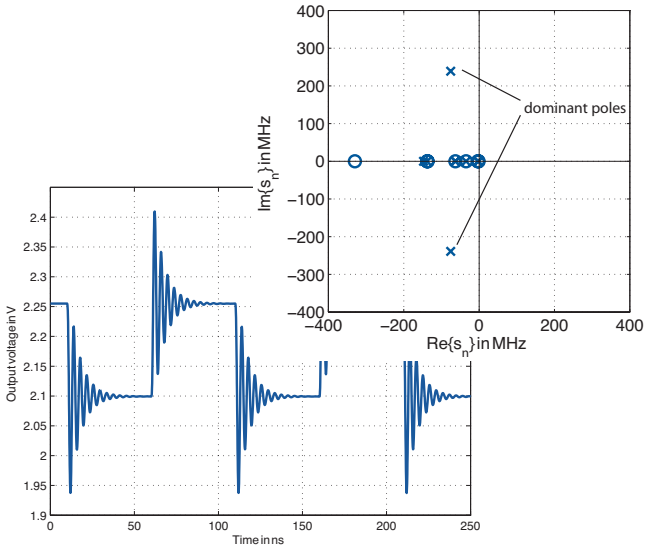

Fig. 2. Transient response and pole-zero plot

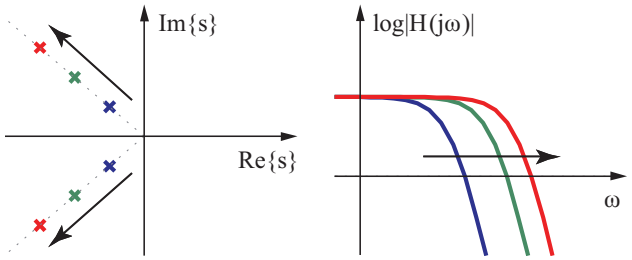

Fig. 3. Compromise between maximum flat frequency response and highest bandwidth

such pole-shifts? The underlying idea can be rooted back to discrete circuit design and bread boarding. If the circuit was not working correctly the designer touched different devices with his finger observing the curves on the oscilloscope. In many cases the circuit suddenly began to work correctly. So the designer would then try to modify the circuit replacing or modeling his finger by inserting/connecting resistors or capacitances to the wire or device he just was touching when the circuit started to work.

To transfer the methodology to integrated circuit design and modern EDA-methods we have developed the following strategy for automated frequency compensation. The underlying idea is to imitate the finger of the designer by inserting new elements into the circuit followed by a selection algorithm that extracts and later sizes only these inserted elements that improve the performance of the circuit:

Starting with an uncompensated design in the first step capacitances are inserted between all nodes of the circuit. We insert capacitances (resistive-capacitive branches are also possible) in order not to chance the operating point. It should be noted, that this is a combinatorial problem, i.e. the possible number of inserted branches/capacitances is

$$N = \frac{n(n-1)}{2}, \tag{1}$$

where n are the number of nodes of the circuits.

Hence, already for a small circuit with 9 nodes 36 capacitances are obtained. Fig. 4 shows an example of some (not all) new introduced capacitances. Note, that the real finger of

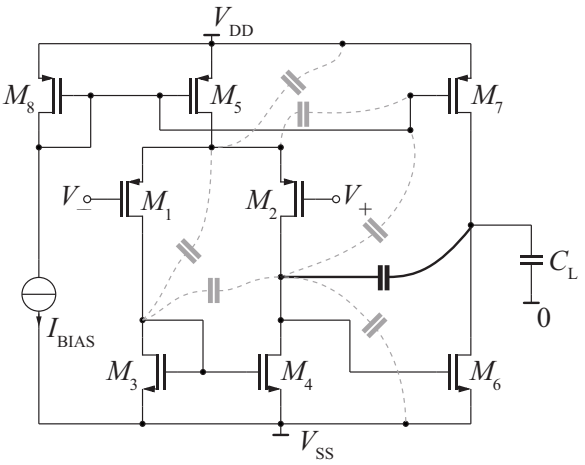

Fig. 4. Connection of capacitances in a circuit

a designer only allows for local additional elements or circuit modifications, while the *EDA Designer Finger* introduced in this paper also generates couplings over different stages of the circuit.

The idea now is to investigate the influences of the new introduced capacitances with respect to the closed-loop poles as illustrated in the root-locus plot in Fig. 5. From the root-locus plots conclusions can be directly drawn for frequency behavior and stability. The advantage of this approach is that no open-loop configuration is needed, and that the frequency behavior can be highly optimized, due to shaping frequency and transient response by taking advantage of complex pole pairs as already outlined in Fig. 3.

Here, two problems arise: On the one hand even for

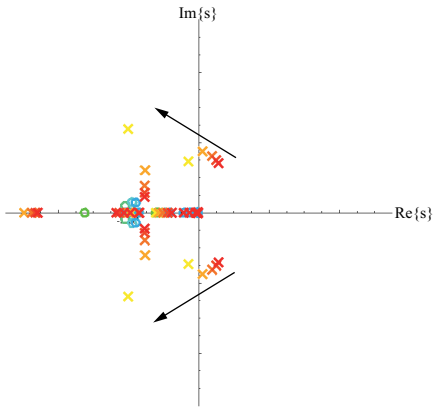

Fig. 5. Root-locus plot

medium-sized circuits hundreds of introduced capacitances blow up the computational effort enormously, and on the other hand traces of root loci are partly highly nonlinear and bifurcations may occur.

Hence, the next important step is to reduce the complexity of the compensation network formed by all the inserted capacitances. This is done in two ways: First, only those capacitances are kept that lead to eigenvalue shifts, which improve the performance, i.e. that move the eigenvalues in the gray area as depicted in Fig. 6. Secondly, a ranking is

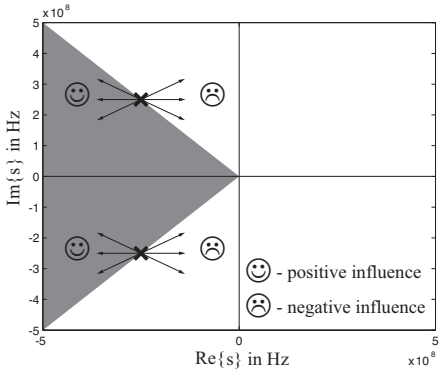

Fig. 6. Definition of influence on relevant poles

generated identifying those capacitances that have the most significant influence on the dominant pole or pole-pair.

To solve the problem, a ranking based on eigenvalue sensitivities is introduced [2], [3].

$$S(p_i) = \frac{\partial \lambda}{\partial p_i} = (\mathbf{v}^{\mathrm{H}}\mathbf{C}(\mathbf{p})\mathbf{u})^{-1}\mathbf{v}^{\mathrm{H}}\left(\frac{\partial \mathbf{G}}{\partial p_i} - \lambda\frac{\partial \mathbf{C}(\mathbf{p})}{\partial p_i}\right)\cdot\mathbf{u} \tag{2}$$

Eq. 2 shows the formula that can be obtained for a generalized eigenvalue problem [4] of the form

$$(\mathbf{G} - s\mathbf{C}(\mathbf{p}))\cdot\mathbf{u} = \mathbf{0} \tag{3}$$

$$\mathbf{v}^{\mathrm{H}}\cdot(\mathbf{G} - s\mathbf{C}(\mathbf{p})) = \mathbf{0}. \tag{4}$$

$\mathbf{u}$ and $\mathbf{v}$ denote the right and left eigenvectors associated with the Laplace variable s (corresponding to the eigenvalue λ in time domain), and $\mathbf{v}^{\mathrm{H}}$ denote the Hermitian transpose of $\mathbf{v}$. $\mathbf{G} - s\mathbf{C}(\mathbf{p})$ is obtained by setting up e.g. modified nodal equations and separating them into static $\mathbf{G}$ and dynamic $\mathbf{C}(\mathbf{p})$ part (matrix $\mathbf{C}(\mathbf{p})$ is a function of the introduced elements/parameters $\mathbf{p}$). Hence, the $\mathbf{G}$-matrix contains all resistive components as well as controlled sources, while the $\mathbf{C}$-matrix only contains capacitances (and inductances). λ denotes the eigenvalue of interest (dominant eigenvalue), while p represents the parameter (circuit element) for which the eigenvalue sensitivity is calculated. In the case of a purely capacitive compensation network the derivation of the respective eigenvalue sensitivities is rather simple (details in [5]). Hence, the complete list of sensitivities for all capacitances w.r.t. a selected eigenvalue can be calculated with a few matrix operations. This is our ranking list, which is then sorted w.r.t. the absolute value of the sensitivity and the direction (gray box in Fig. 6). In subsequent steps all non-dominant or improper w.r.t. direction capacitances are removed so that only the dominant capacitances from the top of the ranking list remain. The final step is to size the capacitances in the order of the ranking list until a performance optimum of the circuit is obtained [6].

A. The EDA Designer Finger Flow

To cope with the combinatorial complexity of the problem that was motivated in the previous section, a workflow, the *EDA Designer Finger*, has been developed. Fig. 7 shows the developed flow, which was designed to especially reduce the enormous complexity of the problem finding a compromise between computational effort, quality (local optimum) and speed. The flow is divided into the main program and the sizing

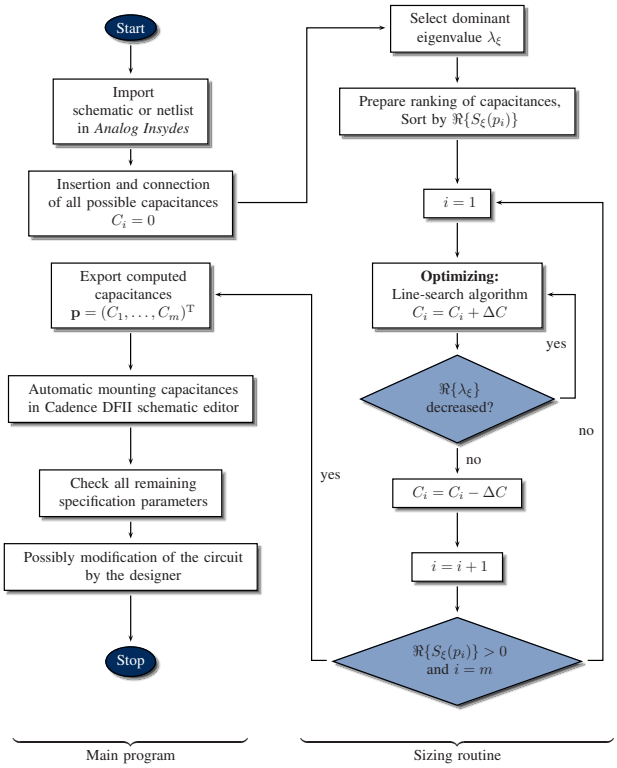

Fig. 7. Full automatic topology modification

routine for the capacitances. In the first step after inserting all possible capacitances setting their values to $C_i = 0$ the circuit designer has to manually choose the dominant or the complex eigenvalue, which is responsible for ringing effects in time domain. Usually, these are poles with a larger imaginary part compared to the real part. Following, the sizing routine generates a ranking list of all sensitivities for all inserted capacitances with help of Eq. 2. Capacitances with negative influence according to Fig. 6 will be removed from the circuit. Now, the actual sizing process starts. The sizing method is a simple line-search optimization procedure. The coordinates are the capacitances C_i. The step size ΔC for computing new

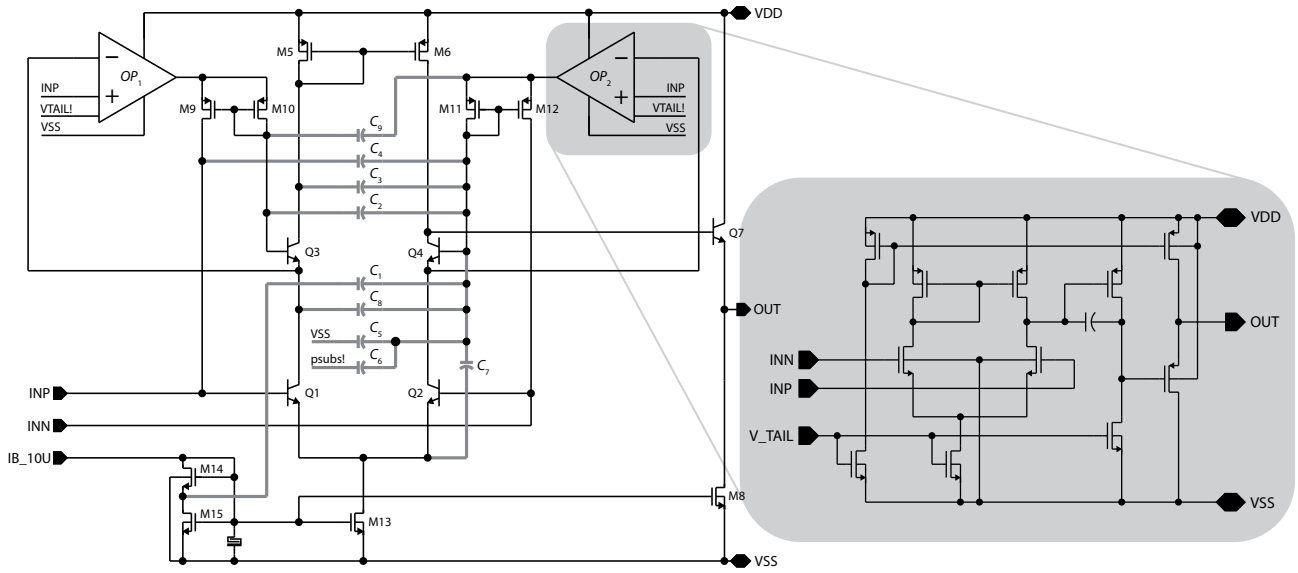

Fig. 9. Transimpedance amplifier with control OpAmps

iterated capacitances can be fixed, e.g. to $5\,\mathrm{fF}$. After each optimization step the real part of eigenvalue λ_ξ is checked if its absolute value has increased (less ringing and higher bandwidth). That means that the selected eigenvalue moves into the direction of gray depicted area in Fig. 6. If the real part cannot be further increased (absolute value of real part) a local optimum is reached (Fig. 8) and last step will be canceled.

Now, the next capacitance C_{i+1} of the ranking list will be chosen. The sizing routine will be finished if all capacitances from the ranking list cannot improve the frequency-behavior anymore. The sized capacitances will then be exported automatically from Analog Insydes [7] to the schematic editor Cadence® Composer [8] and inserted to the amplifier circuit. After all, the circuit designer may simulate the circuit and check further specification parameters like PSRR, noise etc. of his design for further optimization.

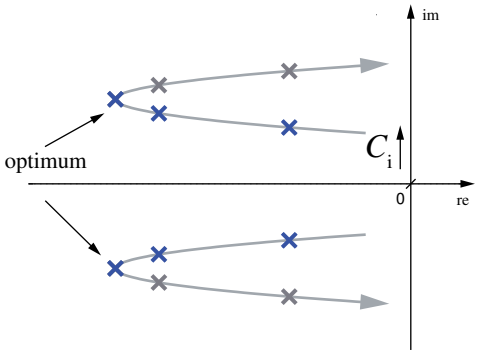

Fig. 8. Optimum of eigenvalue position

III. Example: High Performance TIA

The presented methodology has been successfully applied to a transimpedance amplifier (TIA, Fig. 9) used in an industrial Optoelectronic Integrated Circuit (OEIC) design [9]. These classes of amplifiers have to provide high bandwidth, high gain and slew rate, low offset, and low peaking in the closed-loop frequency response. To determine the characteristics of the TIA, the test bench in Fig. 10 was used. The challenge is to get a very fast circuit by introducing complex pole pairs as motivated in the preceding sections. We allow some overshoot in the transient response and peaking in frequency response (Table I) to improve the slope of the output signal.

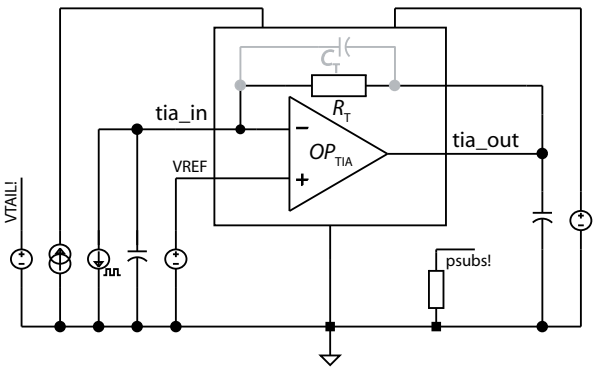

Fig. 10. Toplevel test bench

A. TIA Circuit

Given by the specifications, the TIA designed in this example needs to obtain a transimpedance R_T of $15.8\,\mathrm{k\Omega}$ or $84\,\mathrm{dB}(\Omega)$. Because a $0.6-\mu\mathrm{m}$ BiCMOS technology had been chosen, fast and well-matching bipolar transistors could

TABLE I
SPECIFICATION AND RESULTS OF COMPENSATION METHODS

Parameter	Specification	Compensation: dominant-pole	Compensation: line search
3dB Bandwidth	$\geq 250\,\mathrm{MHz}$	$245\,\mathrm{MHz}$	$362\,\mathrm{MHz}$
Slewrate (rising)	$\geq 400\,\mathrm{V/\mu s}$	$1000\,\mathrm{V/\mu s}$	$1100\,\mathrm{V/\mu s}$
Slewrate (falling)	$\leq -400\,\mathrm{V/\mu s}$	$-530\,\mathrm{V/\mu s}$	$-502\,\mathrm{V/\mu s}$
Peaking in frequency response	$\leq 1\,\mathrm{dB}$	$0.67\,\mathrm{dB}$	$0.9\,\mathrm{dB}$
Total Capacitance	$---$	$75\,\mathrm{fF}$	$5.8\,\mathrm{pF}$ (9 Caps)

be used in the design. Fig. 9 shows the internal operational amplifier of the TIA (without the gray capacitances). BJTs are used in the first stage. A base-current cancellation is applied to improve the offset ($M_9 - M_{12}$). Due to the low supply voltage, controlling op-amps (OP_1, OP_2) are used to ensure that $Q_1 - Q_4$ do not leave the active region.

In order to demonstrate the strength of the developed method compared to classical compensation, the TIA circuit was compensated with the classical dominant-pole compensation C_T, see Fig. 10. This compensation capacitance creates a dominant pole in the open-loop frequency response. Following, the TIA was optimized by a numerical optimizer (WiCkeD [10]), w.r.t maximum flat frequency response and bandwidth. The result after circuit optimization was that the TIA could not fulfill the specification in $-3\,\mathrm{dB}$-bandwidth (Table I). Therefore, the dominant-pole capacitance C_T was removed from the circuit and the new *EDA Designer Finger* algorithm was applied.

B. TIA Results of EDA Designer Finger

The TIA network consists of $n = 37$ nodes; hence, $N = 666$ capacitance insertions are possible. We start with the first complex pole having a larger imaginary part than its real part ($s_p = (-4.73 \cdot 10^8 + \mathrm{j}1.26 \cdot 10^9)\,\frac{\mathrm{rad}}{\mathrm{sec}}$), see in Fig. 12: poles of the uncompensated TIA. After applying a ranking using the sensitivity formula from Eq. 2, the number of relevant capacitances was reduced to 231. From this list, the 9 most dominant capacitances were chosen and sized with the line-search algorithm (Fig. 7) using a fixed step size of $\Delta C = 5\,\mathrm{fF}$. These 9 capacitances were included in the circuit as shown in Fig. 9 (gray capacitances).

Table II shows the inserted capacitances with their calculated values and their sensitivities S_i before starting the line-search algorithm ($C_i = 0$). The table is sorted by the absolute values of sensitivities showing that capacitance C_1 has the largest influence. It is connected between current mirror reference branch (M_{11}), and main bias system of the TIA (M_{14}, M_{15}). Fig. 11 presents the frequency response of uncompensated, classical compensated and line-search compensated TIA. The *EDA Designer Finger* compensation yields a significant higher bandwidth than the dominant pole compensation. The difference in $-3\,\mathrm{dB}$-bandwidth is almost $120\,\mathrm{MHz}$, see Table I. An explanation for higher bandwidth is illustrated by Fig. 12. The line-search algorithm shifts the dominant poles of the uncompensated TIA to 45°-axis. This means that the amplifier shows lower peaking in frequency response but keeps almost the same bandwidth as the uncompensated amplifier. In Fig. 13 the transient response of uncompensated and compensated TIA is displayed. Due to the finally obtained position of the dominant complex pole pair the circuit only shows one overshoot in time domain and fulfills all specifications.

TABLE II
SENSITIVITY AND VALUE LIST FOR TIA

Capacitance C_i	Value	Sensitivity S_i ($C_i = 0$)
C_1	$160\,\mathrm{fF}$	$-2.67 \cdot 10^{21} - \mathrm{j}5.20 \cdot 10^{21}$
C_2	$1\,\mathrm{pF}$	$-5.00 \cdot 10^{21} - \mathrm{j}2.34 \cdot 10^{21}$
C_3	$1\,\mathrm{pF}$	$-4.36 \cdot 10^{21} - \mathrm{j}2.67 \cdot 10^{21}$
C_4	$1\,\mathrm{pF}$	$-3.35 \cdot 10^{21} - \mathrm{j}3.42 \cdot 10^{21}$
C_5	$1\,\mathrm{pF}$	$-3.35 \cdot 10^{21} - \mathrm{j}3.42 \cdot 10^{21}$
C_6	$1\,\mathrm{pF}$	$-3.35 \cdot 10^{21} - \mathrm{j}3.41 \cdot 10^{21}$
C_7	$180\,\mathrm{fF}$	$-3.30 \cdot 10^{21} - \mathrm{j}3.10 \cdot 10^{21}$
C_8	$300\,\mathrm{fF}$	$-3.26 \cdot 10^{21} - \mathrm{j}2.56 \cdot 10^{21}$
C_9	$120\,\mathrm{fF}$	$-1.80 \cdot 10^{20} - \mathrm{j}1.26 \cdot 10^{20}$

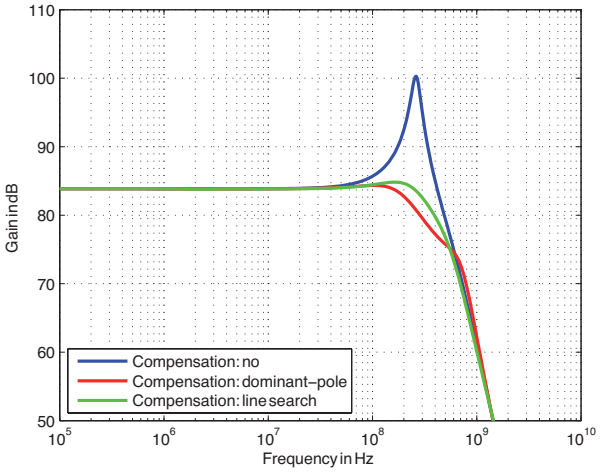

Fig. 11. Frequency response of closed-loop TIA

IV. CONCLUSION

In this contribution, a novel approach to automated frequency compensation for linear integrated amplifier circuits was introduced. The developed methodology automatically synthesizes new compensation networks using direct compensation based on eigenvalue sensitivity calculations. In subse-

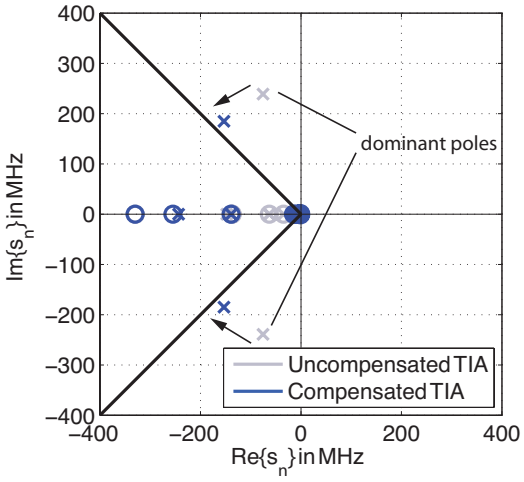

Fig. 12. Closed-loop pole-zero plot

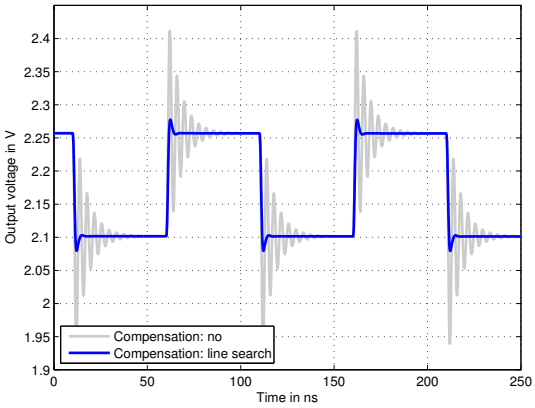

Fig. 13. Transient response

quent steps the new introduced elements are sized for optimizing the frequency performance of the circuit. The procedure was demonstrated and verified on an industrial transimpedance amplifier in a $0.6-\mu\mathrm{m}$ BiCMOS technology. In comparison to a classical compensation, a significantly improved bandwidth could be achieved. Future activities include RC-branch insertion as well as further experimental confirmation of the simulation results.

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