Statistical aspects of NBTI/PBTI and impact on SRAM yield

Asen Asenov[1,2], Andrew R. Brown[1] and Binjie Cheng[1]
[1] Device Modelling Group, School of Engineering, University of Glasgow
Rankine Building, Oakfield Avenue, Glasgow, G12 8LT, UK
[2] Gold Standard Simulations Ltd.
Asen.Asenov@glasgow.ac.uk

***Abstract*— Quantitative simulations of the statistical impact of negative-bias-temperature-instability (NBTI) on pMOSFETs, and positive-bias-temperature-instability (PBTI) on nMOSFETs are carried out for a 45nm low power technology generation. Based on the statistical simulation results, we investigate the impact of NBTI and PBTI on the degradation of the static noise margin (SNM) of SRAM cells. The results indicate that SNM degradation due only to NBTI follows a different evolution pattern compared with the impact of simultaneous NBTI and PBTI degradation.**

Keywords-NBTI; PBTI; Statistical Variability; SRAM; Static Noise Margin

I. INTRODUCTION

Statistical variability (SV) introduced by discreteness of charge and granularity of matter has become a major challenge for scaling and integration. The major sources of statistical variability in conventional (bulk) MOSFETs include random discrete dopants (RDD) [1], line edge roughness (LER) [2] and poly-silicon granularity [3]. Statistical variability approaches more than 50% of the total variability in the 45 nm technology generation [4] and is becoming the dominant component of the variability at the 32 nm technology generation [5].

Statistical variability already profoundly affects SRAM design. Tight threshold voltage matching is needed to control the noise margin variability. At the same time, an extremely tight area budget limits the transistor sizing options, commonly employed in the analogue domain for improving the matching properties. Consequently, the impact of SV on the functionality and performance of SRAM is one of the vibrant areas of variability-aware-design research [6, 7] and the performance and yield of SRAM reflects the ultimate ability that a particular technology generation can offer [8]. In logic circuits SV causes statistical timing problems and increasingly leads to hard digital faults. In both cases the statistical variability restricts the supply voltage scaling, adding to the power dissipation problems [9].

On top of statistical variability, statistical aspects of reliability are becoming an increasing problem with scaling [10,11] and may affect the life-span of circuits and systems in the near future. Most device reliability problems are associated with generation of fixed charges or the trapping of electrons and/or holes on defect states in the gate stack during circuit operation. The introduction of high-κ dielectrics can exacerbate these problems due to higher defect densities and lower dielectric stability. Due to the discrete nature of the fixed charges and trapped carriers, reliability problems in sub-45 nm technology devices will have a distinct statistical manifestation. For a particular density of hot carrier/NBTI/stress generated defects the change in the characteristics of any nano-CMOS device during circuit operation will vary depending on the actual position of single or multiple defect charges in the channel region of the transistor. Using experimental data for the stress dependence of the average density of the stress generated charge and defect states, we study the statistical aspect of NBTI degradation in concert with all other static SV sources typical for a 45nm low-power (LP) technology generation. We also investigate the impact of NBTI on statistical static noise margin (SNM) degradation of 6T SRAM. Due to the increasing importance of PBTI with the introduction of high-κ / metal gate stacks, we also explore the additional impact of PBTI on statistical SNM degradation behaviour.

II. SIMULATION METHODOLOGY

The simulated devices are n- and p-MOSFETs that correspond to early stages of the 45nm LP technology generation. Details about the device structure and doping profiles are published elsewhere [12,13]. We simulate NBTI variability associated with fixed/trapped random positive charges in concert with all other variability sources relevant for this technology. In order to save computing time we have simulated square 42×42nm devices, which have SiO_2 oxide thickness of 1.7nm. Our previous studies of statistical variability in fresh n- and p-channel 45nm LP transistors yielded excellent agreement with measurements [12,13]. The simulations were carried out with the Glasgow 3D 'atomistic' simulator, which deploys fine grain discretisation and density gradient quantum corrections accurately resolving the contribution of individual discrete dopants and trapped charges [5]. Random discrete dopants and line edge roughness were included in the simulations as the dominant sources of statistical variability in the fresh pMOSFETs, however

This work was supported by the European FP7 Projects "Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies (REALITY)" and "Terascale reliable adaptive memory systems" (TRAMS)"

978-3-9810801-7-9/DATE11/©2011 EDAA

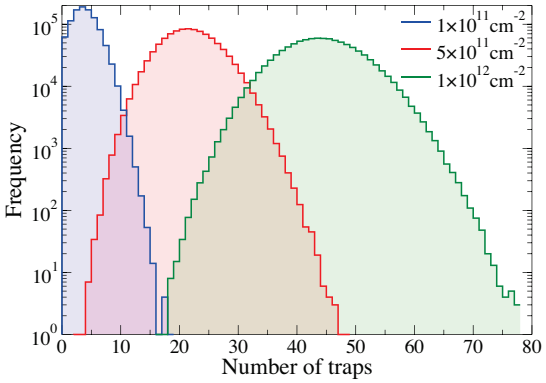


Fig. 1. Distributions of the number of traps generated in a 4500nm^2 region at the Si/SiO_2 interface obtained from 1,000,000 generated devices. Three levels of degradation are presented with areal charge density of 1×10^{11}cm^{-2}, 5×10^{11}cm^{-2} and 1×10^{12}cm^{-2}.

potential pinning at polysilicon grain boundaries is additionally included for the nMOSFETs [13].

In the statistical NBTI simulations the areal charge density associated with the threshold voltage shift observed in NBTI measurements of large self-averaging structures is translated into discrete trapped charges in microscopically different individual devices. With the assumption that all the charges are trapped at the Si/SiO_2 interface, a fine, auxiliary 2D mesh is imposed at the interface. A rejection technique is used at each node of this mesh to determine if a single positive charge is located at that node or not based on the given areal charge sheet density. If it is determined that a single charge should be placed there then the charge is assigned to the surrounding nodes of the 3D discretisation mesh using a cloud-in-cell charge assignment scheme.

In Fig. 1, the distributions in the number of traps obtained using this method are presented for a 4500nm^2 region at the SiO_2 interface. 1,000,000 "atomistically" different devices were generated with the traps having three different areal sheet densities - 1×10^{11}cm^{-2}, 5×10^{11}cm^{-2} and 1×10^{12}cm^{-2}. This gives an expected number of traps of 4.5, 22.5 and 45 respectively. The distribution in the number of traps produced here follows a Poisson distribution.

Fig. 2 illustrates results of the simulation of one particular pMOSFET that is microscopically unique in terms of RDD distribution and LER pattern (a) without and (b) with additional trapped charges. Both the colour mapped hole concentration and the positions of the random dopants are shown (acceptors in blue, donors in red). One iso-concentration surface is included providing a clear visual impression of the nonuniform channel formation due to RDD and LER. In Fig.2a the channel initially forms on the right-hand-side (RHS) of the device, and the majority of the current near threshold flows through this region. This is due to the relatively small number of dopants in this region. The surface plot above the device shows the hole concentration in a slice through the channel indicating that the impact of each discrete dopant is accurately resolved.

In Fig.2b a random set of interface trapped charges (coloured green), with a sheet density of 5×10^{11}cm^{-2}, is added

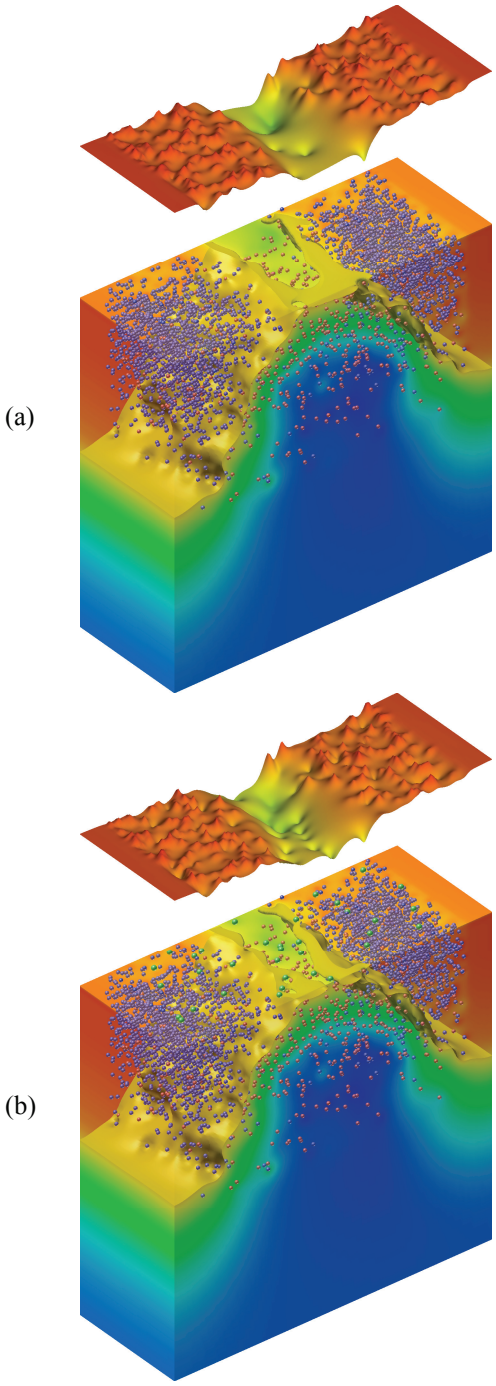


Fig. 2. Hole concentration in one particular microscopically different p-channel device that includes random dopants and LER (a) with and (b) without additional trapped charges with a sheet density of 5×10^{11}cm^{-2}. Acceptors are shown in blue and donors in red, while trapped charges are green. One iso-concentration surface is included, and the surface plot above shows the hole concentration in a sheet through the channel.

to the device of Fig.1a. This random placement has resulted in two traps occurring at the RHS of the channel where the current flow was predominant before. The charges trapped here effectively block this current path, as can be seen from the iso-concentration surface in this case. The result of this particular configuration of discrete dopants and traps is 'anomalously' a

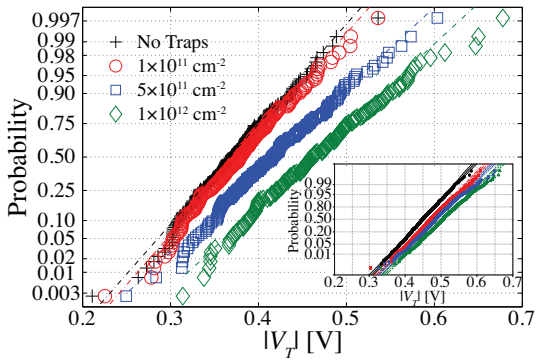


Fig. 3. A normal probability plot of the threshold voltages, V_T of 200 microscopically different 45nm p-channel devices. Plots for devices with no traps, and with trap sheet densities of 1×10^{11}cm^{-2}, 5×10^{11}cm^{-2} and 1×10^{12}cm^{-2}, are shown. The inset shows experimental results for a similar device [9].

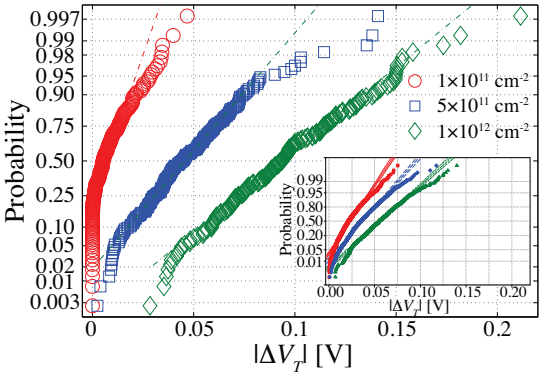


Fig. 4. A normal probability plot of the increase in threshold voltages, ΔV_T, of 200 microscopically different 45nm p-channel devices when trapped charge is introduced at the Si/SiO$_2$ interface. Plots for devices with trap sheet densities of 1×10^{11}cm^{-2}, 5×10^{11}cm^{-2} and 1×10^{12}cm^{-2} are shown. The inset shows experimental results for a similar device [9].

large 140 mV increase in threshold voltage when the expected 'average' increase of the threshold voltage is approximately 40 mV.

III. Device Simulation Results

In order to investigate the effect of additional NBTI-induced interface charges we have performed simulations of statistical samples of 200 devices. The fresh (i.e. non-aged) devices include RDD and LER. The threshold voltages are extracted, based on a current criterion, and their distribution for the fresh devices is plotted with black crosses in Fig. 3. Three different levels of NBTI degradation are investigated corresponding to positive interface charge densities of 1×10^{11}cm^{-2}, 5×10^{11}cm^{-2} and 1×10^{12}cm^{-2}. In each of the initial 200 devices, random discrete charges are generated at the interface corresponding to the above charge densities. Fig. 3 also shows the threshold voltage distributions corresponding to the three different charge densities. Apart from the average increase in the threshold voltage associated with NBTI degradation in large transistors, a marked change in the slope of the distribution is observed in Fig. 3, indicating an increase in the spread with the increase in trap density. Fig. 3 also clearly indicates that the threshold voltage distributions are not

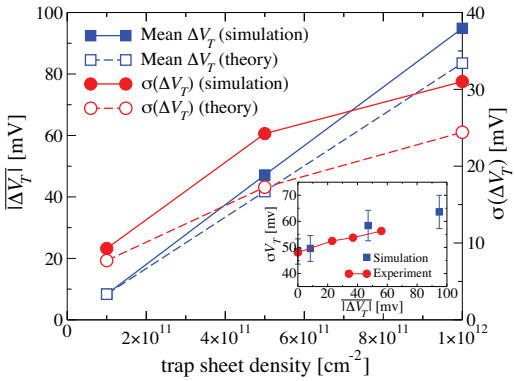


Fig. 5. Mean and standard deviation of the increase in V_T for different trap sheet densities comparing simulations results with simple theory. The inset shows the relationship between σV_T and the average increase in V_T allowing comparison between simulation and experiment. 1σ error bars are included for the simulation data. σV_T from experiement has been scaled to match the same dimensions as the simulated device.

strictly Normal (which would present as a straight line on the plot), and the departure from normality is larger in the tails.

For each of the 200 devices simulated, the change in V_T as a result of the NBTI degradation is shown on a normal probability plot in Fig. 4 for the same three levels of degradation. For low trap sheet density (1×10^{11}cm^{-2}) there are many devices that show no increase in threshold voltage at all. In these cases the traps (if there are any) are not occurring at locations within the channel where there is significant current flow, as dictated by the distribution of discrete impurities. Of the 200 devices simulated with this trap density, 11 devices had a single trap. The threshold voltage shift of these devices varies from 0 to 14mV depending on the trap position and the underlying microscopic distribution of dopants in the channel.

As the number of generated discrete positive charges follows a Poisson distribution, where the variance of the distribution is equal to the mean, for higher trap sheet densities the spread in the number of additional charges becomes significantly larger. This leads to the greater spread in threshold voltage shift with increasing trap density, which is characterised in Fig. 4 by the change in slope of the distributions. This is compounded by the dependence of the threshold voltage shift on the locations of the traps relative to the current conduction paths as discussed previously. Fig. 1 illustrated the most extreme case from Fig. 4 for trap density 5×10^{11}cm^{-2} (i.e. the blue square furthest to the right).

The insets in Figs. 3 and 4 show equivalent experimental distributions for similar 45nm technology devices [9]. In the experimental data, 'maverick' devices with very large ΔV_T are clearly visible, similar to those observable in the simulation results, although in the simulations the effect is stronger due to the smaller width of the devices. Dealing with smaller number of dopants and trapped charges leads to more extreme changes in V_T through specific arrangements of dopants and the limited number of current paths available in the discretely-doped devices.

Fig. 5 shows the mean and standard deviation of the increase in V_T for different trap sheet densities comparing

simulation results with a simple theory which depends on the density of trapped charges only. This theory underestimates the variability as it does not account for the variability associated with the random positions of the charges. The absolute mean value of threshold voltage is increased from 0.23V at zero trap sheet density to 0.32V at trap sheet density of 10^{12}cm^{-2}. Meanwhile, the corresponding standard deviation (SD) is increased from 55mV to 68mV. As the average increase in V_T is directly related to the average trap density this allows comparison of σV_T between the simulation and experiment as shown in the inset of Fig 5.

In this paper we are also considering the effect of PBTI in nMOSFETs. PBTI simulations are carried out on top of the combined static-SV sources simulations of the n-MOSFET that we reported in [12], with PBTI-induced electron trap sheet densities at 10^{11}cm^{-2}, 5×10^{11}cm^{-2} and 10^{12}cm^{-2} respectively. The results follow the same trends as with the NBTI in pMOSFETs. The average absolute threshold voltage value is increased from 0.22 V in fresh devices to 0.30 V at trap sheet density of 10^{12} cm^{-2}, while the corresponding standard deviation increases from 57 mV to 65 mV.

IV. Evolution of SRAM SNM Under the Influence of Device Degradation

Static noise margin (SNM), which is defined as the minimum DC noise voltage needed to flip the memory state during the read operation, and write noise margin (WNM), which is defined as the minimum DC noise voltage needed to fail to flip the memory state during the write operation, are two important SRAM design parameters that determine the yield and stability of SRAM cells. The bias configurations and graphical definitions of SNM and WNM are illustrated in Fig.6. Without bias assistance technologies, the improvement of SNM and improvement of WNM counteract each other under normal working condition, and therefore a design trade-off is needed in order to allow for a balanced performance between read and write operations. The degradation of the pMOSFET caused by NBTI will benefit the write operation at the expense of deterioration of read operation [11].

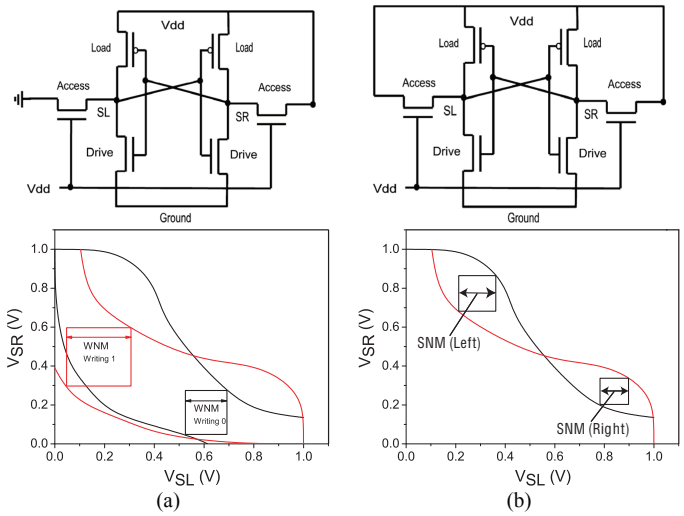


Fig. 6: Bias configuration and graphic definition of (a) WNM, (b) SNM.

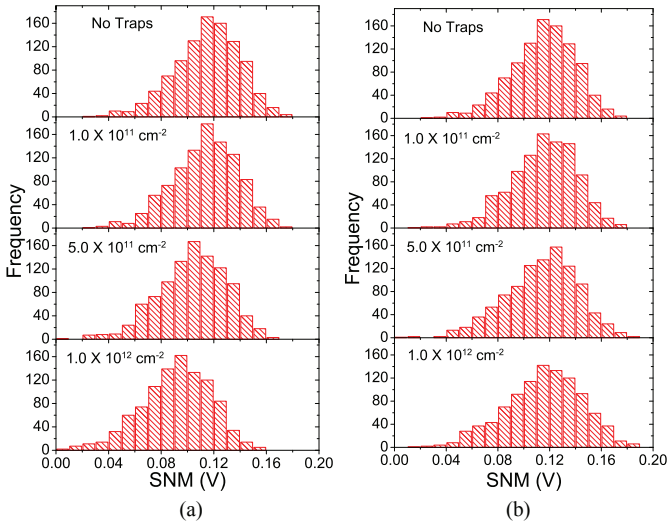


Fig. 7: Distribution of SNM for different degradation stages of (a) NBTI, (b) NBTI and PBTI

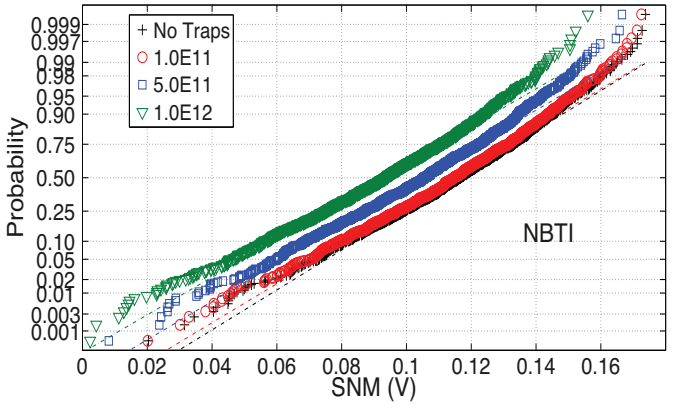
Consequently, we focus on the evolution of SNM under the influence of device degradation in this study.

A two-stage direct statistical compact modelling approach [14] is employed to accurately transfer all the device variability information into BSIM4 compact models. A 6-T SRAM cell with cell ratio of 2 is employed in this study as the test-bed cell. Two simulation scenarios are considered: The first considers the NBTI as the dominant degradation source, which is typical for poly-silicon gate technology; the second considers NBTI and PBTI simultaneously and is in line with the behaviour of high-κ / metal gate stack technology. For each NBTI or NBTI+PBTI degradation stage, a statistical ensemble of 1000 SRAM cells is generated using the Monte Carlo circuit simulation approach describe in [14]. Due to device mismatch, the left-side SNM is not necessary equal to its right-side counterpart. Both SNM values are extracted from SRAM voltage transfer characteristics and the smaller one is chosen as the SNM of the SRAM.

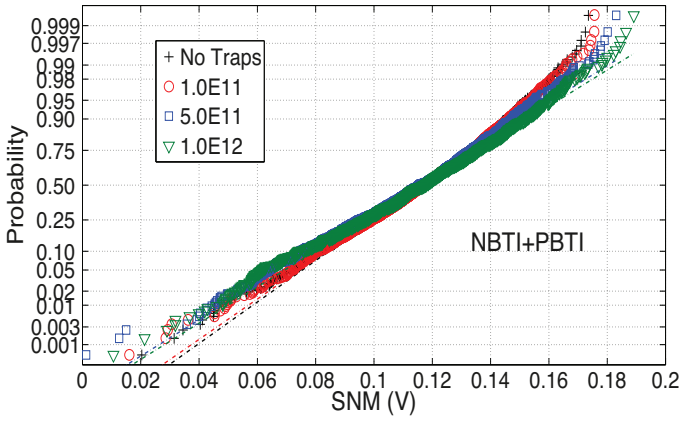
Fig.7 shows the distribution of SNM under the influence of device degradation. With only NBTI considered as the main degradation source, the overall SNM distribution is shifted to the left due to the increase in the absolute value of pMOSFET threshold voltage, resulting in worse average mismatch behaviour between n- and p-MOSFETs in the cell. However, with both NBTI and PBTI playing an active role in the degradation, as expected for high-κ / metal gate stack technologies, the mean of device mismatch between n- and p-MOSFET remains unchanged, and instead of shifting of the distribution, the SNM experiences only a broadening, showing increasing variability.

The probability plots of SNM in Fig.8 further demonstrate the difference in SNM evolution patterns between NBTI degradation only, and combined NBTI and PBTI degradation. In the NBTI-only case the drift of SNM probability distribution is almost parallel at different degradation stages, which indicates that, apart from the distant tails, the SD of SNM is not sensitive to the NBTI-only degradation process. However, for

the combined NBTI and PBTI case, due to the increased variability in the threshold voltage of the nMOSFET and pMOSFET, the slopes of the SNM probability plots are reduced with the increase of trap charge sheet density, indicating an increase in SD of SNM with combined NBTI and PBTI degradation.



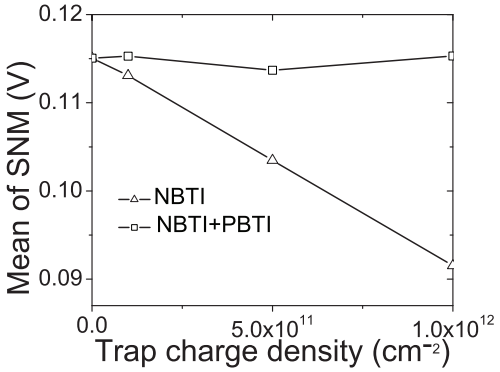
(a)



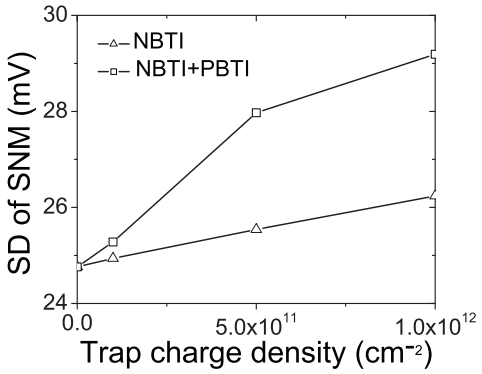
(b)

Figure 8 Probability plot of SNM for different degradation stages of (a) NBTI, (b) NBTI and PBTI

Fig.9 quantifies the impact of the degradation on the SNM evolution. For this particular 45nm LP technology, with NBTI acting as the dominant degradation source, as the trapped charge sheet density increases the mean of the SNM is linearly reduced from 0.116V in fresh transistors to 0.093V at the maximum considered trap sheet density of $10^{12}cm^{-2}$, which represents 20% degradation of the average SNM value. At the same time the influence of NBTI on the SD of the SNM is very mild with the SNM value increasing from 24mV in fresh transistors to 25mV at later degradation stage. However, with NBTI and PBTI present simultaneously, the increase of SD of SNM becomes the major source of SNM concern, increasing from 24mV in fresh transistors to 30mV at later degradation stages. At the same time, the mean SNM value remains almost unchanged, decreasing from 0.116V in the fresh transistors to 0.114V at later degradation stages. However, a reduction in the read speed would be expected with the PBTI degradation in the nMOSFETs since this will adversely affect the performance of the SRAM cell's access and drive transistors.



(a)



(b)

Figure 9 (a) Mean and (b) standard deviation of SNM at different degradation stages.

V. CONCLUSIONS

Statistical 3D simulations are used for the quantitative evaluation of the statistical impact of NBTI under different degradation stages for pMOSFETs corresponding to the 45nm low power technology generation. The statistical aspect of PBTI on nMOSFETs is also explored due to the increasing importance of PBTI with the introduction of high-κ / metal gate stacks. All the statistical degradation information obtained from 3D simulations is transferred into BSIM4 compact models through a two stage direct statistical compact modelling approach, and Monte Carlo circuit simulations are carried out to investigate the impact of device degradation on the SNM of an SRAM cell. The reduction in the mean of the SNM is the major concern associated with the NBTI-only induced SNM deterioration. The increase in SD of the SNM is the major cause of SNM deterioration when NBTI and PBTI are considered simultaneously.

REFERENCES

[1] A. Asenov, "Random dopant induced threshold voltage lowering and fluctuations in sub 0.1 μm MOSFETs: A 3-D 'atomistic' simulation study," IEEE Trans. Electron Devices, Vol. 45, No. 12, pp. 2505–2513, 1998

[2] A. Asenov, S. Kaya, and A. R. Brown, "Intrinsic parameter fluctuations in decananometer MOSFETs introduced by gate line edge roughness," IEEE Trans. Electron Devices, vol. 50, iss. 5, pp. 1254–1260, 2003.

[3] A. R. Brown, G. Roy and A. Asenov, "Poly-Si Gate Related Variability in Decananometre MOSFETs with Conventional Architecture", IEEE Trans. Electron Devices, Vol.54, No.11, pp.3056-3063, 2007

[4] H. Aikawa, E. Morifuji, T. Sanuki, T. Sawada, S. Kyoh, A. Sakata, *et al*., "Variability aware modeling and characterisation in standard cell in 45 nm CMOS with stress enhancement technique", Symposium on VLSI Technology, pp. 90-91, 2008

[5] G. Roy, A. R. Brown, F. Adamu-Lema, S. Roy and A. Asenov, "Simulation Study of Individual and Combined Sources of Intrinsic Parameter Fluctuations in Conventional Nano-MOSFETs", IEEE Trans Electron Dev., Vol. 52, pp. 3063-3070, 2006

[6] A. Bhavnagarwala, X. Tang, J. D. Meindl, "The impact of intrinsic devicefluctuation on CMOS SRAM cell stability", IEEE J. Solid State Circuits, Vol. 36, pp. 658-665, 2001

[7] B. Cheng, S. Roy, A. Asenov, "CMOS 6-T SRAM cell design subject to 'atomistic' fluctuations", Solid-State Electronics, vol. 51, pp. 565-571, 2007

[8] A. Nackaerts, M. Ercken, S. Demuynck, et al. "A 0.314/spl mu/m/sup 2/6T-SRAM cell build with tall tripe-gate devices for 45nm applications using 0.75NA 193nm lithography", Tech Digest IEDM, pp. 269-272, 2004

[9] K. Bernstein, D. J. Frank, A. E. Gattiker, W. Haensch, B. L. Ji, *et al*., "High-performance CMOS variability in the 65-nm regime and beyond", IBM J. Res. Develop. Vol. 50 pp. 433-449, 2006.

[10] S. E. Rauch III, "Review and Reexamination of Reliability Effects Related to NBTI-Induced Statistical Variations", IEEE Trans. Dev. Materials Reliab. Vol. 7 pp.524-530, 2007

[11] V. Huard, C. Parthasarathy, C. Guerin, T. Valentin, E. Pion, *et al*., "NBTI degradation: from transistors to SRAM arrays" IEEE CFP08RPS-CDR 46th Annual International Reliability Physics Symposium, pp. 289-300, 2008

[12] A. Cathignol, B. Cheng, D. Chanemougame, A. R. Brown, K. Rochereau, G. Ghibaudo and A. Asenov, "Quantitative Evaluation of Statistical Variability Sources in a 45nm Technological Node LP N-MOSFET", IEEE Electron Dev. Lett., Vol.29, No.6, pp.609-611, 2008

[13] A. Asenov, A. Cathignol, B. Cheng, K. P. McKenna, A. R. Brown, *et al*., "Origin of the Asymmetry in the Statistical Variability of n- and p-channel Poly-Si Gate Bulk MOSFETs", IEEE Electron Dev. Lett., Vol. 29, No. 8, 2008

[14] B. Cheng, S. Roy, G. Roy, F. Adamu-Lema, A. Asenov, 'Impact of intrinsic parameter fluctuations in decanano MOSFETs on yield and functionality of SRAM cells', Solid-State Electronics, vol. 49, pp. 740-746, 2005