# Modeling Manufacturing Process Variation for Design and Test

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***Abstract*—For process nodes 22nm and below, a multitude of new manufacturing solutions have been proposed to improve the yield of devices being manufactured. With these new solutions come an increasing number of defect mechanisms. There is a need to model and characterize these new defect mechanisms so that (i) ATPG patterns can be properly targeted, (ii) defects can be properly diagnosed and addressed at design or manufacturing level. This presentation reviews currently available defect modeling and test solutions and summarizes open issues faced by the industry today. It also explores the topic of creating special test structures to expose manufacturing process parameters which can be used as input to software defect models to predict die specific defect locations for better targeting of test.**

***Keywords-Manufacturing test; Photolithography; Defect Modeling; Fault Diagnosis; Layout Enhancements for Manufactuing***

## I. INTRODUCTION

For the last decade, the wavelength of lithographic light sources has not scaled in tandem with technology. The transition to deep ultra-violet (DUV) light source (193nm) required changes in lens materials, mask blanks, light source and photoresist. A continuation of the past progression toward shorter wavelengths for optical lithography has been thwarted by several factors, including thermal expansion of photomasks during exposure with shorter wavelengths, difficulty with focusing systems coupled with requirements that the exposure system be purged of oxygen and water at shorter wavelengths. Consequently, as the industry moves towards manufacturing end-of-the-roadmap CMOS devices, lithography is still based on 193nm light source to print critical dimensions of 32nm, 22nm and likely 16nm.

Deep sub-wavelength lithography (DSL) relies on a number of resolution enhancement techniques (RET) that include changes to the light source, photomasks, exposure systems and the layout. Currently, in addition to optical source engineering, a number of layout enhancement for manufacturability (LEM) techniques are being used - including optical proximity correction (OPC) and phase shift masking (PSM).

For process nodes 22nm and below: immersion lithography, dual & triple pattern lithography, source-mask optimization (SMO), and layout compensation for lens aberrations have been proposed. The impact of such changes needs to be corroborated using lithography simulation, which is based on a model. Model inaccuracies may result in systematic defects being passed to silicon. Thus, the models must be continuously validated.

Defect modeling has two explicit goals. The first goal is to assist in manufacturing test pattern development. Without some knowledge about potential defects, manufacturing test patterns may lack adequate coverage resulting in a loss of shipped product quality level (SPQL) [1]. The second goal is to improve yield [2]. If the nature of the expected defects are known a priory, care make be taken during design process to avoid them in the first place. There is historical precedence for both in context of particulate defects [6]. At a time, when particulate defects were the primary mechanism for chip failure, a critical area based defect model was developed. This model was used to predict location of bridge and open faults for better targeting of test [6]. This model was also used during physical design process to reduce critical area and improve yield.

A similar process is needed for modeling lithography related defects. Model development is a 3-step process. First step involves (i) identification of physical mechanisms for manufacturing defects. The second phase involves (ii) modeling the design and manufacturing factors that contribute to occurrence of such defects. The third phase involves, (iii) quantifying the model parameters for a given technology node at certain point of maturity. The first step involves real defect data or hypotheses concerning the source of defects. In case of hypotheses, they must be verified through steps (ii) and (iii) above. Increasingly, hard defect data is difficult to obtain.

Debugging defective chips using optical microscopy is prohibitively expensive in both equipment and time. At 22nm or below, the standard failure analysis process involving decapsulation, stripping layers using reactive ion etch, microsectioning and optical analysis becomes difficult, as (i) the chips are simply too large to explore without some target focus area, (ii) physical stripping and sectioning processes themselves may induce defects and (ii) the defect sizes are often below the level of optical resolution requiring more expensive x-ray systems or scanning electron microscopy. This pushes the model development process towards a hypotheses based approach. The hypotheses based approach may be iteratively validated using a silicon debug process [7]. A defective chip may be analyzed using diagnosis software to localize defects to a specific block or module within a design, which is then analyzed by defect models that have been hypothesized. Such hypotheses may predict defect location and behavior which are then validated by applying patterns and observing response on a tester. This process confirms hypotheses without direct physical observation of defects.

This paper discusses the challenges and possible solutions aimed at creating models and test strategies under manufacturing

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variations. The remainder of the paper is organized as follows. Section II covers the need for manufacturing aware test solutions with pointers to the modeling challenges faced today. Section III briefly lists the typical steps in defect modeling and the lithographic issues that can be tied to defect modeling and diagnosis. Section IV covers from lithographic modeling methods and layout based diagnosis solutions that can be used in manufacturing test today. Section V is a conclusion to the presentation with guidelines on how to model for future manufacturing changes.

## II. PRELIMINARIES

### A. Fabrication Process

The steps involved in fabrication of an integrated circuit are described in this section. Semiconductor fabrication can essentially be categorized into three important tasks.

#### 1) Patterning (Photolithography)

Patterning involves the task of transferring the patterns on the mask onto the wafer. The process of patterning can be additive or subtractive. They involve the process of deposition of a uniform film of material on the wafer; creating structures by lithographic process using a photosensitive material called photoresist and finally clear out areas where metal or other contacts have to be laid using etch process. Photolithography involves the process of preparing the wafer, photoresist coat, exposure followed by baking and development.

##### a) Photoresist Coating

In this step, a light sensitive polymer is evenly applied to a thickness of about 1μm by spinning the wafer. This material is originally insoluble (soluble) but becomes soluble (insoluble) when light is shown upon it. This way patterns that need to stay are prevented from light using the mask.

##### b) Stepper exposure

Once the photoresist has been coated, the wafer is exposed to UV light. The current process technology uses a Argon Fluoride light source with wavelength of 193nm. The light passes through a mask filled with patterns and the lens system and falls onto the wafer. Exposed regions become soluble and the rest stay insoluble. The mask is made of silicate glass; patterns that need to stay on the wafer are opaque and the rest are transparent (for positive photoresist). Figure 1. shows a typical light system used in exposure.

##### c) Photoresist bake and develop

After exposure, the wafer is baked to a particular temperature to aid in the process of dissolving the exposed photoresist. This is called post-exposure bake (PEB). The final process in lithography is to develop the photoresist patterns on the wafer. In this step, the wafer is dipped into a develop solution which washes away all the photoresist regions that have become soluble due to exposure. Now the wafer is ready for etching and repetitive process steps such as oxidation, metal deposition and ion-implantation. It is important to note that the process mentioned here is for a positive photoresist material, which becomes soluble when exposed to light. The opposite happens when a negative photoresist is used.

#### 2) Etching

Etching is the process of removing regions of material not covered by photoresist after lithography. There are different types of etching namely; wet and dry etch. Wet etch involves the use of an etchant solution to clear out the regions. This method is the easiest but does not lead to perfect etch of material. Another type of etch called the plasma etch is a dry method. It uses ionized gas to remove material. This method can be highly controlled and can lead to better etching.

#### 3) Implantation

After patterning and etch, certain regions of the wafer are implanted with dopant atoms to create transistors. Typical dopants are Arsenic, Boron and Phosphorus depending on the type of transistor required. Care is taken to make sure the doping is done correctly as it controls the current flow and hence operation of the transistor.

### B. Lithography Process

#### 1) The Optics

A simple optical lithography system is shown in Figure 1. . The system consists of an effective light source giving out light rays forming a coherence plane that illuminates the opaque photomask. The objective of the lens system is to deliver light from the coherent source with sufficient energy, direction, phase and spatial characteristics through the mask and onto the image plane as shown in Fig.

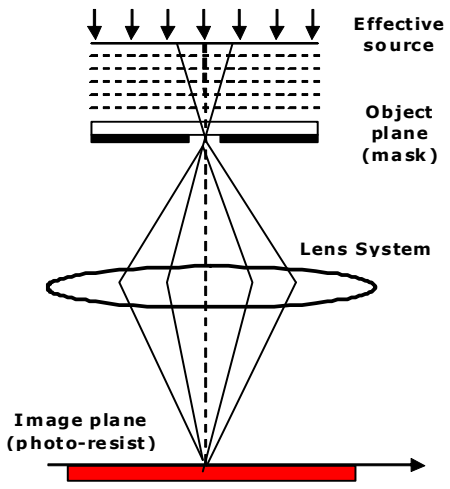


Figure 1. A simple lithography imaging system

The mask used to print features on the wafer is made of silica glass with opaque patterns of chrome imprinted on them. The mask is manufactured by the same photolithographic process. Opaque regions of the mask have zero transmittance and hence reflect the incident light. Other non-opaque regions have maximum transmittance and hence allow light to pass through them. For example in a binary mask (BIM) patterns shaded dark have zero transmittance and the rest have maximum transmittance of 1. The purpose of the lens is to shrink the image and correctly project all portions of the mask pattern onto the wafer. The lens creates a diffraction pattern which resembles the mask pattern and projects it onto the image plane. The image plane for the optical lithography system is a silicon wafer with a coat of light sensitive material called photoresist on it.

Modeling the underlying optics in lithography, aids in predicting the shape of patterns that will be printed on the wafer. There have been many techniques suggested in the literature aimed

at modeling the optical pattern transfer process. These can be classified into major streams: full *physical models* and *phenomenological models*. The full physical models utilize both the optics and the etching process (models to be explained in the next section) to predict the 3D shape of the final pattern. Phenomenological models on the other hand only utilize a simplified etch model while upholding the same level of optical information. A universally used optical model formulation method is the Abbe's method [4]. J. J. Hopkins later simplified it by separating the optical system components and the mask input parameters [5]. A detailed overview of these models is out of the scope of this presentation. Please refer to C. A. Mack's book on optical microlithography [3] for further reading.

*2) Resist*

Resist development is a process by which materials are removed from unprotected regions on the wafer to form the required patterns. As a part of phenomenological models, a few simplified resist models were suggested. These models predict the behavior of the resist after exposure only to the first order, with a minimal set of parameters to control. Examples of such models include the aerial image threshold model, the variable threshold model, and the lumped parameter model. They are primarily modeled for speed and not for accuracy.

The fully physical models on the other hand predict the change in resist composition during the post-exposure bake and development process. The models use parameters such as resist dissolution rate, exposure dose, resist light absorption rate etc. Apart from resist models, fully physical model include etch models. These are similar to the resist models, where instead of the developer solution, the properties of the etchant and its impact on photoresist is modeled to observe the goodness of the wafer before the next stage of processing.

### C. Chemical Mechanical Polishing Process

CMP is the process planarizing the wafer covered by metal or dielectric material. The reason to level out a layer of material on the wafer is to make the height of metal and interconnect features to be uniform and also to aid better printability for layer that will be formed over the current one. Global and local planarity requirements are met using CMP.

CMP involves the process of planarization using an abrasive slurry solution and a polishing pad. The wafer is held using vacuum suction while the polishing pad rotates and moves over the wafer. As the slurry flows in between the polishing pad and the wafer, the abrasive substances remove a layer of material thereby performing planarization.

A well known model for CMP is the Stine's model [11]. This uses the distance of separation between existing features on the wafer and the speed of the polishing pad to predict the height of the resulting wafer. This technique is widely used by various post CMP models that predict polygon height/ imaging system defocus.

## III. Lithographic Distortions

Photolithography, along with other processes such as oxidation, metallization, doping and etching, leads to the creation of the final IC product. In all of these manufacturing processes, statistical variations are commonplace. With scaling come constant changes in each of the above mentioned processes. In lithography, distortions occur due to lens imperfections, change in focus, exposure dose, light source flare, proximity effects–caused by interference of diffraction patterns from neighboring lines, out-of-band-illumination to name a few [3].

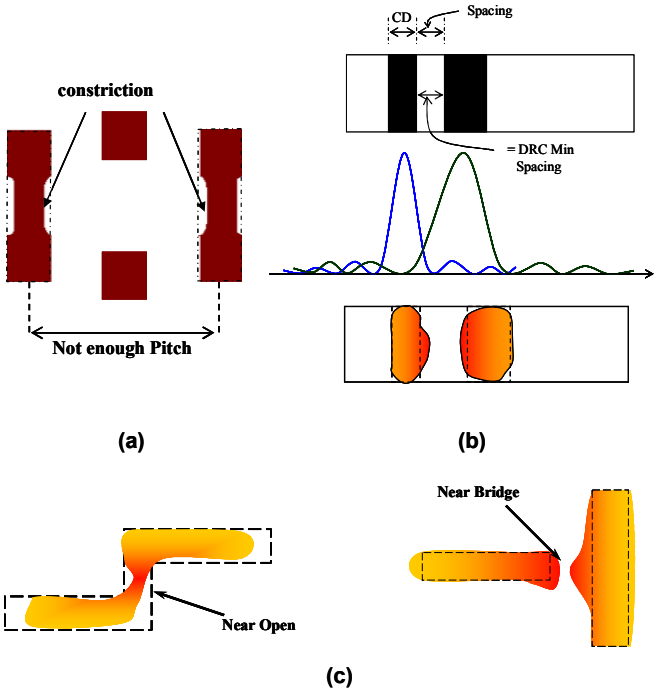


Figure 2. (a) Constriction due to diffraction, (b) metal widening due to constructive interference of diffraction patterns, (c) illustration of soft-faults/defects in layout metal/via/contact polygons to be detected through physical commonality extraction

### A. Proximity based distortions

Photolithography involves the passing light through an opaque mask which is then absorbed by a light sensitive material on the wafer in order to form the required polygons. Light passing through an opaque wafer consisting of region of high and low transmittance leads to the formation of diffraction patterns. Each slit (region of high transmittance) in the mask results in diffraction patterns on the wafer extending significantly up to 3 times the optical source wavelength on either side of the slit. Any other slit (polygon) within this distance will cause interference between the resulting diffraction patterns. The interference pattern can lead to increase or decrease in the final polygon width on the wafer. Constructive interference occurs when the two diffraction patterns are in-phase, resulting in an increase in polygon width (see Figure 2. (b)). Destructive interference occurs when the diffracted waves are out-of-phase with each other resulting in pinching/decrease in polygon width (see Figure 2. (a)).

Other similar types of effects have been observed at polygon corner and edges ("T" and "L" shaped features) causing corner rounding and line end shortening. The region of influence changes with any modifications in the imaging process parameters. Defect models that target complete opens, shorts, resistive opens and bridges have to be modeled based on the impact of neighbors from the layout perspective. Simple stuck-at fault models that target all inputs and output of a gate will not suffice. Distortion specific knowledge will help target potential faults thus improving fault coverage.

### B. *Distortions due to layout density*

Chemical Mechanical Polishing (CMP) is a mechanical process through which metal and dielectric layers are planarized using abrasive materials to the required thickness. Stine et.al [11] showed that the post-CMP thickness is dependent on the density of current and all underlying metal layers. As shown in Figure 3. , isolated lines lead to decrease in final thickness (dishing) and dense features lead to erosion of the planarized material (erosion). Increase or decrease in metal layer thickness at certain areas lead to change in focus in those areas. The density effect is converted to focus variation to observe the change in metal width.

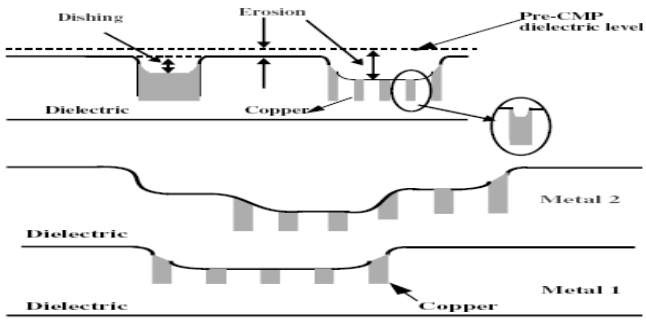


Figure 3. Illustration of change in metal height and width due to pattern density and CMP [10][11]

### C. *Gate length and width distortions*

Similar to the distortions observed while printing metal interconnect lines, poly-gate masks and diffusion masks also undergo them. Proximity effects on poly masks cause fluctuations in width and length of the gate. Coupled with line end erosion (LEE), line-end shortening (LES), line-edge roughness (LER), the gate length varies along its width. Hence gates produced through the photolithography process in deep sub-wavelength lithography (DSL) are non-rectangular in nature (see Figure 4. ). Non-rectangular gate (NRG) models have been proposed that closely approximate the behavior of post-silicon transistors [2][3], nevertheless significant variation exists among manufactured transistors.

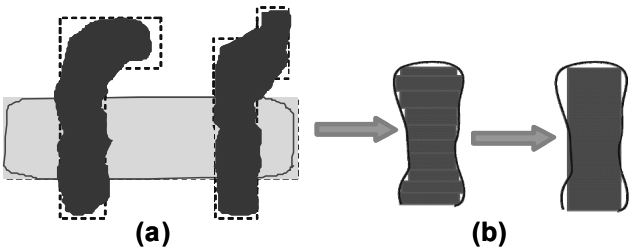


Figure 4. Illustration NRG gate (a) post-litho gate contour, (b) equivalent NRG gate model

## IV. MODELING LITHOGRAPHIC DEFECTS

### A. *Defect Modeling Using Litho Simulation*

Defect/Fault models have to accommodate the fact that unlike logical faults, physical defects are greatly dependent on the neighborhood. For parametric defects such as resistive opens and resistive bridges as well as crosstalk faults, location of the defect on a physical net decides whether the fault is detectable, and if so, the specific pattern(s) that can detect such faults.

Near bridge defects due to lithographic distortion cause increase in coupling capacitance, hence crosstalk. Static crosstalk models use only the coupling capacitance between nets to deduce the vulnerability of the net. Dynamic crosstalk models on the other hand use both coupling capacitance and timing information to accurately filter/predict the potential victim and aggressor nets in the design. In both of these cases, the accuracy of coupling capacitance information forms the basis for effective crosstalk fault detection. In the presence of lithographic variation, the width and height of interconnects on wafer are different from their drawn dimensions. Width changes are caused by proximity effects, whereas the height variation can be tied to CMP driven changes.

These modifications have to be fed into the fault model to accurately predict fault locations and hence produce test patterns aimed at high fault coverage. The modifications themselves are obtained from litho and CMP simulation as described earlier which are controlled by their own manufacturing process parameters.

### B. *Parametric Defects*

Parametric defects include those that impact the performance of the circuit. These can be chiefly those that cause changes in gate and path delays in the design. Gate delays are the primary contributor towards timing violations during the circuit realization process. Lithographic distortions on gate layer masks has been shown to drastically change the ON and OFF current behavior of the transistors. Figure 5. shows the average gate length variation under 10% lithography variations. Gate delay models must have standard cell specific gate length and gate width variation into account in order to effectively predict the critical path.

Path delays are tied to interconnect parameter fluctuations that include resistance and capacitance changes due to variation in length, width and height of the interconnect. As observed in the previous discussion on lithographic distortions, proximity effects and density fluctuations control the behavior of patterns being printed on the wafer. The change in resistance of interconnects and the capacitance between them has to be modeled to predict the extent of impact on path delay.

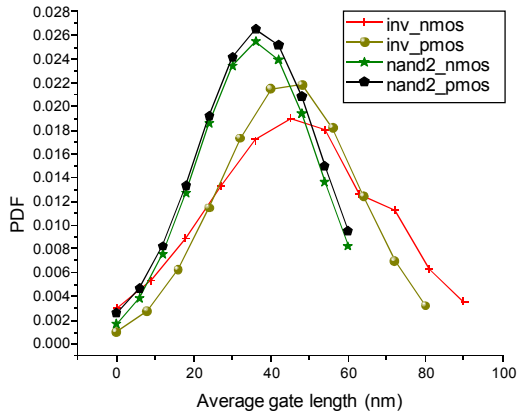


Figure 5. Fluctuation in gate length of transistors within standard cells under lithographic variation-Making parametric defect identification and extraction more complex

Parametric defect analysis and modeling must rely on detailed design information such as static timing data and internal net parasitics (RC) and performs lithography simulation at various lithographic process corners to estimate the range of variation of circuit parasitics. Using this information, parametric hotspots can be identified and test patterns targeted towards detecting them.

## V. MANUFACTURING AWARE TEST METHODS

With the advent of new complex manufacturing schemes, test methodologies have to adapt in order to attain the expected goals. Defect extraction methods must graduate from using simple drawn layout parameters to using pattern matching methods to identify complex polygons that can lead to manufacturing failures. Similarly, as a derivative to defect extraction, test pattern generation also have to incorporate some amount of weight to target location by being manufacturing aware. In this section we also present the importance of using novel test structures to quantify the amount of manufacturing variation and also to identify the source of the same.

### *A. Target Extraction*

Apart from modeling defects, extraction of defects plays a vital part in test pattern generation. Extraction of defect locations can also aid in updating design rules and yield estimates. Lithographic defect extraction have to be performed through simulation due to the high cost involved in manufacturing test chips at varying process corners. Extensive lithography simulations are highly compute intensive and hence cannot be performed on full chip layouts. Typical lithography induced defect mechanisms modeled into complex geometric rules. As the impact of neighborhood on each interconnect is important, these rules do not stop at the closest polygon, but those within a region.

A step further from using geometric rules, pattern matching based vulnerable region identification can also be performed. Pre-created set of patterns that have been extensively analyzed using lithography simulators can be used as a benchmark for defect identification over large layouts.

### *B. Targeted Test Pattern Generation*

Test pattern generation methodologies also have to be modified in order to incorporate changes to defect locations due to manufacturing variations. A combined methodology of lithographic hotspot identification and test pattern generation is an effective targeted test pattern generation approach.

For example, crosstalk based ATPG tools can be tied to a fast lithography simulator which analyzes metal layer masks to produce higher granularity in fault identification and pattern generation. Filtering out potential defect locations can reduce the overhead on ATPG and ATE tools, thus producing more robust and high coverage tests.

### *C. Test Structures*

The use of control structures has been in existence since the introduction of complex manufacturing methods. Control structures were designed to observe the validity of particular process method or as sensors to measure parameter fluctuations. Example of control structures include ring oscillators-to estimate chip frequency changes, spiral structures-for voltage to capacitance measurements; to name a few. Control structures can also be used as aids to improve test pattern application and test coverage. One example of their use in the context of lithographic variation is process corner identification.

Lithographic variation is prevalent throughout the wafer. The type and extent of lithographic fluctuation varies with location. Some area may have an increased exposure dose and some other may be out of focus. These variations can be random in nature and hence will end up producing dies that don't behave identically and also not have the same type of failures. Applying the same test pattern set to all the dies will not produce high fault coverage in many of them. Having process corner information will help identify the best test set to be used for dies that belong to a certain region on the wafer.

Test pattern optimization utilizing process corner information is always sort out for. One such method is to place a variety of control structures all over each die/wafer that can predict the current lithographic process corner. The variety comes from control structures that are drawn to vary with a particular type of lithographic variation. For example, a control structure dependent on CMP fluctuations can have alternating metal layers that are dense and isolated, so as to trigger changes in width and height of the feature polygons. Such changes can be used to trigger a probed output node which helps to identify the current lithographic process corner.

## VI. DIAGNOSIS AND MODEL CALIBRATION

Today's designs are mostly hierarchical using standard cells as building blocks and placement and routing of standard cells to implement overall design. The diagnosis of layout defects and layout fixes that are confined to standard cells tend to be somewhat different from diagnosis and fixes applied to inter cell defects. In standard cells, the layout tends to be compact, mostly at the minimum pitch and they are analyzed using detail lithography simulation to check for manufacturability compliance, where as detail litho simulation of cell interconnects is computationally infeasible and they are usually checked by approximate models which may result in errors in some instances. The defects inside standard cells tend to be more parametric in nature. Some of the defects in standard cells include non-rectangular gate transistors due to corner rounding, excessive line edge erosion due to etch overload, diffusion area rounding, contact resistance and stress induced defects due to contact placement locations. On the other hand, some of the examples of inter-cell defects are opens and bridges, line and via disappearances, stress voiding etc. These cases have to modeled and treated separately.

Traditional diagnostic strategies under silicon debug aims to identify hard faults such as opens and shorts. Diagnoses of soft-faults that lead to delay defects have not been studied extensively in the literature. With lithography induced defects having a larger impact than process defects for current and future technology nodes, increased occurrence of coupling capacitance, and resistive open faults can be observed. Effective soft-fault diagnosis calls for proper at-speed tests, targeted test patterns and most importantly, diagnostic resolution to identify each failing net. Also, with ever-present limitations in traditional physical failure analysis tools, it is important to provide a methodology to find the root cause of failing dies.

Linking the diagnosis data with layout information of all failed chips can be used in a productive way to locate physical hotspots in designs causing systematic defects, thus helping model calibration and yield improvement. There have been techniques that attempt to use this idea. Liu et.al. [9] and Mekoth et.al [8]

proposed methods show that using both logic netlist and layout information to be necessary to improve resolution. Using layout information, logically possible but physically infeasible nets/regions can be eliminated producing a reduced failure set. Layout regions that are feasible defect areas and also standard cell locations indicating within cell defects that can lead to stuck-on and stuck-open faults were reported. Another, layout aware diagnosis system to narrow the list of suspect candidates for open faults was proposed by Keim et.al. [8]. The method analyzes net topology to arrive at possible defect locations. It compares the layout of nets sharing common polygons. By means of region elimination, the suspected defect area is narrowed down to certain regions. This ability to reduce the number of potential defect sites can be fed back to the defect model to enhance its capabilities. These methods can be tuned to utilize lithographic variability information to produce far more pruned suspect regions.

## VII. YIELD IMPROVEMENT

Profitability of an IC product is tied to its manufacturing yield. Yield analysis during design phase permits changes during design, thus avoiding costly iteration through test silicon. If iteration through yield analysis is not included in design methodology, then the only available solution to improving yield is based on failure analysis that may result in either (i) recalibrating the manufacturing process based on its metrology or (ii) changes to the design. This process not only increases manufacturing cost, but also increases the time to market (TTM) of the product. Consequently, early stage yield analysis is preferred. The problems with yield analysis during design phase are (i) availability and fidelity of failure models, (ii) parameter fit for these models, and (iii) computational complexity to make yield analysis viable during design iteration. This requires creating models for each manufacturing process step that allow statistical failure prediction. The benefits of successful yield prediction are (i) reduction in manufacturing cost, (ii) time to volume manufacturing, and (iii) design co-optimization with area, performance and power metrics.

Traditional yield estimation methodologies have been based on particle defects. Critical area analysis is the most well known process yield estimator. As we move from process centric to lithography and design related defects, layout yield analysis has to incorporate impact of lithography, CMP and etch. Moreover, the analysis will have to layout specific and not to be generalized for a process setting. There are yield modeling solutions that incorporate lithography simulation and CMP. They use polygon linewidth and density respectively to predict the final yield of the mask. However, with an increasing number of problems arising in each mask layer, these models have to be constantly updated.

## VIII. CONCLUSION

Lithography related defects have become the dominant failure mechanism today. Simulation of manufacturing processes against physical designs result in clues about potential defects/locations. Such clues may be used to fix design or develop targeted tests. However, manufacturing process simulation needs both models and parameters. Models can be physical or phenomenological. The parameters for these models may be obtained from circuit-under-test by using special test structures that are highly sensitive to manufacturing process parameters.

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