Robustness Analysis of 6T SRAMs in Memory Retention Mode under PVT Variations

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Abstract— **Process variability is becoming a major challenge in CMOS design of general and embedded SRAMs in particular due to continuous device scaling. The main problems are the increased static power and reduced operating margins, robustness and reliability. A common way to reduce the static power consumption of an SRAM memory array is to decrease its supply voltage when in memory retention mode. However, this leads to a further reduction in memory robustness. The most common tool for statistical analysis of circuits under process variability is standard Monte Carlo simulation which has been proven to be too expensive when applied on an ultra dense SRAM [1]-[6]. In this paper a statistical robustness analysis method is proposed based on decoupling statistical integration from robustness region determination in the parameter domain. The robustness is estimated with a ~ 556X speed up relation to Monte Carlo and an error of ~ 1%.**

Keywords-6T SRAM;Robustness Analysis;Data Retention; PVT Variability.

I. INTRODUCTION

Increased process variability in nano-scaled technologies is becoming a major challenge for CMOS designers. Process variability, which can be classified as inter-die and intra-die, is due to the fabrication process and non-uniform conditions during dopant deposition or diffusion resulting in highly variable transistor parameters.

Because of its speed and compatibility with standard logic process, SRAM is the embedded memory of choice for many VLSI systems [7]. According to ITRS 2009, the density of SRAM could reach over 5 million transistors / cm^2, by 2015 [8]. In order to achieve the high density requirement, SRAM bit-cells are designed with minimum sized transistors, rendering them more sensitive to process variations. The major concerns regarding embedded SRAM memories and technology scaling are increased static power, lower cell stability and reduced operating margins, robustness and reliability [7].

Static power consumption is predominant in SRAMs. At the circuit level, leakage reduction can be achieved by controlling the voltage at different cores of the IC. By lowering the supply voltage (V_{DD}) of idle SRAM memory blocks to its standby limit, leakage power can be effectively reduced. In order to ensure cell stability, the lower limit of the supply voltage, must be higher than the *Data Retention Voltage* (*DRV*) determined for the nominal parameter cell because of process variability. Another factor that can affect SRAM robustness is the temperature. Depending on the proximity of the idle memory block to the active logic units, significant spatial temperature variation can be observed [9].

This paper analyzes statistically the effect of process, voltage and temperature (*PVT*) variability on the robustness of a 6T SRAM cell in data retention mode using an improved non-Monte Carlo method.

The next section presents an overview of commonly used statistical failure analysis techniques of SRAM memory under process variability. The third section describes in detail the proposed method of statistical analysis, and in the fourth the method is applied for robustness analysis of an idle 6T SRAM cell under process, voltage and temperature variation. The method is proven to be an efficient tool for circuit analysis when compared to other similar tools in the fifth section. Finally, the conclusion section summarizes the advantages of the proposed method and its applications for robustness analysis of 6T SRAM memory.

II. STATE OF THE ART

The most common tool for statistical analysis of circuits under process variability is standard *Monte-Carlo* (*MC*) simulation. Monte Carlo methods are a class of computational algorithms that rely on repeated random sampling to compute their results. Accuracy depends on the sample size, so for an extremely small probability events the number of random experiments to accurately estimate it is extremely large (sample size must be quadrupled to achieve twice the accuracy) [10].

Extensive research has been done to find methods to reduce sample size for speed improvement while maintaining the accuracy of standard Monte Carlo simulations. One such method is the *Stratified Sampling* technique which consists in stratifying the sample space by choosing a partition of the input parameter space. The integrals in each stratum are than estimated and combined to obtain the overall integral. Another common method in SRAM analysis is *Importance Sampling*. The idea behind this technique is that certain values of the input random variables have more impact on results than others. Hence, the basic methodology in Importance Sampling is to select a distribution which focuses on the important values. The use of biased distributions results in a biased estimator. The simulation outputs are weighted to correct the biased distribution to ensure that the new importance sampling estimator is unbiased. The issue in implementing importance sampling simulation is the choice of the biased distribution which emphasizes the important regions of the input variables.

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A good sample distribution can provide run-time savings and accuracy improvement [1, 3, 11, 10].

A widely used industry technique of parameter domain failure analysis is the *Most Probable Point (MPP)* [4, 12]. The failure probability estimation problem can be stated as finding the most likely variation point that causes the failure; that is, the point of maximum probability satisfying a certain failure criterion, i.e. *MPP*. The boundary between the acceptance and rejection regions is approximated by interpolation. It can be done by a first order approximation, finding the tangent line to the boundary that passes through the MPP, second order approximation, spline interpolation or rectangular approximation.

Another approach to parameter domain failure analysis is based on *Yield Estimation Nonlinear Surface Sampling* (*YENSS*) which was first proposed by S. Srivastava and J. Roychowdhury in [2] and then improved and presented by C. Gu and J. Roychowdhury in [5]. The method locates the failure region boundary in the parameter domain and determines the failure probability as the ratio between the area (or volume) outside the bounded region and that of the parameter domain.

S. Director, G. D. Hachtel in [16] introduces the simplicial approximation which estimates the boundary of the acceptable region in an N dimensional space as a polyhedron. In their approach the design centering problem is solved by determining the location of the center of the maximal hyperellipsoid inscribed within this polyhedron.

In [6], F. Gong et al. present a method to improve yield estimation efficiency, i.e. the *QuickYield* method, which proposes a yield surface boundary determination by surface-point finding and global search. Performance constraints are included into the differential algebra equation that describes the circuit, resulting into an augmented system equation.

This paper proposes a different approach to statistical robustness analysis in the parameter domain. The method is used to determine the failure probability of a 6T SRAM cell in data retention mode under Process Voltage and Temperature (*PVT*) variation. The method is described in detail in the next section.

III. PROPOSED METHOD

The essence of the proposed method consists in the decoupling between performance and statistics in the parameter domain. That is why it is hereafter referred to as ***SB-SI*** (***S****atisfiability* ***B****oundary* – ***S****tatistical* ***I****ntegration*). There is a range of values in the parameter domain for which the device satisfies the required performance. These values form the *Acceptance Region* while the remaining make up the *Rejection Region*. Robustness estimation is completed in two steps: first, the *Satisfiability Boundary* separating the Acceptance Region from the Rejection Region is found and second, a *Statistical Integration* over the two regions is performed to estimate probabilities.

A. Satisfiability Boundary (*SB*)

The Satisfiability Boundary is defined as the hyper-surface in the N dimensional space that separates the Acceptance Region (AR) from the Rejection Region (RR). The analysis is conduct in the parameter domain and the acceptance/rejection criterion is given by the circuit performance metric.

Assuming a circuit with N parameters ($\boldsymbol{p} = [\, p_1\ p_2 \cdots p_N \,]$) affected by variability and whose performance metric must have larger values than a certain limit specified by $Perf(\boldsymbol{p}) > P_{min}$. The two regions and the boundary between them are defined as follows:

$$AR = \{\boldsymbol{p} \mid Perf(\boldsymbol{p}) > P_{min}\} \quad and \quad RR = \{\boldsymbol{p} \mid Perf(\boldsymbol{p}) < P_{min}\} \tag{1}$$

$$SB = \{\boldsymbol{p} \mid Perf(\boldsymbol{p}) = P_{min}\} \tag{2}$$

where $\boldsymbol{p}$ is the N dimensional vector of the process parameters: $\boldsymbol{p} = [\, p_1\ p_2 \cdots p_N \,]$. In the parameter domain, the *AR* and *RR* are N dimensional hyper-volumes and the *SB* is composed of *N-1* dimensional hyper-surfaces.

The Satisfiability Boundary search can be very expensive and time consuming if done by means of simulation. This is why this paper proposes a method to estimate the ***SB*** by finding a set of boundary points (*Significant Points – SP*) and then interpolating to approximate the boundary surface with controllable error.

To simplify the explanation of the method, we first consider a circuit with two ($N = 2$) parameters (p_1 and p_2) subject to variability (Fig. 1). The figures in this subsection are obtained by analyzing a 6T SRAM cell in data retention mode and assuming that only two transistors parameters are affected by process variability.

In the parameter domain, the Satisfiability Boundary is approximated by a polygon whose vertices (hereafter referred to as *Significant Points (SP)*) are obtained by simulation. Evidently, the boundary is approximated more precisely with increasing the number of vertices. The first polygon obtained to approximate the Satisfiability Boundary in the 2D parameter domain is a quadrilateral. In this case, the SPs in this situation are determined by intersection between the **SB** and the parameter domain axes. If the obtained quadrilateral is not a good estimate for the boundary, an extra set of SPs will be added to the previous one. They are obtained at the intersection between the **SB** and the bisection lines (Fig. 1) – *First Angular Bisection (FAB)*. For a more accurate approximation of the **SB**, more significant points can be found by further bisecting the resulting angles (Fig. 3). For the two dimensional case the Significant Points (*SPs*) are determined by intersecting the satisfiability boundary with the segments given by the table in Fig.1. Assuming the parameter domain space defined by the parameter variation, the nominal parameter point ($p_{nom} = [\, p_{1nom}\ p_{2nom} \,]$) defines the origin of the system axis, i.e. the *[0 0]* point. The maximum and minimum values on the two axes are given by ($+\Delta_1$, $-\Delta_1$) and ($+\Delta_2$, $-\Delta_2$) respectively.

Once the directions are established, the intersection points are found using a searching algorithm. For this particular case, the *bisection method* was chosen for its robustness and simplicity. This method is applied separately to find each Significant Point of the Satisfiability Boundary. The number of directions, and consequently the number of simulations grows with increasing the number of parameters, i.e. the dimension of the parameter domain.

In the 2D case, the Satisfiability Boundary can be approximated by the polygon obtained when applying an

interpolation algorithm on the set of significant points (Fig.2). The first step to obtain the polygon is to find the adjacent points, which is intuitive for the two dimensional case but gets challenging for higher dimensions. The algorithm used in this work, which is extensible to the general N dimensional case, is described below for two dimensions.

In the *Quadrilateral Approximation (QA)*, the interpolation is straight forward, as the SPs are given by the intersection with the axes. For the first- and higher-order angular bisection approximations, the problem becomes more complex and an algorithm must be implemented. First, the extreme points in the parameter domain are mapped (+Δ values are mapped to 1 and -Δ values are mapped to -1), as shown in the table in Fig. 2. Starting the search from the [1, 1] point, half of the adjacent points are found by decrementing 1 for each variable and the other half is found starting from the [-1,-1] point and incrementing 1 in each direction as shown in the diagram of Fig.2.

Two points form a straight line. Thus, by connecting the adjacent points two by two the polygonal estimate of the Satisfiability Boundary is obtained (Fig. 2).

The general equation of a straight line is given by:

$$a \cdot x + b \cdot y = 1 \tag{3}$$

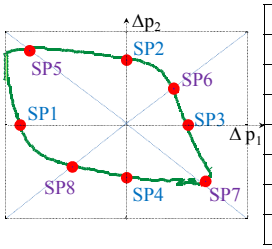
The a and b coefficients for each of the straight lines forming the polygon are determined by solving the system:

$$\begin{bmatrix} x1 & y1 \\ x2 & y2 \end{bmatrix} \bullet \begin{bmatrix} a \\ b \end{bmatrix} = \begin{bmatrix} 1 \\ 1 \end{bmatrix} \tag{4}$$

where *(x1,y1)* and *(x2,y2)* are the coordinates of two of the adjacent points.

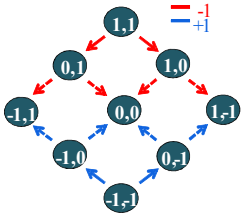
After obtaining the entire set of straight lines the boundary polygon (defined by the set of all a and b coefficients) is obtained (Fig. 3).

The quadrilateral approximation (4 SPs), and the first (8 SPs), second (16 SPs) and third (32 SPs) angular bisections are illustrated in Fig. 3.



[(0,0) (-Δ1,0)]	→SP1
[(0,0) (-Δ1, -Δ2)]	→SP5
[(0,0) (0,+Δ2)]	→SP2
[(0,0) (+Δ1, +Δ2)]	→SP6
[(0,0) (+Δ1,0)]	→SP3
[(0,0) (+Δ1, -Δ2)]	→SP7
[(0,0) (0,-Δ2)]	→SP4
[(0,0) (-Δ1, -Δ2)]	→SP8

Figure 1 – Choice of the Significant Points on the Satisfiability Boundary: First Angular Bisection (FAB)



SP1	→[-Δ1,0]	→[-1,0]
SP5	→[-Δ1, -Δ2]	→[-1,-1]
SP2	→[0,+Δ2]	→[0, 1]
SP6	→[+Δ1, +Δ2]	→[1, 1]
SP3	→[+Δ1,0]	→[1,0]
SP7	→[+Δ1, -Δ2]	→[1, -1]
SP4	→[0,-Δ2]	→[0, -1]
SP8	→[-Δ1, -Δ2]	→[-1, -1]

Figure 2 – Finding the adjacent Significant Points on the Satisfiability Boundary: First Angular Bisection (FAB)

An increase in the number of Significant Points results in improved accuracy of the boundary approximation but also in a larger number of simulations, that is, a longer estimation time.

Once the polygonal approximation of the **SB** is obtained, the acceptance and rejection regions are found. The condition that a random point in the parameter domain is in the acceptance or rejection region is given by

$$\begin{aligned} &(x,y) \in AR \; if \; for \; all \; (a,b) \;\; a \cdot x + b \cdot y - 1 < 0 \\ &(x,y) \in RR \; if \; for \; all \; (a,b) \;\; a \cdot x + b \cdot y - 1 > 0 \end{aligned} \tag{6}$$

The method is extended to the general case of N parameters subject to variability. The significant points on the **SB** are determined analogously, using the bisection method. Once the significant points are found, the **SB** can be approximated by a hyper-surface. N by N adjacent points must be connected similarly to obtain the hyper-surface estimating the SB.

Based on the above parameter domain partition, the robustness is determined by *Statistical Integration* ***(SI)*** as described below.

*B. Statistical Integration (**SI**)*

Assuming a multivariate distribution of N random variables, the joint (cumulative) distribution function is given by:

$$F(x_1, x_2, \cdots x_N) = P(X_1 \le x_1, X_2 \le x_2, \cdots, X_N \le x_N) \tag{7}$$

where $X_1, \ldots, X_N$ are the random variables under analysis and the probability density function is $f(X_1 \ldots X_N)$. The probability that the variables are between certain limits is given by

$$P(x_1 \le X_1 \le y_1, \cdots x_N \le X_N \le y_N) = \int_{x_1}^{y_1} \cdots \int_{x_N}^{y_N} f(X_1 \cdots X_N) dX_1 \cdots dX_N \tag{8}$$

The parameter domain is an N-dimensional hyper-rectangle. Given the complex shapes of the two regions (AR and RR), a computation strategy is required to determine the value of P in (8).

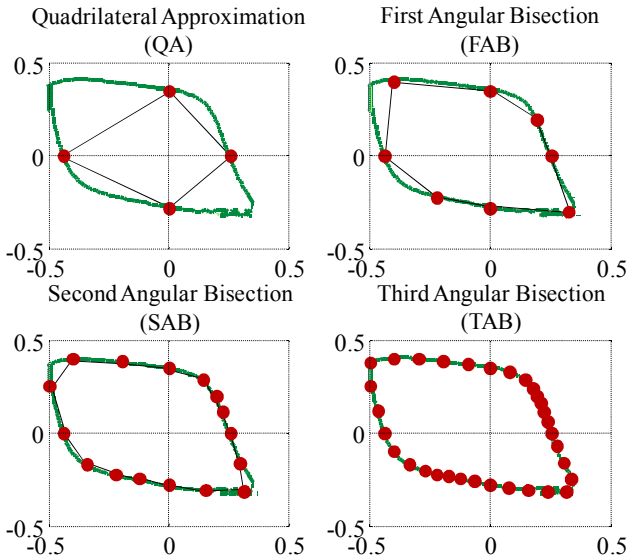


Figure 3 – The polygonal estimation of the Satisfiability Boundary for different levels of angular bisection

As integration over a regular, well defined space is straight-forward and it is relatively easy to consider correlation [13], the parameter domain must be divided into hyper-rectangles. Three regions are obtained, i.e. *Hyper-rectangle Acceptance Region* (*HAR*), *Hyper-rectangle Rejection Region* (*HRR*) and *Hyper-rectangle Satisfiability Boundary* (*HSB*) as shown in Fig. 4 for the two dimensional case. The partition is performed using a bisection-like method. The left side of Fig. 4 illustrates the first step of space division: each edge of the initial rectangle is divided in half and by connecting the resulting points, four rectangles are obtained. In order to determine to which of the three regions these rectangles belong, the positions of the vertices are checked using (6). The rectangles in *HAR* and *HRR* are left untouched, whereas those in *HSB* are further divided (Fig. 6) until the desired accuracy is reached.

- If all vertices are in the acceptance region, the rectangle (*R*) is in *HAR*.
- If all vertices are in the rejection region, the rectangle (*R*) is in *HRR*.
- If there are vertices both in the acceptance and rejection regions, the rectangle (*R*) is in *HSB*.

After completing the space division the statistical integration is performed by overlapping the parameter distribution of the parameter domain. By integrating the probability density function in each of the obtained rectangles using (8), the acceptance, rejection and boundary probabilities are obtained.

The following section describes the application of the **SB-SI** method for SRAM robustness analysis in data retention mode.

IV. Application to 6T SRAM

The robustness of the SRAM bit-cell in data retention mode is analyzed by using the **SB-SI** method, considering the effects of process, voltage and temperature (PVT) variability on its robustness.

A. Problem Statement

In order to reduce the static power consumption of an SRAM array in memory retention mode, its supply voltage is reduced to Data Retention Voltage (*DRV*). The DRV is the minimum supply voltage required for the SRAM to retain stored data. Its value is influenced by process and temperature variability.

The conventional way to analyze the robustness of a SRAM bit-cell is to quantify its immunity to noise. If the noise is represented by two opposite sign DC voltage sources at the internal nodes of the SRAM cell, the *Static Noise Margin* (*SNM*) is implied (Fig 5a).

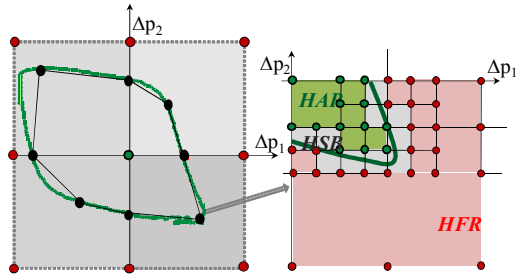


Figure 4 – Parameter domain division in rectangles

Graphically, the SNM is determined by drawing and mirroring the *Voltage Transfer Characteristics* (*VTC*s) of the two cross coupled inverters in the 6T SRAM cell, thus obtaining the so-called *Butterfly Curve*. The maximum square which can be inscribed in the loops of the butterfly gives the value of the SNM (Fig. 5b) [14]. Under random process variability, which causes asymmetry in transistor strengths, the butterfly curve becomes asymmetrical and the SNM is given by the smaller of the two maximum squares (Fig. 5c). The supply voltage also has a strong influence on the SNM as the butterfly curve shrinks down with decreasing the supply voltage, rendering the cell more sensitive to noise (Fig. 5d). The effect of the operating temperature is also illustrated in Fig. 5e, where a narrowing of the butterfly curve can be observed when the temperature increases.

Fig. 5 shows the importance of analyzing the robustness of the SRAM bit-cell in data retention mode considering the joint effects of process variability, supply voltage scaling and temperature variation.

The simulation environment is HSPICE and the SRAM cell is designed using 45nm Predictive Technology Model (PTM) transistors [15]. As the SRAM cell design is symmetrical, systematic process variability is significantly reduced by applying certain design rules, that is why only random process variability is taken into consideration in the present analysis. The combination of random dopant distribution and line edge roughness has an impact on threshold voltage variability. Assuming normal distributions of the threshold voltages of the four transistors, with a standard deviation estimated at σ=60mV [2] (for the 45nm transistor). Considering the large number of SRAM cells in a SRAM array, a 6σ upper bound in the variability range of the threshold voltage is a realistic assumption ($max|(\Delta V_{TH})|=360mV$).

The **SB-SI** method is applied to determine the robustness of an SRAM cell for different values of the supply voltage when all transistors in the SRAM cell are assumed to be affected by random process variability. As the analysis is conducted on a 6T SRAM cell in data retention mode, the access transistors are off. Hence, only four of the six transistors are included in the analysis. The four parameters defining the parameter domain are given by the variation of the threshold voltages: $\Delta p_{1\div4} = \Delta V_{TH1\div4}$. The performance metric under study is the Static Noise Margin (*Perf* = *SNM*). Two situations are examined: a) robustness when the **SB** is given by $P_{min}=SNM_{min}=0$ and b) robustness to noise levels lower or equal to ten percent of the supply voltage when the **SB** is given by $P_{min}=SNM_{min}=10\%V_{DD}$.

The Acceptance/Rejection Regions and Satisfiability Boundary are determined using (1) and (2). In order to approximate the satisfiability boundary, the bisection method is applied to find the significant points with a maximum absolute error of 1% for different supply voltages and temperatures. Starting from these points, the hyper-plane approximations of the **SB**s are determined by linear interpolation. The hyper-rectangular division is performed with a minimum absolute error of 0.1% (given by the maximum size of the hyper-rectangles on the **SB**). The robustness probabilities are determined and illustrated in Fig. 6 as a function of supply voltage and temperature.

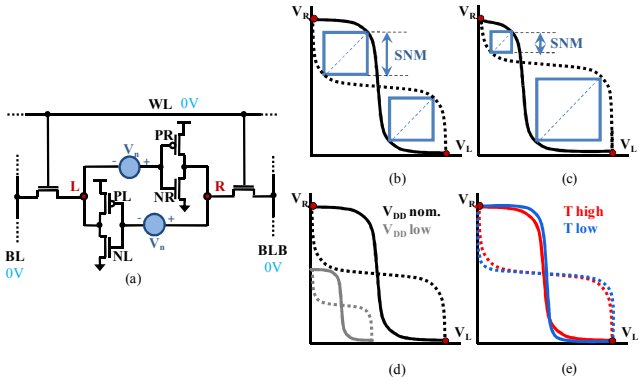


Figure 5 – (a) SRAM bit-cell in memorization mode, illustrating also the noise sources; Butterfly Curves: (b) nominal process parameters, (c) transistor strength asymmetry, (d) different supply voltages, (e) different temperatures

When the temperature increases from room temperature to 125°C the SRAM cell becomes less robust whereas the opposite effect is achieved when the temperature decreases to -40°C.

The **SB-SI** method finds the minimum value of the supply voltage for which the robustness requirements are met. Considering process variability (6σ distribution of threshold voltages), the minimum supply voltage for which the 6T SRAM cell under study is robust (i.e. retains stored data) is 360mV. If the robustness constraints are stronger, i.e. the 6T SRAM cell under study must be robust to any noise lower or equal to 10% of V_{DD}, the supply voltage must be maintained at minimum 410mV (Fig. 6).

V. ACCURACY AND SPEED

In this section the accuracy and speed of the **SB-SI** method are analyzed and compared to the results obtained by standard Monte Carlo simulations.

Both accuracy and speed are dependent on the number of simulations performed to obtain the satisfiability boundary.

The number of simulations is given by the number of significant points multiplied by the number of steps needed to obtain one significant point. The number of steps determines the accuracy with which the SPs are found.

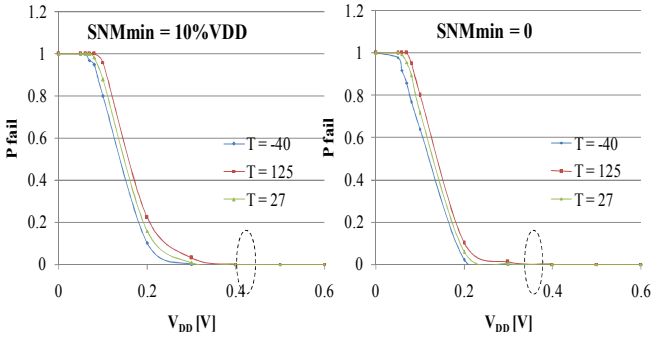


Figure 6 – Statistical robustness analysis for different supply voltages and temperatures

Evidently there is a tradeoff between accuracy and speed. The dependence of the accuracy of the polygonal approximation of the **SB** on the number of significant points is shown in Fig. 7. The Relative error is computed as the difference between the area occupied by the Acceptance Region and the area delimited by the polygon approximating the **SB** divided by the area of the Acceptance Region.

$$Relative\ error = \frac{A_{AR} - A_{polygon}}{A_{AR}} \quad (5)$$

Note that moving from *Quadrilateral Approximation* (QA) to *First Angular Bisection* (FAB), leads to a decrease of 63% in relative error at the expense of doubling the number of simulations. The increase in accuracy is less significant by moving to *Second Angular Bisection* (SAB) and *Third Angular Bisection* (TAB), and moreover the number of simulations keeps doubling. When the two curves are combined, the second approximation is found to be the optimal choice from both the accuracy and speed point of view.

The **SB-SI** method determines the statistical robustness of a 6T SRAM cell in data retention mode at room temperature for different values of supply voltage and levels of bisection. The results are summarized in Table I.

For the specific case of the 6T SRAM memory cell, the number of simulations needed for SB estimation can be reduced in the first- and higher-order angular bisections due to the symmetry of the cell. For example, in the first angular bisection, the number of significant points to be determined is 80, while considering the symmetry of the cell implies finding 52 significant points only, which translates into increased speed for the same accuracy.

The **SB-SI** method and Monte Carlo simulation data are compared. As expected, when the SB is approximated by a 2N vertex hyper-rectangle, the result is obtained more rapidly but with less accuracy, while the third angular bisection approach leads to the slowest but more accurate result.

Table II compares the SB-SI method with first angular bisection to standard Monte Carlo simulation for different values of the supply voltage.

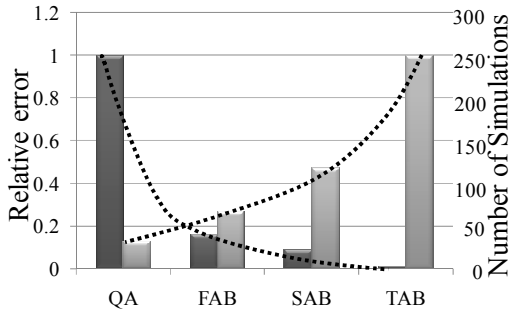


Figure 7 – Relative error and number of simulation according to the number of points found on the SB

TABLE I: STATISTICAL ROBUSTNESS ANALYSIS

SNM_{min} = 0V, T = 27C				
V_{DD} [V]	0.4	0.3	0.2	0.1
SB-SI Method	Probability of Perf < P_{min}			
2N vertices hyper-polygon	0	0.0214	0.1302	0.7384
1st angular bisection	*0*	*1.3e-4*	*0.0578*	*0.7161*
2nd angular bisection	0	1.29e-4	0.0578	0.7162
SNM_{min} = 10%V_{DD}, T = 27C				
V_{DD} [V]	0.4	0.3	0.2	0.1
SB-SI Method	Probability of Perf < P_{min}			
2N vertices hyper-polygon	1.1e-3	0.0361	0.2463	0.8903
1st angular bisection	*0.61e-4*	*0.0059*	*0.1583*	*0.8794*
2nd angular bisection	0.61e-4	0.006	0.1583	0.8791

TABLE II – ACCURACY AND SPEED (SNM_{min}=10%V_{DD})

V_{DD} = 0.4V, T = 27C			
Method	P	Error	Speed up
Monte Carlo (500k)	0.62e-4	-	-
***SB-SI** 1st angular bisection*	*0.61e-4*	*1.63%*	*556X*
V_{DD} = 0.3V, T = 27C			
Monte Carlo (500k)	6.01e-3	-	-
***SB-SI** 1st angular bisection*	*5.9e-3*	*1.83%*	*555X*
V_{DD} = 0.2V, T = 27C			
Monte Carlo (500k)	*0.1599*	-	-
***SB-SI** 1st angular bisection*	*0.1583*	*1%*	*556X*

VI. CONCLUSIONS

The paper presents the **SB-SI** method of statistical robustness analysis based on finding the boundary separating the acceptable performance region (**SB**) and the rejection region in the parameter domain and then statistically integrating (**SI**) the probability density function over the rejection region. The method is applied for robustness estimation of a 6T SRAM cell in data retention mode, under process, voltage and temperature variation. The **SB-SI** method is demonstrated to be accurate and fast when compared to the standard Monte Carlo simulations. If required its accuracy can be easily improved by increasing the number of significant points to be determined on the satisfiability boundary and the accuracy with which these points are found (though this method offers only slight increase in accuracy), and by further dividing the *HSB* region.

As an application of the **SB-SI** method, the robustness of a 45nm PTM 6T SRAM cell in data retention mode is estimated for different supply voltages and temperatures. The minimum supply voltage that can ensure data retention and certain robustness can be accurately determined by plotting the two metrics. For the particular case of the 45nm PTM 6T SRAM cell used in this analysis the minimum supply voltage for which data is retained is 0.36V under process and temperature variability.

The robustness probability results are in good agreement with those obtained by standard Monte Carlo simulations. In addition a considerable speed up is achieved. The proposed method is general and applicable for robustness estimation of SRAM in other modes and circuits with well characterized performance metrics in the parameter domain.

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