Challenges in Designing High Speed Memory Subsystem for Mobile Applications

Tsunwai Gary Yip, Philip Yeung, Ming Li and Deborah Dressler
Semiconductor Business Group
Rambus Inc.
Sunnyvale, California 94089 USA

***Abstract*—Some constraints imposed on the design of components for mobile devices are the size of the handheld device, safety for handling, heat dissipation, and in-system electromagnetic interference. This paper discusses challenges in designing the next generation low power DRAM subsystem operating at multi-gigabits per second. A new mobile DRAM interface that can meet the challenges and some test data are presented.**

Keywords-low power DRAM; thermal; EM emission; high data rate; package-on-package; mobile phone

I. Constraints on Designing Handheld Devices

Volumetric Constraint - Upon the introduction of 3.5 inch touch sensitive displays in 2007, the trend of reducing the size of mobile phones was reversed. While smaller phones, roughly 100 mm x 50 mm x 12.5 mm, are still common, smartphones have become as large as 120 mm x 66 mm x 11.5 mm to accommodate a 4.3-inch touch sensitive display. The extra area is also used to accommodate a larger battery to extend operation time. According to this study of recently introduced phones and from last year [1], active electronic components are confined to 13% or less of the volume of a phone.

Safety - The surface of a handheld device must not exceed 40°C for safety and comfort [2]. Among all active components in a mobile phone, DRAM memory has the lowest maximum operating temperature, typically 85°C [3]. The 45°C difference and the available external surface area for heat dissipation together set the limit for the power consumption of each mobile phone.

Heat Dissipation – Active cooling is not used in handheld systems due to volumetric constraint, acoustics, and the extra power consumption. Almost 75% of the heat generated in a mobile phone is conducted to the hand of the user; the remaining is dissipated by convection and radiation to the environment [1, 2]. For a small candy-bar phone with a size of 100 mm x 50 mm x 12.5 mm, 2 W is the upper limit of heat dissipation. The limit is 2.65 W for a large smartphone with a 3.5 inch display. These limits are based on 40°C for safety and comfort of human hand, and 30°C for the ambient air.

II. New Challenges in System Design

A package-on-package (PoP) configuration is common in phones to reduce the foot print area of the memory and processor packages. In feature phones, a flash memory package is stacked on top of a baseband processor as shown in Figure 1. In smartphones, a DRAM-Flash memory package is on top of an application processor. Some smartphones have both kinds of PoPs.

Area savings from using PoPs has led to two new design challenges at the system level. Compared to the side-by-side layout of processor and memory packages, stacking the packages increases power density, that is, more heat is generated over a smaller area. A more effective heat spreading mechanism is needed to distribute the heat from the smaller area of a PoP to the surface of the phone.

The second design challenge is the electromagnetic radiation from the stacked memory and processor packages. The impact of the radiation will go up as the speed of DRAM goes from the current data rate of 400 Mbps up to multi-Gbps, and processor frequency from 1 to 2 GHz. A solution to reduce EM emissions is urgently needed.

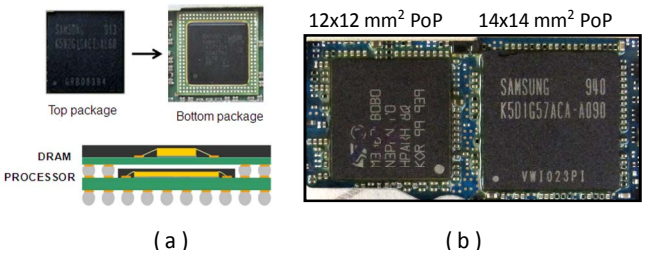

Figure 1. PoP structure and dual PoP in a smartphone.

III. Relief for Thermal Constraint

The thermal constraint of a PoP can be relieved by reducing the thermal resistance in the heat flow paths and the power consumed by the DRAM and processor. 1.2 W is the upper limit of continuous heat dissipation for a PoP [1]. Industry roadmaps suggest that 28 nm processors operating at 1 to 2 GHz could be lowered to 0.5 ~ 0.7 W. The DRAM limit would be 0.5 ~ 0.6 W. According to this estimates, the characteristics of the heat flow path between a PoP and the surface of a mobile phone are described in Figure 2.

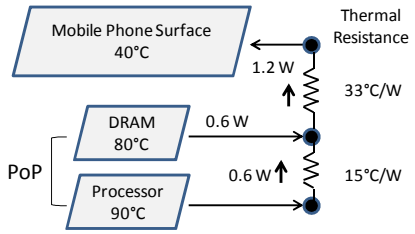

Figure 2. Characteristics of steady state heat flow path in mobile phone.

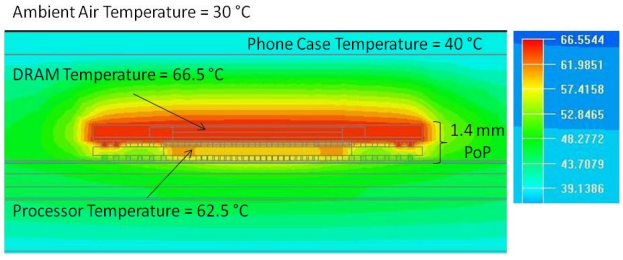

Figure 3. Temperatures of DRAM.

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Designing a thermal solution to meet the temperature limits of DRAM and processor is not difficult. The simulation results in Figure 3 suggest that both the DRAM and processor will have significant thermal headroom.

To prevent the DRAM silicon from reaching 80°C, the memory package is made as thin as possible to reduce the thermal resistance between the DRAM silicon and phone surface. This feature can be found in the cross-section of a PoP shown in Figure 4. The height of the PoP is 1.4 mm. The top package contains a DRAM die and a flash memory die, and is only 500 µm thick.

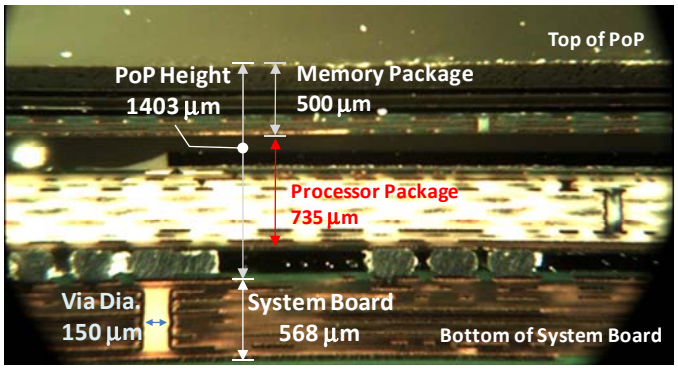

Figure 4. Thin top package (500 µm) in a 1.4 mm PoP for smartphone.

IV. Low Power & Low EM Emission High Speed Memory

As more functions of consumer electronics are packed into a mobile phone, the bandwidth of the memory subsystem is expected to exceed 5 gigabytes per second in two years. At this data rate, the upper power limit of 0.6 W for DRAM in a PoP is not easy to meet.

New low power architecture for the DRAM interface has been developed to meet this challenge. The interface is implemented in a PoP as shown in Figure 5. References [4] and [5] provide the details of the circuit design that implements the new memory interface. Test data of the prototype suggests that the new architecture implemented on 28 nm process can deliver the required bandwidth while satisfying the power consumption limit.

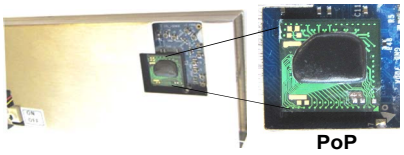

Figure 5. Prototype of 3.2 Gbps interface in a 12mm x12mm PoP.

The new interface uses a 200 mV differential signal with a common mode of 100 mV. The very low swing at near ground reduces the energy it takes to transfer data while enabling the interface to run 8 times faster than the current generation of mobile DRAMs. Figure 6 shows the PRBS differential data eye at the receiver of the low power interface during a WRITE operation. Power consumption is at 2.2 mW/Gbps. The fast data rate allows for low pin count and thus significant savings in area.

To further lower the power consumption of the DRAM, the calibration and timing circuitry are placed in the controller. This greatly simplifies the design of the DRAM interface. The clock is forwarded and distributed to both the controller circuit blocks and the DRAM device from a central PLL located in the memory controller PHY. A PLL and/or DLL are not needed on the DRAM, thus lowering power consumption.

Current mobile DRAMs employ single-ended signaling that can generate significant levels of electromagnetic emission. Figure 7 shows that the emission by single-ended signals in a smartphone is significantly higher than that of the new fully differential interface. The new DRAM interface is not expected to interfere with other RF components if shielding is properly installed over the PoP.

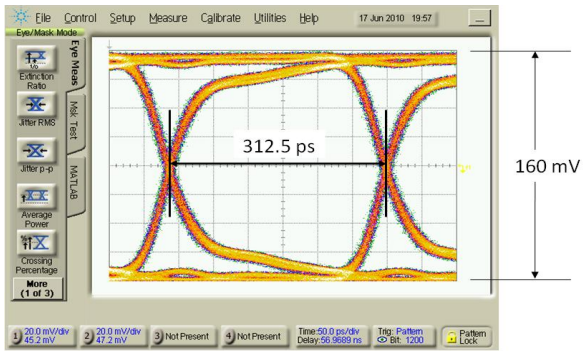

Figure 6. Very low swing differential signaling at 3.2 Gbps.

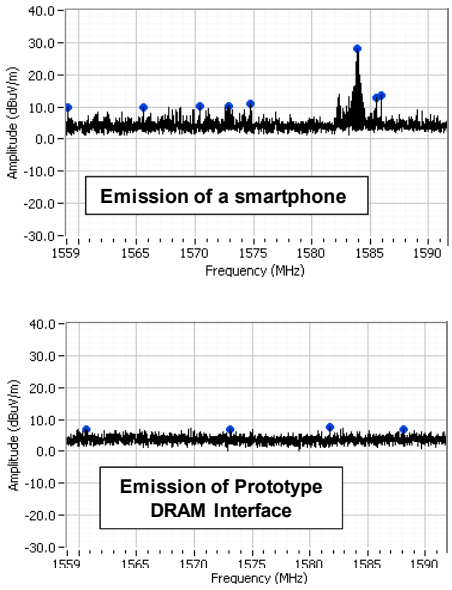

Figure 7. Comparison of EM emission in 1575.2 MHz GPS frequency band.

V. Conclusion

The new low power DRAM interface will allow mobile devices to use a high bandwidth memory subsystem without violating the thermal limits for reliable operation and safe handling. The new architecture will reduce the power consumption and electromagnetic radiation of future multi-gigabits per second mobile memory.

References

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