Power Management Verification Experiences in Wireless SoCs

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Abstract— **We look into the validation a power managed ARM Cortex A-8 core used in SoCs targeted for mobile segment. Low Power design techniques used on the chip include clock gating, voltage scaling, and power gating. We focus on the verification challenges faced in designing the processor core including RTL modeling of power switches, isolation, and level-shifting cells, simulation of voltage ramps, generation of appropriate control signals to put the device into various power states, and ensuring correct operation of chip in these states as well as during the transitions between these states.**

Keywords- low power, verification, power gating, dynamic volatage scaling, power switches, isolatio, ARM Cortex A-8

I. INTRODUCTION

Power management is important not only for improving battery life of products targeted to wireless, automotive, and consumer electronics markets but also for optimizing meantime between charging and system costs for battery operated devices. In addition, it plays an important role in avoiding high failure rates in devices as well as in reducing cooling costs for products that require high performance.

In this paper, we focus on the power management architecture verification experiences of Wireless SoCs and specifically on the tasks for validating a power managed ARM Cortex A-8 core [1] used in SoCs targeted for mobile segment. The low power ARM core includes power management for various key functional areas on chip including the debug unit, the main core with fetch, decode, execute, and load-store modules, and the NEON SIMD engine for multimedia processing as the three main power domains. There are six main power states of the chip including all powered up and all powered down states. Power techniques used on the chip include clock gating, voltage scaling, and power gating [2-6]. We focus on the verification challenges faced in designing the processor core including RTL modeling of power switches, isolation, and level-shifting cells, simulation of voltage ramps, and generation of appropriate control signals to put the device into various power states.

The power management verification strategy was put in place with following goals in mind:

- Ensuring the intent of power-aware design is implemented per its architecture definition.
- Correct sequencing of control signals during the switching and scaling of power supplies
- Correct input and output functionality of each power domain during the power cycles
- Coverage of all power states and all legal transitions between these power states

Some of the specific verification issues encountered and to be discussed here include the following:

- Ensuring that each of the domains are clamped correctly in all valid power states of the chip
- Ensuring level-shifters and level shifting clamps are correctly placed and validated for presence of different voltages and clock frequencies associated with the power domains
- Issues with voltages on level-shifters corrupting signals across domains
- Delay dependent issue with isolation resulting from voltage ramp times
- Un-initialized registers & memory contents on each power cycle corrupting downstream logic

We conclude the paper by highlighting the need for defining power intent early in the design cycle and maintaining it throughout the flow with necessary checks at each stage of the design cycle.

II. POWER MANAGEMENT VERIFICATION

A. Voltage-Aware Modeling of the Power Switch

Accurate power-up and power-down voltage ramps (Figure 1) must be modeled for effective power-aware simulations. A voltage regulator usually has a source power supply (connected to AC mains, Battery, or another voltage regulator), an output "regulated voltage", digital control bits to set the voltage or turn the regulator on/off, and some status/handshake signals to indicate stability of output. From the power management verification point of view, the interaction of power management state and voltage regulation scheme must be captured in the verification infrastructure.

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FIGURE 1: High-level Modeling of Power Switches

Such a modeling of the power switch allows issues such as a clock wiggling during power shut-down process and delay dependent isolation and other issues to be visible during simulation-based verification process.

B. Processor's Power State Table

The power domains can be independently controlled to give combinations of possible power states on the chip. The six valid power states resulting from powered-up and powered-down domain combinations are listed in Table I.

The processor can accommodate many different levels of static, or leakage power management. All of these techniques are specific to a given implementation of the processor. In this implementation, we worked with power gating of the Core, Debug, and NEON domains as well as full retention by saving all architectural state to memory.

C. Typical Power Management Verification Issues

The key to verifying a power-managed processor's functionality is to ensure that the processor functions well in each of its power modes and the transitions to these power modes are done correctly. In the context ARM Cortex-A8, this amounts to verifying scenarios such as: i) NEON powers up correctly while the processor is in reset and when processor is not in reset, ii) Debug domain is powered down and powered up correctly, iii) Powering down the core power domain, iv) Powering up core and NEON together, and several other such Cortex power architecture scenarios.

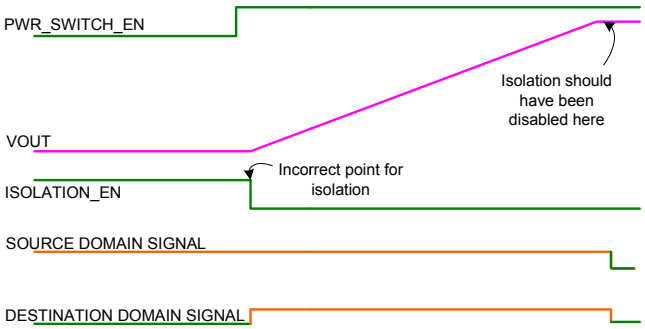
Each of these scenarios follow a specific protocol related to the domain clocks and other power control signals and the verification process must ensure that the sequence of events described in these protocols are exhibited correctly in processor's implementation.

For example, to ensure that Debug is powered down correctly, the clocks going to the debug unit should be on a separately controlled and shared power supply. In addition, the outputs of debug unit must be clamped to benign values while powered down to indicate that the interface is idle. And not only the isolation/clamping of signals get the desired value but they must also occur correctly in relative timing order of events. The isolation control can be enabled either before or after it really needs and that may lead to various issues. Figure 2 shows a situation where isolation was disabled at the same time when the power switch was enabled and, as a result, this did not account for the voltage ramp up time and led to functional issues.

TABLE I. PROCESSOR DOMAINS AND STATES

Power States	**Processor Power Domains**		
	Core	***Debug***	***Neon***
All Power Down	Down	Down	Down
Debug Mode	Down	Up	Down
Core Mode	Up	Down	Down
Core Debug Mode	Up	Up	Down
Core Neon Mode	Up	Down	Up
All Power Up	Up	Up	Up

FIGURE 2: Generation of isolation control signal didn't account for voltage ramp up time corrupting outputs



We will look at several such issues in the power management verification of ARM Cotex-A8 processor that highlight the need for defining power intent early in the design cycle and maintaining it throughout the flow with necessary checks at each stage of the design cycle.

III. REFRENCES

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