

An Analytical Compact Model for Estimation of Stress in Multiple Through-Silicon Via Configurations

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Abstract

We present a compact model that provides a quick estimation of the stress and mobility patterns around arbitrary configurations of Through-Silicon Via's (TSVs). No separate TCAD simulations are required for these configurations. It estimates nFET and pFET mobility for industry-standard as well as for (100)/<100> substrate orientations.

As the model provides mobility info in less than 0.1 millisecond/transistor/TSV, it is possible to be used in combination with layouting tools and circuit simulators to optimise layouts of circuits for digital and analog applications. The model has been integrated into the 3D PathFinding flow, for steering 3D IO placement during stack definition.

Introduction

The stress patterns around TSV's are considered as an important concern for 3D integration, as this leads to additional variability in MOSFET mobility, threshold voltage, and drivability [1]. As a consequence, Keep-Out-Zones (KOZ) are defined around the TSV, within which the added variability becomes unacceptably high.

The KOZ is typically determined by either experimental measurements (measure the mobility/on-current change versus distance-to-TSV) or through TCAD simulations. While this approach works well for a few TSV's, actual designs may feature thousands of TSV's in complex configurations. Therefore, design layout tools may benefit from an analytical model that predicts the stress around arbitrary TSV configurations in a fast and accurate way.

Details of the Compact Model

The proposed compact model starts from the stress pattern around one TSV, simulated by TCAD (Fammos, [2]). This abstract focuses on the simulation of a 5-micron radius Cu TSV, using experimentally measured mechanical properties for copper, and giving good quantitative agreement with experimental results [1]. The three stress components (radial $\sigma_{Rad.}$, tangential $\sigma_{Tang.}$ and out-of-plane $\sigma_{Vert.}$, see Figure 1) versus distance-to-TSV is the only required input for the compact model.

Using the distance d and angle α between a transistor and a TSV, the stress components σ'_{xx} , σ'_{yy} and σ'_{zz} in the transistor can be calculated as:

$$\begin{bmatrix} \sigma'_{xx} \\ \sigma'_{yy} \\ \sigma'_{zz} \end{bmatrix} = \tilde{L} \cdot \begin{bmatrix} \sigma_{Rad.} \\ \sigma_{Tang.} \\ \sigma_{Vert.} \end{bmatrix} \quad [1]$$

with $\tilde{L}$ a matrix taking the tensor rotation of $\sigma_{Rad.}$, $\sigma_{Tang.}$ and $\sigma_{Vert.}$ to the transistor's reference frame into account.

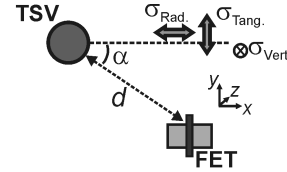


Figure 1. Top-view drawing, showing the position of one TSV versus an nFET/pFET.

The total stress for multiple TSVs is then obtained by combining the stress for all TSVs:

$$\sigma_{ii} = f(\sigma'_{ii,TSV1}, \sigma'_{ii,TSV2}, \sigma'_{ii,TSV3}, \dots) \quad [2]$$

for $ii=xx, yy$ or zz .

Knowing the stress components in the x , y and z direction, the mobility change can be estimated using the appropriate piezoresistance coefficients [3]:

$$\delta\mu / \mu = \tilde{\Pi} \cdot \vec{\sigma} \quad [3]$$

with $\vec{\sigma}$ a 3x1 vector containing the stress components, and $\tilde{\Pi}$ a 3x3 piezoresistance matrix, dependent on wafer orientation and the transistor type (nFET or pFET). Both for (100)/<110> (industry standard) and (100)/<100> wafer orientations, piezoresistance theory predicts no dependence of mobility on shear stress [4], therefore calculation of shear stresses has been omitted in Equations [1-2].

Results

Figure 2 shows the input used for the compact model: stress versus distance to a single TSV, simulated by TCAD (Fammos) for two different TSV modules, leading to different stresses. The out-of plane stress was found to be negligibly small for the configurations under study.

Using the above input, the pFET mobility change around a single TSV is shown in Figure 3. Depending on the location of the transistor, the mobility is degraded or improved around the TSV.

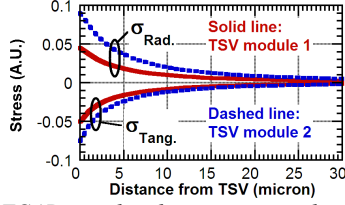


Figure 2. TCAD-simulated stress versus distance to a single TSV, used as input for the compact model.

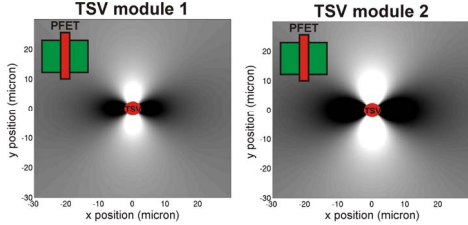


Figure 3. PFET mobility change around a single TSV for pFETs oriented in the x (left) and y (right) direction.

The compact model allows quick estimation of the KOZ around any TSV configuration, as is demonstrated for a 4-TSV arrangement in Figure 4. The combined effect of the TSVs leads to KOZ sizes in the order of 50 micron for TSV module 1 and 60 micron for module 2, indicating that optimization of the TSV module is an important parameter to reduce the KOZ.

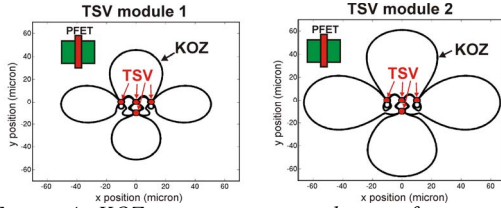


Figure 4. KOZ estimation around a configuration of four TSV's, using TSV module 1 (left) and 2 (right).

Figures 5 and 6 illustrates one of the important issues for TSV scaling: reducing the distance between TSVs does not change the KOZ significantly, neither for column (Figure 5) or matrix configurations (Figure 6).

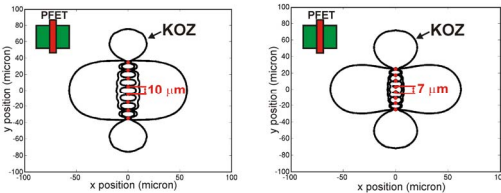


Figure 5. KOZ estimation for a column of 8 TSV's using TSV module 1. The distance between TSV's is either 10 micron (left) or 7 micron (right).

While the compact model can easily be used to generate KOZ's like in Figures 4-6, its goal is also to provide a fast interface for layouting tools, where the effect of TSV proximity is needed only at specific locations-of-interest. Starting from the TCAD-simulated profile of Figure 2, the compact model has been implemented in a freeware

software language. Even without aiming for speed in the current implementation, the model calculates the effect on mobility within less than 0.1 millisecond per transistor and per TSV on a standard Linux workstation, much faster than what is possible with TCAD.

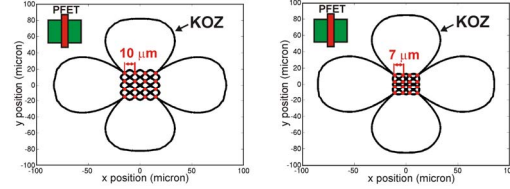


Figure 6. KOZ estimation for a matrix of 4x4 TSV's using TSV module 1. The distance between TSV's is either 10 micron (left) or 7 micron (right).

We use the mechanical model to decide on the optimal 3DIO placement when defining the 3D stack in the early phases of the system design. Hereto, we have integrated the mechanical compact model into the PathFinding flow [5]. As an illustration, we demonstrate a DRAM on logic stack definition in Figure 7. A virtual physical design is created for both logic and DRAM tiers. An array of TSVs in the middle of each die connects both tiers. We use the mechanical model to estimate stress around the array of TSVs, use this info to define the KoZ and in this way optimize the floorplan.

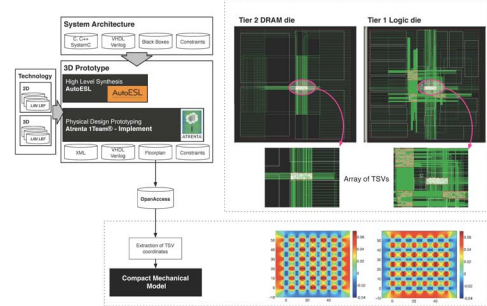


Figure 7. Schematic of the integration of the mechanical compact model into PathFinding design flow.

Conclusions

Compact models for fast stress estimation around TSVs are helpful to automatically optimise TSV and transistor placement. This compact model starts from the stress pattern around a single TSV, which has been calibrated with experimental data. The stress pattern is then rotated and combined for multiple-TSV configurations. The model shows adequate agreement with TCAD and is significantly faster.

Using the model, it has been demonstrated that the TSV module is an important parameter to reduce the KOZ. On the other hand, scaling the TSV-to-TSV spacing cannot be used to obtain smaller KOZs.

References

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