Smart Imagers of the future

Antoine Dupret, Michael Tchagaspanian, Arnaud Verdant, Laurent Alacoque and Arnaud Peizerat
CEA-Léti MINATEC
38000 Grenoble, France
(firstName.lastName)@cea.fr

Abstract—**This paper presents the evolutions of CMOS image sensors. From the early works, highly image processing oriented, the main research effort has then emphasized on image acquisition. To overcome the rising limitations of standard approaches and to promote new functionalities, several research directions are underway with promising results.**

Keywords-image sensors; vision chips; imagers; 3D technology

I. INTRODUCTION

First, let recalls one key issue: prior any image processing, it is of most importance to acquire image. Charge Coupled Devices (CCD) technology has been the workhorse technology of image acquisition from the 60s' to the early years of the millennium. The principle of CCD is rather simple: photoelectric effect generates charges that are accumulated in the photo sites during the integration time. Then, these charges are shifted from site to site by applying successive voltages onto the CCD gate array (Figure 1.). CCD is therefore a very specific process, optimized to transfer charges: in high ends CCDs less than one electron over one million is lost during the transfer of a whole image. This performance is obtained at the expense of high voltages applied to the MOS capacitors constituting the sites of the CCDs, and consequently it results in high power consumption.

In spite of CCDs performances in image acquisition, the mid 80s' have seen the beginning of CMOS technology as an alternative. Indeed, CMOS features processing capabilities that can not be implemented using CCD. Interestingly, one of the very first CMOS optoelectronics circuits was Lyon's optical mouse [1]. This 4×4 array of photodiodes circuit was chiefly an optoelectronic motion detector. Yet Lyon pioneer's works has settle some of the fundamental aspects of design methodologies for image sensors, i.e. use of very simple and conservative devices, mixing analog and digital circuits. Since that time, the design of image sensor has evolved with the demand for, first of all, pixel numbers for Digital Still Camera, and secondly for higher performances or functionality. Pushing further the functionalities leads naturally to the concept of Vision Chips. Developing on-chip functionalities was the first to raise the interest of academic researches while image acquisition has seen a growing interest almost a decade later.

In this paper we will first recall the pioneer works and we will analyze why their impact is not perceptible in today's circuit. We will then present why image acquisition is challenging and then, from the limits of image sensors, what the trends are for next generations of image sensors.

978-3-9810801-7-9/DATE11/©2011

II. A TRIBUTE TO THE PAST: ELECTRONIC RETINAS: THE QUEST FOR SEEING SILICON

A. Biomorphic chip

The early works on neural networks have led many researchers to work on dedicated integrated neural networks circuits. In this field of investigations, Carver Mead is reckoned to have designed one of the very first neuromorphic Silicon Retina [2]. Derived from what exists in distal layers of the vertebrate retina, i.e. the cones, the horizontal cells, and the bipolar cells, his basic idea was to combine the image acquisition circuit next to the image spatial filtering implemented thanks to a resistive grid.

The main motivation of these works was to propose alternatives to classical computation paradigms. To some extents, nowadays works such as the [3] or [4] are the legacy of Carver Meads initial works. Although the CNN paradigm does refer directly to neuromorphic computation, the works of Rodriguez-Vazquez (e.g. [5]) and some others have several common points with this early realization.

B. Massively parallel optical input image processors

Far from the biological inspiration, the Francis Devos' and Bertrand Zavidovique's works were based on an algorithmic approach. Considering the integration densities of the MOS technologies of the 80s, their processing were based on simple Boolean operations. From their works, they have developed one of the very first programmable retina (65×76 pixels)[6]. In this retina the image was binarized at pixel level, and then processing is performed by a succession of Boolean operations within each pixel. It has enabled a successful implementation of edge detection, motion detection, and halftoning.

Apart of the concept of massively programmable, yet simple, processors, one of the interesting ideas was to use the projection of images on the Focal Plane Array to achieve highly parallel input ports, even used to retrieve random signals [7]. Nowadays, jointly designed by ENSTA and CEA-Léti team, the smart image sensor in Caladiom from Bertin technology can be considered as the ultimate evolution of those early works [8].

C. What were the limitations?

These initial works have led to very interesting compact operators, even for very complex algorithms (e.g. stochastic algorithms in [9] or [10]) compatible with on-chip image

processing. They have contributed to explore concepts such as fine grain processing or spikes computing, and some of these concepts are still under investigation.

In spite of the initial interest that these works have aroused, they had very little impact on commercial circuits. Indeed, in those silicon retinas, the pixels required tens of transistors, resulting in too large pixel to enable practicable resolution for which a parallel processing would have been meaningful. Yet, the pixels were still too small to allow more than very specific processing capabilities. Even worst, with the down scaling of CMOS process, these simple processing capabilities were at the reach of dedicated digital architecture or even of on the shelf processors [9]. Finally, the area of the photosensor itself was small with respect to the pixel area, leading to a reduced sensitivity. Hence, the lightening conditions were too limited to lead to useful devices. Conversely, offering very robust, very cost effective solutions, especially with the growing processing capabilities of either on the shelf digital processors and optimized FPGA designs, CCD associated to digital processors has long dominated the image processing world. Moreover, the good image quality of image under various illuminations strengthens this approach. Yet, thanks to its processing capacities, CMOS technology has slowly but dramatically conquest the imager market.

III. IMAGERS: YET A COMPLEX SYSTEM ON A CHIP

A. Image acquisition: a not so simple task

In the early years of the new millennium, the main breakthroughs have been brought by the cameraphone applications. This application is very demanding in terms of costs, which is given by the ¼ inch silicon area. Yet the format must be ever larger which implies to reduce the pixel size while preserving the image quality. Hence, image acquisition has to face several hard constrains.

TABLE I. TYPICAL SCENES ILLUMINATIONS

Scene	Outdoor, full moon night	Outdoor, street at night	Indoor, apartment	Outdoor, sunny day
Illumination (lux)	0.5	20 - 70	200 - 400	50,000 – 100,000

Let's point out some figures and establish the connection between the illumination and electrical quantities. Some typical illumination values are given TABLE I. The sensitivity of a pixel is proportional to the quantum efficiency (QE) and the Fill Factor (FF). The FF is the ratio between the sensitive area and the pixel area. The quantum efficiency QE is defined as the ratio between the generated electrons (é) to the number of incoming photon. For the sake of simplicity, we can consider the global quantum efficiency, i.e. from the lens to the junction that we will refer as Quantum Effective Efficiency (QEE). Typical QEE values are around 40%. From the designer point of view, the only way to increase sensitivity is to increase the Fill-Factor, i.e. to drastically reduce the number of transistors per pixel.

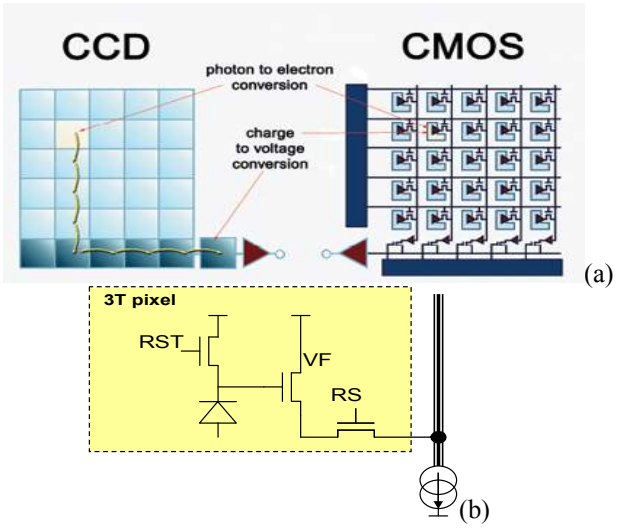

Figure 1. Architectures of CCD and CMOS Imager (a), and focus on the 3T pixel architecture (b)

From TABLE I. and considering a typical sensitivity of 5000é/lux, the photocurrent is between 0.4fA and 95pA. The only practical way to handle such small currents is to integrate it over time in a capacitor. This capacitor introduces a charge to voltage conversion. The conversion gain is typically around 60µV/é. The maximum supply voltage, typically 1.8V, limits the amount of charges to less than 10ké. This leads to the conceptual imager architecture, given Figure 1. and to the 3T pixel architecture (Figure 1. The RST transistor sets the initial voltage. When the RST transistor opens, the reverse diode capacitance is discharged by the photocurrent. The VF transistor is a used as a unity gain amplifier while the RS transistor is the classical Row Select Transistor used to read one selected pixel.

The amount of charges is quite low and several effects impair this low amount of charges. Some of these effects may be fixed by a proper design:

- Signal to Noise Ratio (SNR): The photodiode and the MOS transistors introduce noises ([12], [13]). The maximum amount of charge is limited by the dark current (thermally generated), leading to a dead amount of charges Q_{obs}. The signal to noise ratio is then given by: $SNR=20\ log((Q_{Max}-Q_{obs})/Q_{noise})$. Nowadays imager feature SNR about 70dB. This means a noise level less than 3é ([14]).
- FPN: the devices are subject to mismatch. Hence, the mismatches produce a noisy image, referred as Fix Pattern Noise (FPN). To avoid a costly frame memory, the FPN is removed using Correlated Double Sampling (CDS) techniques.
- kTC: The reset of the photodiode introduces a *kTC* noise: during the reset phase, the reset transistor is used as a switch that adds noise: $Q_n^2=k\,T\,C$, with k, Boltzmann constant, T, the temperature and C, the integration capacitance. Since this noise is stored at the end of the reset phase, it can also be suppressed using CDS techniques.

Yet, the need for keeping noise performance about 70dB has lead to add specific steps to the standard CMOS process in order to get a pinned photodiode. This diode can be fully depleted, which suppresses the *kTC* noise by having no free charges when being reset (i.e., fully depleted). The pinned photodiode leads to the 4 transistor architecture (Figure 2.). Factorizing 3 transistors in each cluster of 4 pixels enables to have only 1.75 transistors/pixel.

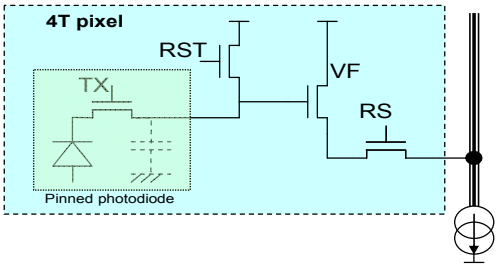

Figure 2. 4T pixel with process specific Pinned-Photodiode

In spite of many works proposing enhanced architecture, the simplest 3T, 4T and now 1.75T architectures, are now the most used in visible CMOS image sensors. Actually, the architecture and the layout of a pixel have a dramatic impact on its performances and yields. So, designers keep conservatively their pixels architecture and floorplan. In spite of these efforts, there is need for defect corrections that are handled in an algorithmic way in specific digital blocks of the image sensor.

B. *Image sensor as a SoC*

In the preceding sections, some of the most important features of photon transduction where presented. Yet, some post processing is required to ultimately get images and the operators must be embedded within the image sensor to further reduce their cost.

- The voltages of the pixels must be converted into digital. The resolution of the Analog to Digital (ADC) conversion is connected to image restitution. Indeed, the photodiode converts the energy of light in a quasi-linear way but the human vision system compresses high lights whereas lowlights are amplified. Hence, the standard image processing pipelines process raw pixel data with a power law called Gamma-correction that requires 10 bits Equivalent Number of Bits (ENOB). . Gamma corrected raw values are then down-quantified to their final 8 bits per color.
- Demoisaicing: Photodiodes can not discriminate wavelengths, their absorption range from near-infrared to blue. To acquire color images, one has to use a set of color filters. The most used mosaic of color filters is the Bayer matrix and consists of a 2×2 colors tile (one blue, one red and two diagonal green filters). In raw images, each pixel contains only one of the three primary colors; the two missing colors are computed from the neighboring pixel values. This step, referred as demosaicing, introduces a spatial low-pass filter and aliasing. Some alternatives have been explored at technological level, e.g. Foveon proposes a 3D pixel [15] that suppresses the need for demosaicing. Yet, this technology has a less accurate color rendering than the classical filters.
- White balancing: the illumination spectrum varies according to the light sources (sun, bulbs, neon lights…) and human visual system continuously adapts to perceive as white a wide palette of tints. On the opposite, photodiodes always produce a faithful image of the scene. By finding grey patches in the image, white balancing algorithms aim at analyzing the pixel raw values, determining the current scene conditions and computing a color correction matrix to translate color coordinates into the chosen white reference.

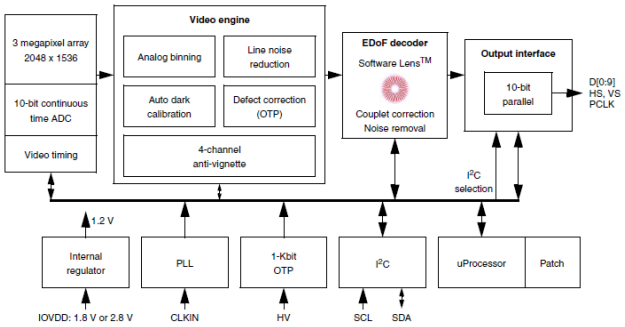

Figure 3. overview of a VD6803 imager (courtesy of STmicro)

In fact, as shown on Figure 3. image sensors encompass even more functions and CMOS Imagers are now real heterogeneous highly complex SoC.

IV. LIMITS AND HOW TO BREAK THEM

A. *Physical limits*

1) *Pixel size and dynamic*

Ultimately, the pixel size is limited by optical phenomena such as the Airy spot. The photo transduction by itself is a random process that follows a Poisson law. It constitutes the ultimate noise level. The amount of charges becomes dramatically low and even a pixels free of electronic noise would require the storage of a few thousands electrons to keep the 70dB dynamic range.

In order to keep the dynamic, "high" voltages (typically 1.8V) are required. Hence, deep submicron technology (65nm, 45nm… nodes) requires specific transistors with much larger minimum Gate Length (close to the ones in .25µm technologies). The size of those transistors might well be the limiting factor to further reduce the size of standard pixels.

2) *Frame rate and imager format consideration*

One of the drawbacks of the trend towards higher resolution is that imaging systems are encountering difficulty to accommodate the considerable amount of data of stemming from high resolution frames. For instance, considering a high end CMOS cameraphone image sensor, i.e. over 10Mpixel, achieving a 15 frame per second (fps) requires a sampling equivalent to 150Ms/s. Such image sensors can be limited either by the throughput of the digital shift register or by the conversion times of the standard ramp ADC (cf. Figure 4.).

TABLE II. HIGH ENDS ADCS CHARACTERISTICS AND FIGURE OF MERIT

Column based ADC Charateristics	ΔΣ [1] 14bits	SAR [2] 14bits	16 col. Multiplexed SAR 10bits	Single slope 10 bits
Technology	Samsung 130nm	Aptina 180nm	Leti 90nm	Leti 90nm
Pixel pitch	2.25µm	4.2µm	downto 1µm	1.4µm
Area (µm²)	4.5×850	8.4×1320	7920 16 columns	1.4×380
Conv. Time (µs)	2.3	1.5-1.7	0.325	17
FOM	0.71mJ/ Mpix	2.03mJ/ Mpix	16×17fJ/step @12bits	180fJ/step

3) ADC limitations considerations

The classical solution to get high throughput is to implement one ADC per column. Such architecture requires compact implementations, mainly based on single slope ADC (e.g. [16]). However, the exponential rate of convergence limits single slope ADC. 2nd order Delta Sigma [17] and SAR [18] based ADC are relevant candidates with aggressive figure of merit (FOM) for high frame rates and, large format (8.9Mpix@60fps for [18]). Yet, these implementations are limited by top-bottom column based implementations with large pixel pitch. A scalable architecture has thus been proposed with a SAR ADC shared by a group of columns. This implementation combines the pros of column based topology and a reduced area, being scalable down to 1µm pixel pitch even if its FOM is slightly increased (see TABLE II.).

B. A cleverer image acquisition?

Ten years ago, Abbas El Gamal has established a roadmap predicting the amount of transistors that could be integrated in a 5×5µm pixels with a 30% Fill-Factor as a function of the technology node [19]. Our approach is somewhat different: change the pixel architecture as little as possible but use the image properties and seek for new enabling technology to overcome the limitations of the standard approaches.

1) Processing in transposed space: from wavelet on the fly to compressive sensing

Image sensors now require several high speed 1Gbps output links to transmit high resolution images at video rate. Additionally, high-level image processing algorithms tend to require the storage of an increasing number of frames whereas storage ability is limited to keep system costs low in order to address the consumer market. Image sensors are therefore in need for an effective compression scheme that can accommodate imagers' severely complexity-constrained environment.

Several works have shown that the wavelet transforms can provide higher compression ratios than the Discrete Cosine Transform (DCT). Indeed, the Haar transform enables ultra-compact implementations: we have demonstrated an original wavelet decomposition that features a near lossless on the fly compression up to 5× at a hardware cost of a few kilogates (0.05mm² in 65nm technology) [20].

Once the image is in the Wavelet space, its components have a sparse representation, i.e. most of the useful information is dense. Pushing further the concept of using smart transposed spaces leads to the concept of compressive sensing. The idea is to apply a sampling function to transpose the image in a sparse space. This promising approach may significantly reduce power needs by compressing the image prior the ADC stage even if the preliminary works exhibit average compression ratio and specific pixels [21].

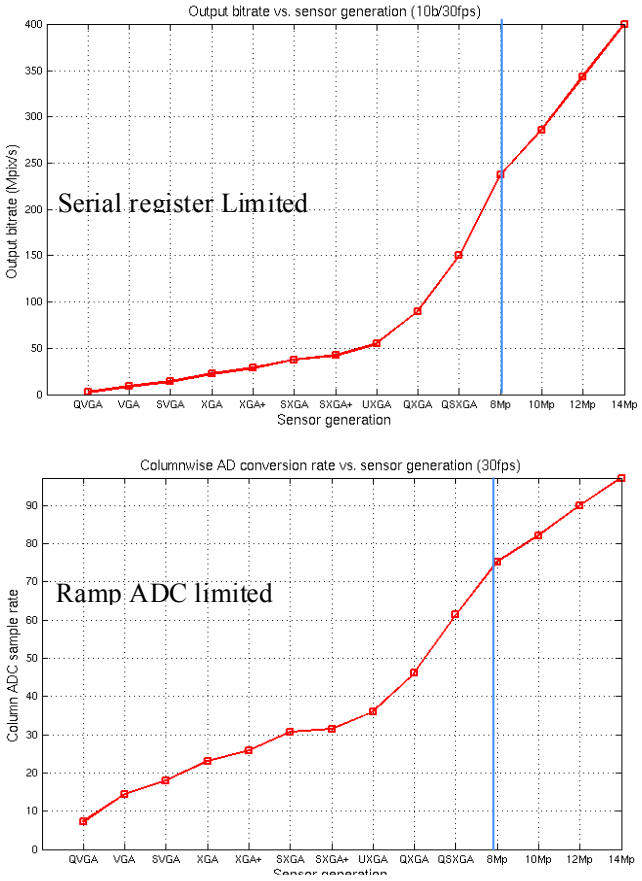

Figure 4. Throughput has 2 sources of limits: register transfert speed (a) and ramp ADC conversion time (b)

2) Smart image acquisition: working with ROIs

Since vision aims at retrieving information from a set of images, vision chips have slightly different constraints and issues than imagers. Yet the architectures for vision sensors must combine a good compliance with standard pixels along with specific operators.

In some applications, such as video surveillance, the background is unimportant and accelerating image processing can be obtained by focusing on the moving objects of the scene, i.e. determining Regions of Interest (ROI). Our concept is based on a vector of Analogue Programmable Processors whom architecture is very similar to the ADC ones. Such an approach enables to get rid of the ADC while enabling a set of arithmetic operations. These processors are optimized to compute estimators of the scene background, based on Sigma Delta or Recursive Average algorithms ([22], [23]). By

subtraction between the estimator and the current image, the ROIs where moving objects are located. Using a subsample view of the image and processing the image prior any ADC stage enable ultra-low power consumption (300µW for a 110×240 pixel array at 25fps) [24].

Pushing the concept further leads to retrieve the location of ROIs rather than reading the whole image. Hence, the concept of asynchronous scan has been developed. The idea is to asynchronously scan the processed pixel array. The scan is interrupted when a pixel containing relevant information is encountered. Its address is then sent to a supervisor. Once the address is read, the supervisor enables the scanning to proceed. On contours, reading can be accelerated by a factor of 100 [25]. A smaller Silicon footprint version has also been proposed to meet the low transistor per pixel count [26].

The smart reading of image is a very promising way to overcome the bottleneck of the throughput and to drastically reduce the power consumption in the image acquisition chain.

3) Technological trends: 3D integration

Three-dimensional integrated circuits (3D-ICs) have been explored since the mid 80s (e.g. [27]). 3D-IC should soon offer multiple advantages, namely lessening the communication bottleneck and enabling novel architectures. Most of the woks reported on 3D-ICs image sensors concentrate on achieving more computing capabilities (e;g. [28]). Instead, we consider that the important points in imager design are the image quality and the power consumption, tightly related to throughput.

One way to enhance the quality of image is to prevent pixels from saturating in bright area while keeping signal high enough in dark area. It implies to a High the Dynamic Range (HDR), typically up to 120dB, in order to cover most of the dynamic range of natural scenes illumination. HDR requires the equivalent of a 22 bits linear coding. Working towards a 3D-IC HDR image sensor, we have developed an architecture that combines HDR imaging and image compression. As shown on Figure 5. the pixel value is coded as a 10 bits mantissa and a 4 bits exponent. Considering that the illumination is homogeneous on a small area, after a voting process, a common exponent value is attributed to all the pixels within 32×32 pixels sub-blocks. The mantissa of the 32×32 block is then compressed using DCT. The overall compression ratio is greater than 10 with a PNSR above 30dB [29].

4) Expending the spectrum

Other parts of the spectrum can be detected like Infra-Red (IR) and X-Ray, and the problematic is slightly the same as for visible sensors once the quantum detection is done. For instance, the thermal effect due to photon absorption is exploited in uncooled microbolometers IR image sensors. The challenges in micro-bolometers are the removal of the FPN and its temporal variations. The FPN and its variations are usually compensated using a 2 temperatures reference map and require a mechanical shutter and thermo-electrical cooler (TEC) temperature regulation. Algorithmic solution can be used to get rid of the noise [30]. Alternatively, a compact analytical model, of the sensor allows for an accurate prediction of the variation of FPN. This enables to get rid of both shutter and TEC [31].

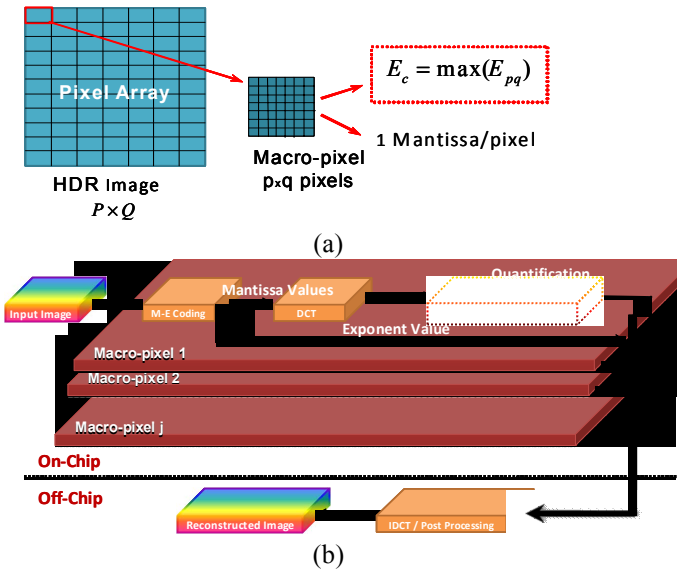

Figure 5. HDR image acquisition and compression principle (a) and architecture (b)

Since the IR and X-Ray pixel size can be large (25-150µm pixel pitch) and/or readout circuitry can occupy 100% of the pixel area, more complex readout pixel circuitry can be implemented. For instance, recent works have led to pixel-level ADC for HgCdTe IR sensors, which needs to be cooled down to 77°K to limit the photodiodes' dark current. It has enable to demonstrate 2mK discrimination over a dynamic range of 90dB, with ultra low power consumption ADC [32]. These specific works pave the way towards an all new set of applications, e.g; compact Positron emission tomography [33].

V. CONCLUSION

Although works on visions chips are still underway, we have identified several limitations that are critical even for "basic" imagers. Apart new technologies that are still to come, the development of specific image processing functions have demonstrated their growing importance to overcome the physical limitations of standard approaches. Yet, the architecture of those image processing functions must be compliant with a high image performances. Especially, the pixels must enable high yields and ever better image quality.

More important: the image sensors are now extremely complex SoC. The design of such heterogeneous systems implies design methodologies. As a first step, the virtual prototyping can be a nice way to explore a few architectural solutions. Such virtual prototype can be done using System-C since the system encompasses programs. Based on faithful models of the sensor, we have demonstrated the SystemC modeling of an entire vision chip ([34]), and the simulation of implemented algorithms on many images sequences. Yet, in order to ensure a consistency all through the design flow, a gap remains to be filled between those models and their physical description.

ACKNOWLEDGMENT

The authors would like to thanks B. Dupont, J.-P. Rostaing, J.-L. Martin, F. Guellec and J. Segura for their contributions.

REFERENCES

[1] Lyon R.F. , "The optical mouse, and an architectural methodology for smart digital sensors" VLSI-81-1, pp. 1-19, August 1981

[2] Mahowald M.A. , "Silicon retina with adaptive photodetectors", Proc. SPIE, Visual Information Processing : From Neurons to Chips, Vol. 1473, pp. 52-58, 1991

[3] Folowosele, F.; Vogelstein, R.J.; Etienne-Cummings, R. , "Real-time silicon implementation of V1 in hierarchical visual information processing," Biomedical Circuits and Systems Conference, 2008. BioCAS 2008. IEEE , pp.181-184, 20-22 Nov. 2008

[4] CulurcielloE. , Andreou, Andreas, "CMOS image sensors for sensor networks", Analog Integrated Circuits and Signal Processing, Springer, 2006, vol - 49, pp 49 51

[5] Carranza, L., Jimenez-Garrido, F., Linan-Cembrano, G., Elisenda M., Servando E., Rodriguez-Vazquez, A. "ACE16k based stand-alone system for real-time pre-processing tasks", Proc. SPIE, 2005 . Vol. SPIE-5837, pp. 872-879.

[6] Bernard, T.M.; Zavidovique, B.Y.; Devos, F.J.; "A programmable artificial retina," Solid-State Circuits, IEEE Journal of , vol.28, no.7, pp.789-798, Jul 1993

[7] Dupret, A.; Belhaire, E.; Rodier, J.-C.; Lalanne, P.; Prevost, D.; Garda, P.; Chavel, P.; , "An optoelectronic CMOS circuit implementing a simulated annealing algorithm," *Solid-State Circuits, IEEE Journal of* , vol.31, no.7, pp.1046-1050, Jul 1996

[8] "CALADIOM, l'œil intelligent qui veille pour vous", Vision DGA La revue de la Délégation générale pour l'armement, 2007, vol . 4, pp. 1, http://www.defense.gouv.fr/content/download/.../vision_dga_4_octobre_07.pdf

[9] Lalanne, P., Rodier, J.-C., Belhaire, E., Dupret, A., Garda, P., and Chavel, P., "Gaussian random number generation by differential detection of speckle", Optical Eng., vol. 34, no. 6, pp. 1835 - 1837, 1995.

[10] Prevost, D., Lalanne, Ph., Rodier, J.-C., Chavel, P., Dupret, A., Belhaire, E., Garda, P., "Video-rate simulated annealing for stochastic artificial retinas", Optics Communications, Volume 132, Issues 5-6, 15 December 1996, Pages 427-431, ISSN 0030-4018, DOI: 10.1016/0030-4018(96)00396-3.

[11] Elouardi, A., Bouaziz, S., Dupret, A. , Lacassagne, L., Klein, J.-O. and Reynaud, R., "Time comparison in image processing: APS sensors versus an artificial retina based vision system", Meas. Sci. Technol. 2007, Vol. 18, no.9

[12] Tian H. , Fowler B. , and El Gamal A. , "Analysis of Temporal Noise in CMOS APS," IEEE Journal of Solid State Circuits, Vol. 36, No.1, pp. 92-101, January 2001.

[13] El Gamal A. , "Trends in CMOS Image Sensor Technology and Design," International Electron Devices Meeting Digest of Technical Papers, pp. 805-808, December 2002.

[14] Cohen, M.; Roy, F.; Herault, D.; Cazaux, Y.; Gandolfi, A.; Reynard, J.P.; Cowache, C.; Bruno, E.; Girault, T.; Vaillant, J.; Barbier, F.; Sanchez, Y.; Hotellier, N.; LeBorgne, O.; Augier, C.; Inard, A.; Jagueneau, T.; Zinck, C.; Michailos, J.; Mazaleyrat, E.; , "Fully Optimized Cu based process with dedicated cavity etch for 1.75µm and 1.45µm pixel pitch CMOS Image Sensors," Electron Devices Meeting, 2006. IEDM '06. International , vol., no., pp.1-4, 11-13 Dec. 2006

[15] Hubel, P., and Bautsch, M., "Resolution for color photography", Digital Photography II, 2006, Proc. SPIE 6069, 60690M (2006), DOI:10.1117/12.654573

[16] Satoshi Yoshihara, "A 1/1.8-inch 6.4 MPixel 60 frames/s CMOS Image Sensor With Seamless Mode Change", IEEE Journal of Solid-State Circuits, Vol. 41, No. 12, December 2006

[17] Matsuo and al., "8.9-Megapixel Video Image Sensor With 14-b Column-Parallel SA-ADC", IEEE Transactions on Electron Devices, Vol. 56, No. 11, November 2009

[18] Youngcheol Chae and al., "A 2.1Mpixel 120frame/s CMOS Image Sensor with Column-Parallel ΔΣ ADC Architecture", ISSCC 2010

[19] El Gamal, A., Yang D., and Fowler B., "Pixel level Processing - Why?, What?, and How?," invited talk, Proceedings of the SPIE, Vol. 3650, pp. 2-13, San Jose, CA, January 27-28, 1999

[20] Alacoque, L., Chotard, L. et al., "A small footprint, streaming compliant, versatile wavelet compression scheme for cameraphone imagers", Proceedings of the 2009 International Image Sensor Workshop, IISW'09, June 2009, Bergen, Norway.

[21] Majidzadeh, V.; Jacques, L.; Schmid, A.; Vandergheynst, P.; Leblebici, Y.; , "A (256×256) pixel 76.7mW CMOS imager/ compressor based on real-time In-pixel compressive sensing," Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium on , vol., no., pp.2956-2959, May 30 2010-June 2 2010

[22] Verdant, A.; Dupret, A.; Mathias, H.; Villard, P.; , "Adaptive thresholding for motion detection in a CMOS image sensor," Signals, Systems and Computers, 2007. ACSSC 2007. Conference Record of the Forty-First Asilomar Conference on , vol., no., pp.495-499, 4-7 Nov. 2007

[23] Verdant, A.; Dupret, A.; Mathias, H.; Villard, P.; Lacassagne, L.; , "Low Power Motion Detection with Low Spatial and Temporal Resolution for CMOS Image Sensor," *Computer Architecture for Machine Perception and Sensing, 2006. CAMP 2006. International Workshop on* , vol., no., pp.12-17, 18-20 Aug. 2006

[24] Verdant, A.; Villard, P.; Dupret, A.; Mathias, H.; "Architecture for a low power image sensor with motion detection based ROI," Electronics, Circuits and Systems, 2007. ICECS 2007. 14th IEEE International Conference on , vol., no., pp.1023-1026, 11-14 Dec. 2007

[25] Dupret, A.; Vasiliu, M.; Devos, F.; , "Performance and power analysis on asynchronous reading of binary arrays," Circuits and Systems, 2006. ISCAS 2006. Proceedings. 2006 IEEE International Symposium on , vol., no., pp.4 pp.-5727, 0-0 0

[26] Dupret, A., Dupont, B., Vasiliu, M., Dierickx, B., Defernez, A., "CMOS image sensor architecture for high-speed sparse image content readout", IEEE International Image Sensor Workshop, 26-28 June 2009, Bergen, Norway

[27] Yasumoto, M., Hayama, H. and Enomoto, T. "Promising new fabrication process developed for stacked LSIs," IEEE Int. Electron Devices Meeting, pp. 816−819, Dec. 1984.

[28] Foldesy, P.; Carmona-Galan, R.; Zarandy, A.; Rekeczky, C.; Rodriguez-Vazquez, A.; Roska, T.; , "Digital processor array implementation aspects of a 3D multi-layer vision architecture," Cellular Nanoscale Networks and Their Applications (CNNA), 2010 12th International Workshop on , vol., no., pp.1-4, 3-5 Feb. 2010

[29] Guezzi-Messaoud F., Peizerat, A., Dupret, A., Blanchard, Y., "On-Chip Compression for HDR Image Sensors", DASIP 2010, to appear

[30] Dupont B. , Chammings, G., Rapellin, G., Mandier, C., Tchagaspanian, M., Dupont, B., Peizerat, A. ,and Yon, J. J. ,"New readout integrated circuit using continuous time fixed pattern noise correction", Proc. SPIE 6940, 69402W (2008), DOI:10.1117/12.779279

[31] Dupont, B.; Dupret, A.; Belhaire, E.; Villard, P.; , "FPN Sources in Bolometric Infrared Detectors," Sensors Journal, IEEE , vol.9, no.8, pp.944-952, Aug. 2009

[32] Guellec, F. , Peizerat, A., Tchagaspanian, M., De Borniol, E., Bisotto, S., Mollard, L., Castelein, P., Zanatta, J.-P., Maillart, P., Zecri, M. and Peyrard J.-C., "A 25 mu m pitch LWIR focal plane array with pixel-level 15-bit ADC providing high well capacity and targeting 2mK NETD", Proc. SPIE 7660, 76603T (2010), DOI:10.1117/12.849684

[33] Rossetto, O.; Rostaing, J.P.; Richer, J.P.; Billoint, O.; Bouvier, J.; Monnet, O.; Peizerat, A.; Montemont, G.; , "Integrated electronics for a CdTe based PET system," *Nuclear Science Symposium Conference Record (NSS/MIC), 2009 IEEE* , vol., no., pp.327-330, Oct. 24 2009-Nov. 1 2009

[34] Verdant, A.; Villard, P.; Dupret, A.; Mathias, H.; , "SystemC validation of a low power analog CMOS image sensor architecture," Circuits and Systems, 2007. NEWCAS 2007. IEEE Northeast Workshop on , vol., no., pp.903-906, 5-8 Aug. 2007