A New Architecture for Power Network in 3D IC

Hsien-Te Chen, Hong-Long Lin, Zi-Cheng Wang, TingTing Hwang
Department of Computer Science,
National Tsing Hua University, Hsinchu, Taiwan, 30013

Abstract— **Providing high vertical interconnection density between device tiers, through silicon via (TSV) offers a promising solution in 3D IC to reduce the length of global interconnection. However, some design issues hinder TSV from volumes of adoption, such as IR drop, thermal dissipation, current delivery per package pin and various voltage domains among tiers. To tackle these problems, the design of power network plays an important role in 3D IC. A new integrated architecture of stacked-TSV and power distributed network (STDN) is proposed in this paper. Our new STDN serves triple roles: power network to deliver larger current and reduce IR drop, thermal network to reduce temperature, and decoupling capacitor network to reduce power noise. As well, it helps to alleviate the limitation of the number of IO power pins. For both single and multiple power domains, the proposed STDN architecture demonstrates good performance in 3D floorplan, IR drop, power noise, temperature, area and even the total length of signal connections for selected MCNC benchmarks.**

1 Introduction

In contrast to device and local interconnection, global interconnection in two dimensional (2D) system-on-chip (SoC) designs is not scaled as feature size of process technology continues to shrink. Henceforth, global interconnection has become a major speed and power bottleneck in advanced technologies when more functionalities are accommodated in one single chip. Without further shrink of device sizes, three-dimensional (3D) integrated circuit (IC) chip has been identified as an effective way to achieve better performance in speed and power by scaled global interconnection [1]. Providing high vertical interconnection density between device tiers, through silicon via (TSV) offers a promising solution in 3D IC [2]. However, some design issues hinder TSV or even 3D IC from volumes of adoption, such as IR drop, thermal dissipation, current delivery per package pin and various voltage domains among tiers. To tackle these issues, the design of power network plays an important role in 3D IC.

While optimizing power network in 3D IC, traditional 2D design methodology is not applicable to 3D IC directly because new considerations come into play :

- **Limited number of power/ground IO pads:** One of major goals in 3D IC is to reduce die area. It results in less number of power/ground IO pads (PGIO, IO pads in redistributed layer (RDL) or in package under bottom-most tier connecting to power/groud voltage sources) available and more current delivery per PGIO. In other words, placement of PGIOs in 2D approach without considering activities among all tiers at the same time is not adequate.
- **Thermal dissipation:** Location with maximum vertical temperature gradient is different from the location with maximum temperature in 3D IC. Thermal TSV should be placed at location with maximum temperature gradient vertically among tiers (3D approach) other than location with maximum temperature on the tier (2D approach) [3]. Henceforth, we are not able to use 2D thermal approach (maximum temperature) to place thermal TSVs at hot spots directly. Power distributed network (PDN) solely is not an effective way to reduce temperature in 3D IC. The placement of PDN should take TSVs into account concurrently for thermal dissipation path. A 2D flow is not able to consider power dissipation path among TSVs vertically.
- **Power network partition:** In multiple power domain applications, 2D voltage island partition is not applicable to 3D tiers because power mesh partition and TSV placement have to consider all tiers at the same time in order to place level shifter.

Though the recent wave of 3D IC research is prosperous, research work pays not much attention to power delivery issues. Among a lot of research on 3D IC, only two papers have discussed the design of power network [4, 5]. One approach is to construct a regular power distributed network by top two layers of metal, the fixed number of TSVs and fixed-pitch power mesh [4]. The other approach is to co-synthesize PDN and floorplan, which develops PDN and floorplan concurrently, in 3D IC [5]. This work uses both uniform PDN and non-uniform PDN. In uniform PDN, there is only one PDN pitch for all tiers. In non-uniform PDN, each tier has its own optimal pitch without taking other tiers into account.

The disadvantage of regular power distributed network [4] and uniform power distributed network [5] is that it can not provide an optimal PDN pitch for a design which consists of active module with small area and inactive module with large area. For small and active module, a small PDN pitch is preferred; however, a large PDN pitch is preferred for large and inactive module. Non-uniform power distributed network [5] seems to be a better solution. Unfortunately, because pitch sizes among tiers are not considered, only limited number of TSVs can be aligned vertically to connect power networks in different tiers. For example, let the pitch of tier-1 be 157um and that of tier-2 be 117um. Because stacked-TSV has to be aligned at the common pitch location between tiers, the pitch for stacked-TSV between tier-1 and tier-2 will be 18369um, the Lowest Common Multiple (LCM) of the pitches of the two tiers. Inadequate interconnections (power TSVs) among power distributed network in different tiers will result in (1) more electronmigration issues, (2) more IR drop and (3) less efficiency in thermal dissipation.

It is essential to bear in mind that thermal, signal integrity and reliability of 3D IC configurations are equally important. Algorithms looking into these issues have to consider the simultaneous interplay of all stacked tiers. In addition, because of low resistance, large capacitance, high current delivery and good thermal conductivity in TSV, a well structure of PDN and power TSV is a good candidate to solve the above design issues in 3D IC. In this paper, a novel integrated architecture of stacked-TSV as power TSV and power distributed network, STDN (Stacked-TSV Distributed Network), is proposed to serve multiple roles to minimize IR drop, temperature and power noise. As well, it helps power delivery efficiency.

Our specific contributions in this paper are as follows.

- A novel integrated architecture of stacked-TSV and its corresponding power distributed network (STDN- Stacked TSV Distributed Network) is proposed. It is applied in 3D IC

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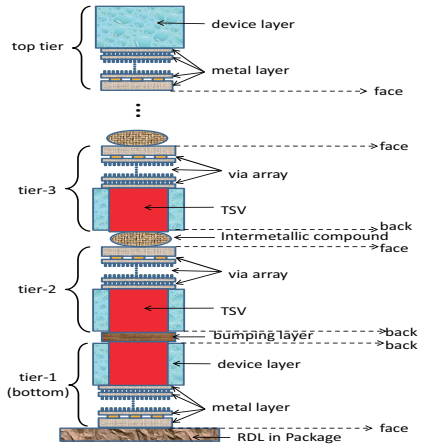

Fig. 1. Profile of Stacked TSV

designs not only with single power domain but also with multiple-power domain. It serves three objectives: (1) power distributed network for IR-drop minimization; (2) thermal distributed network for thermal dissipation; (3) decoupling capacitance distributed network for power noise reduction.

- A *voltage volume* in 3D IC extended from 2D voltage island for multiple power domain is proposed.
- Based on the new proposed STDN architecture, an algorithm to demonstrate the effectiveness of STDN for signal integrity and thermal dissipation in both single power domain (SPD) and multiple-power domain (MPD) is put forth.

The rest of the paper is organized as follows. Section 2 proposes an integrated architecture of stacked-TSV and thermal and power distributed network (STDN). Section 3 formulates the minimization problem for voltage drop, temperature and other factors in the new proposed architecture and proposes an algorithm to solve them during floorplanning. Section 4 shows experimental results. Conclusions are put forth in Section 5.

2 New Architecture of Stacked-TSV and Distributed Network

In this section, we will discuss basic characteristics of STDN and compare it with other work.

Fig. 1 illustrates the profile of stacked-TSV. The basic characteristics of the stacked-TSV are described as follows.

- TSV goes through silicon and stops on metal-1 (M1). M1 uses stacked via-array to connect top metal.
- Connection of tier-1 to package by RDL directly uses flip-chip method. Tier-1 to tier-2 are connected back-to-back by bumping layer which also links TSV of tier-1 to TSV of tier-2.
- Tier-2 to tier-3 are connected face-to-back by intermetallic compound which links top metal of tier-2 to TSV of tier-3. The same interconnection is constructed between tier-3 to tier-4, tier-4 to tier-5, and so on except tier-(n-1) to top tier.
- Tier-*(n-1)* to top tier is connected face-to-face by intermetallic compound which links top metal of tier-*(n-1)* to top metal of top tier. This structure allows that the top tier does not need TSV process.
- All of power/ground (PG) sources are connected through RDL to PG nodes of tier-1, while the PG nodes in upper tiers are connected to PG sources by TSVs of tier-1.

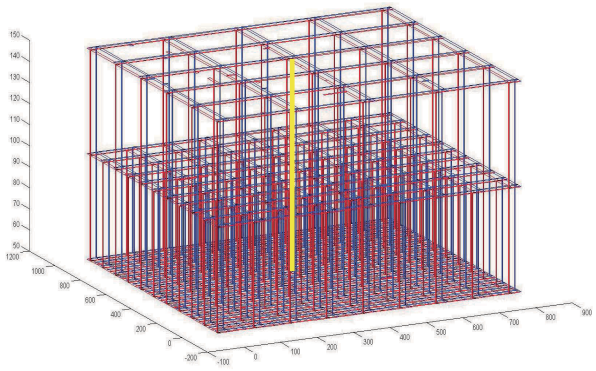

Fig. 2. Architecture of STDN in 3 Tiers

- Taking 3 tiers as an example. To serve as power TSVs and thermal TSVs, stacked-TSVs could be connected in two ways: (1) tier-1 $\rightarrow$ tier-2; (2) tier-1 $\rightarrow$ tier-2 $\rightarrow$ tier-3. To serve as DECAP (decoupling capacitor) TSVs, stacked-TSVs could be connected in three ways: (1) tier-1 $\rightarrow$ tier-2; (2) tier-1 $\rightarrow$ tier-2 $\rightarrow$ tier-3; (3) tier-2 $\rightarrow$ tier-3;

Next, the basic characteristics of the STDN are described as follows.

- **The pitch ratios among all tiers are integers.** For example, in the experiments conducted in this paper, pitch ratio of tier-1:tier-2:tier-3:tier-4 is 1:2:4:4. This is a key property of our power network. With this property, stacked-TSVs connecting power networks in different tiers can be inserted easily. The actual pitch size is determined by module activities, IR drop, thermal dissipation and floorplan during floorplanning.
- Stacked-TSVs are placed on cross section optionally.
- For multiple power domain applications, *voltage volume* is designed. The concept of *voltage volume* in 3D is similar to voltage island in 2D. As is implied by its name, the modules using the same voltage are placed at the same planar (2D) location among all tiers such that STDN are partitioned to cut power mesh and the corresponding stacked-TSVs are able to connect to the same voltage.

An example of STDN in 3 tiers is illustrated in Fig. 2. The pitch ratio of tier-1:tier-2:tier-3 is 1:2:4. The planar lines in red are power mesh and the planar lines in blue are ground mesh. The vertical bars in red are TSVs connected to power mesh while the vertical bars in blue are TSVs connected to ground mesh. The thick solid bar in yellow shows a stacked TSV connects power networks in tier 1, 2 and 3.

Fig. 3 demonstrates an example of 3D floorplan with *voltage volume* in multiple power domain of STDN. The modules in the same color are assigned to the same voltage. The lines of the same color are PDN in the same voltage. In this example, two voltages are assigned for tiers and two *voltage volumes* are constructed. In order to avoid large leakage in standard cell, a level shifter is required when signal propagates from low voltage to high voltage. One advantage of *voltage volume* is that level shifters are easily placed at any tier. Because each tier are partitioned into *voltage volume* according to the number of voltages used, each tier has all its required voltage levels. The two power supply voltages of level shifter are able to be connected at the same tier wherever level shifter is placed. Without the concept of voltage volume, it is very difficult to place level shifter. For example, suppose a level shifter

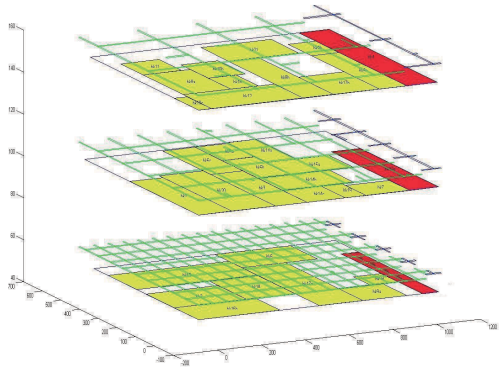

Fig. 3. Example of 3D Floorplan in MPD

converts 0.8V to 1.2V, 0.8V PDN is constructed in tier-3 and 1.2V PDN is constructed in tier-1. It is difficult to connect two power supply voltages whichever tier the level shifter is located.

The major advantages of the proposed architecture are

- Based on regular PDN mesh and the ratios of pitches which are given constants among tiers, the number of TSVs in stacked-TSV architecture and the length of PDN are well controlled by PG mesh pitch. Moreover, all of stacked-TSVs are the same size and aligned. It is friendly to process manufacturing for variation control.
- All of current delivery are uniformly shared by STDN. It helps alleviating the limitation of the number of PGIOs and reducing electron migration impact.
- A key observation in [6] shows both the number of PGIOs and the number of TSVs in each layer being increased (decreased) at the same time according to PDN mesh pitch maximizes the performance in power noise reduction. Our STDN architecture meets this requirement.
- Because of well controlled pitch in STDN, thermal wire is able to conduct thermal lateral to the nearest stacked-TSVs. More importantly, stacked-TSVs provide a **direct path** from top tier to bottom tier for thermal dissipation effectively.
- *Voltage volume* partition approach make it easier to place level shifters.
- Because STDN plays dual roles in power network and thermal network, refinement of STDN reduces IR drop and temperature at the same time.

3 3D Floorplan with New Proposed Architecture

To demonstrate the effectiveness of our integrated architecture, STDN, we will develop a floorplan algorithm to minimize IR drop and temperature. The output includes floorplanning result and the actual size of PDN pitch under given pitch ratios among tiers.

3.1 Problem Formulation

In order to describe problem formulation clearly, multiple power domain (MPD) problem is separated from single power domain (SPD) problem even though those two problems are solved by the same algorithm in a fusion way.

- Problem of single power domain is defined as follows:
  Given a set of current consumption for each module, a net-list of module connectivity in block-level, geometry information of each module (length, width of module, locations of pins, etc.) and the number of tiers for 3D floorplan. Our objective is to floorplan those modules and construct power distributed network by STDN so that IR drop, temperature, area, wire length and the number of signal TSVs are minimized.

- Problem of multiple power domain is defined as follows:
  Given a set of current consumption for each module, a net-list of module connectivity in block-level, geometry information of each module, the number of tiers for 3D floorplan, timing constraints and the number of voltages used. Our objective is to floorplan those modules, construct power distributed network by STDN and assign voltages to modules so that IR drop, temperature, area, wire length, the number of signal TSVs, the number of level shifters, total power consumption are minimized and timing constraints are met.

3.2 IR Drop Modeling

STDN builds electrical resistors and capacitors based on distributed network geometry while treating power pins of each module as current sources. For DC IR drop analysis, resistance of stacked-TSV, resistance of PDN in STDN and *constant* currents are applied. For power noise analysis (transient IR drop), STDN takes resistance, capacitance and *transient* current stimuli into consideration. In addition to resistors, capacitors and current sources, ideal voltage sources are applied from IO pads through bottom-most tier as power sources. In IR drop modeling, both RDL and package are not taken into account for all simulations (including ours and [5] emulations). In other words, ideal voltage sources are directly connected to passivation opening in flip-chip of bottom-most tier.

As to power noise analysis (transient IR drop), the waveform of transient current stimulus is approximated by a triangular waveform to emulate current transitions during voltage transitions of signals. The total charge of transient current waveform is equal to total charge of DC (constant) current waveform. This relationship is formulated as Equ. (1).

$$\int_0^T I(t) \cdot dt = I_{constant} \cdot T \tag{1}$$

where I(t) is transient current stimuli, $I_{constant}$ is constant current and T is simulation time. After 3D floorplan and STDN construction is done, a SPICE simulation run deck and SPICE net-list are generated. Then HSPICE simulator [7] is invoked to simulate run deck and to output IR drop measurement data.

3.3 Thermal Modeling

STDN builds an equivalent thermal circuit through thermal-electrical analogy. By steady-state equation of thermal network, thermal resistors are connected between nodes which are spatially adjacent regions. Moreover, thermal current sources are mapped to power sources. The voltages at the nodes in this equivalent thermal circuit are computed by solving equations of equivalent thermal network. These voltages yield the temperatures at those nodes. The ground node of the circuit corresponds to a constant temperature node which is typically the ambient temperature.

In our thermal modeling of STDN, grid-based method is applied for thermal simulations and analysis. 20×20 grids are used in thermal network laterally.

Based on the above approach, all thermal resistors, voltage sources for ambient temperature, current sources for power consumptions are generated into SPICE run deck and net-list. As does

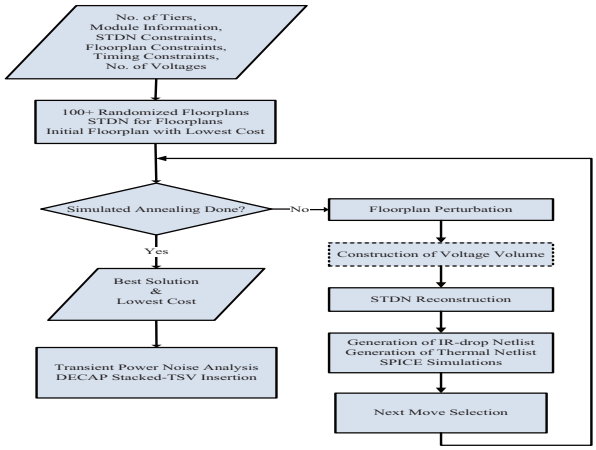

Fig. 4. Proposed Algorithm in 3D Floorplan

IR drop simulation, HSPICE simulator is applied to simulate and to output temperature measurement data.

3.4 Proposed Algorithm

In order to trade off many design factors in 3D floorplan at the same time, nondeterministic algorithm, simulated annealing (SA), is used in our algorithm as shown in Fig. 4. In addition, 3D B*-tree structure is applied in our algorithm as a floorplan representation [5].

First, the number of tiers in 3D floorplan, module information (power consumption, netlist, width, length, pins, etc.), the size of stacked-TSV, the width of PDN in STDN, range of PDN pitch, IR drop and EM limitations are fed into flow. Furthermore, if 3D floorplan is constructed in multiple power domain (MPD) the timing constraints and the number of voltages applied in MPD are also fed into flow. Second, hundreds of 3D floorplan of the selected benchmark are randomly generated and the corresponding STDN structures are constructed accordingly. Based on our cost function, the best floorplan with the corresponding lowest cost is found among those hundreds of random floorplans as an initial solution. In single power domain (SPD), the cost factors in cost function include maximum IR drop, maximum temperature, maximum temperature gradient, maximum area variation, footprint area, the number of stacked-TSVS in STDN, the number of TSVs for signals, total wire length of signals, total wire length of STDN and white space. White space is defined as area not used by module in core area (it might be used by power strips in STDN and stacked-TSVs outside of modules). In multiple power domain (MPD), besides the cost factors defined in single power domain, the cost factors in cost function include the number of level shifters, area of level shifters and product of power and delay.

Third, simulated annealing (SA), a non-deterministic algorithm, is applied as a main body of our algorithm to find lowest cost solution. Fourth, the perturbation of the current floorplan and STDN is created. The perturbation consists of inter-tier movement, inter-tier swapping, intra-tier movement, intra-tier swapping, intra-tier rotation and pitch refinement. Fifth, if 3D floorplan is MPD, *voltage volume* (i.e., voltage domain partition) is constructed. Then Integer Linear Programming (ILP) is applied for voltage assignment [8]. Sixth, the SPICE run decks and net-lists (both DC and transient) are constructed according to 3D floorplan and STDN structure for IR-drop and thermal simulations. Seventh, SA selection method is used with HSPICE simulation results.

TABLE I
Key Parameters Used in Experiments

Parameter	Value
Max. number of tiers	4
Thickness of wafer	50um
Metal width for signals	1um, 10um
Max. Metal Width	10um
Diameter of TSV	6um, 8um
Metal width for STDN	8um, 10um
Min. pitch of STDN	50um
ρ_R of TSV ($\Omega \cdot um$)	0.0198
ρ_C of TSV (fF/um^2)	4.316
ambient temperature	$25°C$

Finally, when the simulated annealing process terminates, transient power noise (transient IR drop analysis taking both resistance and capacitance into account) is analyzed for the generated floorplan and STDN. If transient power noise of node is larger than a predefined threshold (10% VDD in our algorithm), the stacked-TSVs, serving as decoupling capacitors, are added in STDN around nodes which violates power noise threshold.

4 Experiments

4.1 Experiment Setup

Four benchmark examples (AMI33, XEROX, APTE and AMI49) selected from MCNC benchmarks are used in our new architecture for 3D floorplan experiments. The number of tiers varies from 1 to 4 for each benchmark. The CMOS BULK process with copper TSV and metal layers in $90nm$ technology is applied in experiments. As to 3D floorplan in single power domain, 1V typical voltage is applied. As regards 3D floorplan in multiple power domain, three voltages (0.8V, 1.0V, 1.2V) are applied. When the number of tier is one, the flip chip with 2 times STDN pitch is applied to connect power pads. In other words, flip chip pitch is 100um while STDN pitch is 50um. If maximum IR drop and ground bouncing is larger than 15% of VDD, then the metal width of power pin of the module to STDN is redefined to $10um$ (the width is $1um$ by default for power pins of the modules). The key parameters used in experiments are summarized in Table I, where ρ_R is resistivity and ρ_C is capacitance per unit area.

Furthermore, we take effect of TSV area into consideration in Table II and comparison of single and multiple power domains in subsection 4.2.2 where module area is expanded to accommodate the area of TSVs. The amount of expansion is determined by the number of stacked-TSV, size of TSV used and structure of STDN. However, the comparison in Tables III and IV assumes zero size TSV because our data is compared to that presented in [5] where zero size TSV (i.e., a module is not expanded to accommodate TSVs) is assumed.

4.2 Experimental Results

4.2.1 3D Floorplan in Single Power Domain

The first experiment is to understand the effectiveness of STDN in single power domain. The experiment results are shown in Table II. All data are the average of four selected MCNC benchmarks. In this table, the module area is scaled up according to the number of stacked-TSVs and structure of STDN. "Size" in the first column is the size of stacked-TSV, where 6 (8) is a 6 (8)um TSV. "Ratio" in the first column means data in "Ratio" rows are performance ratio of 6um data (numerator) to 8um data (denominator) "#Tiers" is

TABLE II
PERFORMANCE SUMMARY IN SINGLE POWER DOMAIN

Size	# Tiers	Max IR(mv)	Max T($^\circ C$)	Γ ($v \cdot ps$)	TN (mv)	A_{fp} (um^2)	# TSV_S	# TSV_I	WL_S (um)	WL_I (um)	WS (um^2)
6	1	100.6	36.7	406.1	279.1	36847118	0	0	893224	765103	9737985
	2	117.5	31.9	414.5	318.8	18751505	164	96	437387	513562	7745135
	3	131.4	42.3	476.0	345.1	11683205	159	187	357320	467268	8324945
	4	91.5	39.6	496.7	350.4	9715247	1095	196	777953	410769	10530138
8	1	72.4	40.4	478.8	248.7	33996095	0	0	689893	770237	6219809
	2	69.8	31.5	437.8	293.8	18493460	1017	83	1000146	542058	7489598
	3	119.5	34.5	441.5	321.3	12952760	439	163	618380	457895	10722073
	4	91.6	38.5	478.2	346.8	9103561	1121	239	815428	398520	6887283
Ratio	1	1.39	0.91	0.85	1.12	1.08	-	-	1.29	0.99	1.57
	2	1.68	1.01	0.95	1.08	1.01	0.16	1.16	0.44	0.95	1.03
	3	1.10	1.22	1.08	1.07	0.90	0.36	1.15	0.58	1.02	0.78
	4	1.00	1.03	1.04	1.01	1.07	0.98	0.82	0.95	1.03	1.53
Average		1.29	1.04	0.98	1.07	1.02	0.50	1.04	0.82	1.00	1.23

the number of tiers. "Max IR" is maximum IR drop from all nodes when power consumption is DC. "Max T" is maximum temperature from all grids. "Γ is the total sum of power noise which is defined as total sum of the integral of the voltage drop below 10% VDD for power-grid-induced noise at all nodes [9]. "TN" is the maximum transient noise. "A_{fp}" is the area of footprint. "#TSV_S" is the number of TSVs in stacked-TSV structure in STDN for thermal and power delivery. "#TSV_I" is the number of TSVs for signal connections. "WL_S" is total wire length of power mesh in STDN. "WL_I" is total wire length of signal interconnections. "WS" is white space which is core area not used by module (it might be used by power strips in STDN and stacked-TSVs outside of modules). "Average" is the average performance ratio of all 4 tier conditions for all performance metrics.

From power TSV point of view, compared with 6um TSV, 8um TSV reduces IR drop by 29% and white space by 23%. The resistance of TSV is critical to IR drop. From thermal TSV point of view, performance is similar between two sizes. Moreover, a design with more number of TSVs uniformly distributed is more effective than a design with large size of TSVs.

From 3D floorplan quality point of view, 6um TSV outperforms 8um TSV in the number of stacked-TSVs by 50%, in total wire length of STDN by 18%. The area expansion of module due to stacked-TSV area does have impact on 3D floorplan quality. The performance of 6um TSV is similar to 8um TSV in total sum of power noise, in transient noise, in footprint size, in the number of signal TSVs and in the total wire length of signal interconnection. The TSV size does not have impact on signal interconnections.

Moreover, the temperature in 1-tier is higher than that in 2-tier because there is no TSV for thermal dissipation. As to the number of tiers, it does not have consistent relationship to (1) IR drop; (2) temperature; (3) power noise; (4) the number of stacked-TSVs; (5) the total wire length of STDN and (6) white space. However, the more number of tiers results in (1) smaller footprint (but not proportional reciprocally to the number of tiers); (2) more TSVs for signal interconnections; (3) less total wire length of signal interconnections; and (4) more transient noise.

The second experiment is to compare architecture performance of STDN with that of [5]. Before we present the simulation data of [5] and ours, the following experiment setup is described:

- Our tool is integrated in the tool developed by [5]. Hence, the software platform used by two methods including floorplan representation in B*-tree and simulated annealing engine are the same.
- TSV size, maximum metal width and other process-dependent parameters are the same.
- IR drop and thermal generation are conducted by models as described in Section 3 for both methods.
- The simulation data of MCNC benchmarks are identical.
- Regardless of the number of TSVs and the structure of power network, module area is not expanded for both sides.
- Power pins (e.g., VDD, GND pins) of module connects to the nearest PDN mesh in our approach while power pins of module in [5] connects to TSV (cross point of power mesh) .

TABLE III
PERFORMANCE COMPARISON WITH NON-UNIFORM FLOORPLAN [5]

Size	# Tiers	Max ΔV	Max T	Max ∇T	FP Area	# TSV	Wire Length	White Space
6	1	0.15	1.11	1.88	0.73	-	0.64	0.33
6	2	0.47	0.87	0.74	0.76	6.72	0.50	0.54
6	3	0.31	0.87	0.61	0.63	4.68	0.56	0.39
6	4	0.38	0.74	0.37	0.72	4.17	0.56	0.55
8	1	0.24	1.08	1.62	0.68	-	0.60	0.32
8	2	0.58	0.97	1.10	0.86	8.31	0.66	0.87
8	3	0.43	0.77	0.39	0.71	6.82	0.59	0.48
8	4	0.35	0.81	0.68	0.72	3.44	0.58	0.48
Average		0.36	0.90	0.92	0.73	5.69	0.59	0.50

According to experimental results in [5], performance of uniform and non-uniform mesh is similar. Henceforth, we choose only non-uniform approach for comparison.

Performance comparison with non-uniform 3D floorplan in [5] is summarized in Table III. All data are the average of four selected MCNC benchmarks.

"Max. ΔV" is ratio of maximum IR drop by our approach (numerator) to the maximum IR drop by [5] (denominator). "Max. T" is ratio of maximum temperature and "Max ∇T" is ratio of maximum temperature gradient. "FP Area" is ratio of foot print area. "#TSV" is total number of TSVs used in power network. "Wire Length" is total length of signal wires. "White Space" is area not used by module in core area. "Average" shows the average performance ratio of all 8 test conditions (6um with tier from 1 to 4, 8um with tier from 1 to 4) in all performance metrics.

TABLE IV
COMPARISON OF NETWORK STRUCTURE [5]

Size	#Tier	AMI33				XEROX				APTE				AMI49			
		Max IR		#TSV		Max IR		#TSV		Max IR		#TSV		Max IR		#TSV	
		Ours	[5]	Ours	[5]	Ours	[5]	Ours	[5]	Ours	[5]	Ours	[5]	Ours	[5]	Ours	[5]
6	1	0.012	0.140	0	0	0.018	0.148	0	0	0.068	0.597	0	0	0.139	0.479	0	0
6	2	0.143	0.145	8	12	0.070	0.143	36	72	0.211	0.326	96	168	0.153	0.153	72	256
6	3	0.130	0.139	10	16	0.067	0.135	32	168	0.288	0.366	94	196	0.180	0.282	94	168
6	4	0.131	0.127	12	28	0.053	0.131	34	252	0.334	0.577	72	264	0.154	0.161	246	450
8	1	0.013	0.144	0	0	0.018	0.110	0	0	0.080	0.201	0	0	0.144	0.469	0	0
8	2	0.071	0.137	8	8	0.091	0.138	40	72	0.263	0.341	70	8	0.183	0.221	40	70
8	3	0.086	0.145	10	16	0.090	0.132	40	24	0.258	0.404	72	160	0.163	0.185	120	216
8	4	0.081	0.104	20	24	0.089	0.123	40	252	0.234	1.185	86	324	0.158	0.198	162	216

As to the maximum temperature and the maximum temperature gradient, both structures show similar performance. As to footprint area, total wire length and white space, our approach shows better results. As to the maximum IR drop, out approach reduces 64% more voltage drop than that in [5].

As to the number of TSVs, our approach shows flexibility to provide 5 times more number of TSVs than [5]. Even though 5 times more number of TSVs are used, the total area of TSVs occupies less than 2% (0.51%, 0.51%, 0.23%) of footprint area in AMI33 (XEROR, APTE, AMI49).

Next, we want to understand if our power network is a better structure even without large number of TSVs, we conduct an experiment to remove the requirement of IR drop reduction in our approach. Table IV is the comparison of [5] and ours. It shows that we use less or equal number of TSVs for 31 cases out of 32 and achieve smaller maximum IR drop for all cases.

4.2.2 3D FLOORPLAN IN MULTIPLE POWER DOMAIN

The third experiment is to understand the effectiveness of STDN in multiple power domain. In multiple power domain, two kind of application domains are experimented- high performance (HP) and low power (LP). Three voltages (0.8V, 1.0V, 1.2V) are available in experiment of multiple power domain. Because of no timing information provided in MCNC benchmarks, we create delay information of module based on module area. The larger module area results in larger delay. As to HP experiments, the timing constraint of MPD is set to 0.9X of SPD delay in 1.0V (i.e., speed of MPD is 10% faster than that of SPD in 1.0V). As regards LP experiments, the timing constraint of MPD is set to 1.3X of SPD delay in 1.0V (i.e., speed of MPD is 30% slower than that of SPD in 1.0V). All data are the average of four selected MCNC benchmarks.

In summary, both in high performance (HP) and low power (LP) experiments, MPD shows similar performance as compared with SPD in footprint area, the number of TSVs for signal interconnections, and the total wire length of signal interconnections.

As to speed in HP experiments, compared with SPD, MPD achieves 14% faster with overhead of 2.0X more maximum IR drop, 8% higher maximum temperature, 1.4X more number of stacked-TSVs, 41% longer total wire length of STDN, 10% more white space, 26 level shifters added and 29% more power .

As regards power-related performance in LP experiments, compared with SPD, MPD achieves 42% less power, 31% less maximum IR drop, 11% lower maximum temperature with overhead of 24% more number of stacked-TSVs, 18% longer total wire length of STDN, 28% more white space, 21 level shifters added and 29% slower.

From *voltage volume* point of view, the total wire length of signal interconnections and footprint area are not much affected. Moreover, the number of level shifters is very limited. However, multiple power domain partition (cut) does have impact on STDN architecture (the number of stacked-TSV and total wire length of STDN) and white space.

5 CONCLUSION

A new integrated architecture, STDN (Stacked TSV Distributed Network), is developed to create 3D floorplan and its distributed network for power delivery and thermal dissipation at the same time. It presents its effectiveness in solving IR drop, temperature, power noise and floorplan quality. Furthermore, *voltage volume* is proved as an effective approach in multiple power domain partitioning for 3D floorplan.

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