Analytical Heat Transfer Model for Thermal Through-Silicon Vias

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***Abstract*—Thermal issues are one of the primary challenges in 3-D integrated circuits. Thermal through-silicon vias (TTSVs) are considered an effective means to reduce the temperature of 3-D ICs. The effect of the physical and technological parameters of TTSVs on the heat transfer process within 3-D ICs is investigated. Two resistive networks are utilized to model the physical behavior of TTSVs. Based on these models, closed-form expressions are provided describing the flow of heat through TTSVs within a 3-D IC. The accuracy of these models is compared with results from a commercial FEM tool. For an investigated three-plane circuit, the average error of the first and second models is 2% and 4%, respectively. The effect of the physical parameters of TTSVs on the resulting temperature is described through the proposed models. For example, the temperature changes non-monotonically with the thickness of the silicon substrate. This behavior is not described by the traditional single thermal resistance model. The proposed models are used for the thermal analysis of a 3-D DRAM-μP system where the conventional model is shown to considerably overestimate the temperature of the system.**

***Index Terms*—3-D ICs, Thermal through-silicon via (TTSV), thermal resistance, heat conductivity.**

I. Introduction

In 3-D integrated circuits, thermal issues are forecast to be a major challenge. This situation is due to the high power density, the low thermal conductivity along the primary heat transfer path, and the smaller footprint area of the circuit attached to the heat sink [1]–[3].

Several techniques have been developed to facilitate the heat transfer within 3-D circuits to reduce the temperature, such as *thermal through-silicon via* (TTSV) planning [4], [5], thermal wire insertion, liquid cooling, and thermal-driven floorplanning [3], [6]. TTSVs are vertical vias used only to convey heat. Using thermal vias to facilitate the transfer of heat has been traditionally utilized in the design of packages and printed circuit boards [7]. Several papers have demonstrated that TTSVs can alleviate the thermal problem in 3-D IC designs [4], [5]. Analyzing how the TTSVs affect the developed temperature in 3-D ICs is important for efficient TTSVs insertion. The thermal properties of TTSVs, in turn, are determined by several physical and technological parameters.

The traditional approach is to thermally model a TTSV as a vertical lumped thermal resistor in each physical plane, which is proportional to the length and inversely proportional to the diameter of the TTSV [1], [7]–[9]. The TTSV is considered as a one-dimensional (1-D) network implying a flow of heat only in the vertical direction towards the heat sink of the system. This method is shown to be insufficient in capturing the thermal behavior of the TTSVs since the lateral heat transfer through these structures is neglected. Compact thermal models can capture the heat transfer in all directions by representing a circuit with a set of nodes connected with thermal resistors [10], [11]. Alternatively, a highly accurate and common mesh-based method to analyze the thermal behavior of a system including TTSVs is the *finite element method* (FEM). Nevertheless, neither the compact models nor the FEM approaches offer a link between the heat transfer process and the physical parameters of the TTSVs.

To accurately describe and offer insight about the thermal properties of these structures, novel analytical thermal models for the TTSVs are presented in this paper. These models include the most important physical and technological parameters related to TTSVs, such as the thickness of the insulator liner and the thickness of silicon layers.

A thermal TSV is modeled as a compact resistive network rather than a single resistor. The accuracy of the resulting models is verified by the COMSOL Multiphysics tool [12]. The effect of the parameters related to TTSVs on temperature reduction is discussed through simulations in [13], [14]. There is, however, no analytical method to describe and quantify these effects.

The remainder of the paper is organized as follows. The proposed analytical thermal model of TTSVs is introduced in Section II. A distributed model without fitting coefficients is presented in Section III. The effect of the TTSV parameters on the temperature of 3-D circuits is presented in Section IV along with a case study of a 3-D DRAM-μP system. The conclusions are drawn in Section V.

II. Thermal Analysis of TTSVs

The traditional thermal model of a TTSV only considers the vertical transfer of heat through TTSVs. Consequently, a single thermal resistance is assumed to suffice. Alternatively, the

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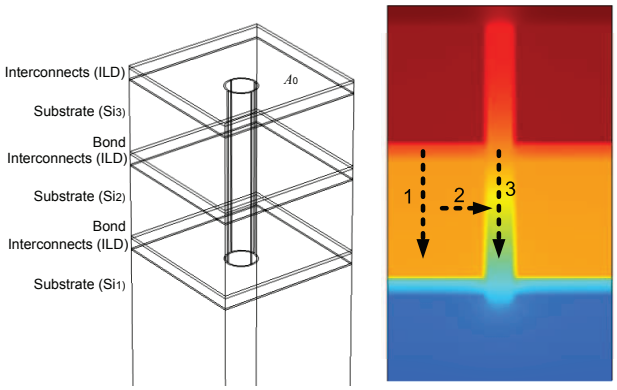

(a) (b)

Fig. 1. A segment of a three-plane 3-D IC with a TTSV, where (a) is the geometric structure and (b) is the cross section. The footprint area of the circuit is denoted by A_0. Three paths of heat transfer are depicted with the dashed lines.

compact models consider heat conveyed in all directions for full-circuit analysis [10]. An improved steady-state analytical model integrating the advantages of these two approaches is presented in this section.

3-D ICs utilizing wafer bonding technology are considered [6]. A segment of a typical three-plane 3-D circuit with a single TTSV is illustrated in Fig. 1. The physical structure is illustrated in Fig. 1(a). The cross section of the circuit and the temperature distribution from COMSOL Multiphysics is illustrated in Fig. 1(b). Although for different fabrication technologies the materials and geometries of the circuit can vary, the underlying structure remains the same.

As labeled in Fig. 1(a), each plane of the circuit consists of three layers describing the silicon substrate (Si), the *inter layer dielectric* (ILD) and metal interconnects ($i.e.$, BEOL), and the bonding layer, respectively. The heat sources include the power generated by the active devices on the top surface of the Si substrates and the Joule heat generated by the interconnects surrounded by the ILD. The cross section of Fig. 1(a) and the temperature distribution is illustrated in Fig. 1(b). Different paths of the flow of heat are depicted with the dashed lines in Fig. 1(b).

The proposed thermal resistance network (Model A) describing the thermal conductance of TTSVs is illustrated in Fig. 2. Due to the similarity between heat transfer and electrical current flow [10], the heat sources are modeled as current sources (q_1 - q_3 in Fig. 2) and the temperature is analogous to the voltage at a node. In Fig. 2, T_0 - T_5 are used to denote the difference between the temperature in different planes and the temperature at the bottom of the first plane, which is adjacent to the heat sink and is considered as a reference temperature. A voltage source and/or another resistor can be included to describe the ambient temperature and/or the thermal resistance of the package. These elements, however, are not required for modeling the thermal behavior of the TTSVs (but rather for the temperature rise within a 3-D IC). In the proposed model, a TTSV is considered as a stack of TSVs through all the planes, as depicted in Fig. 2. Based

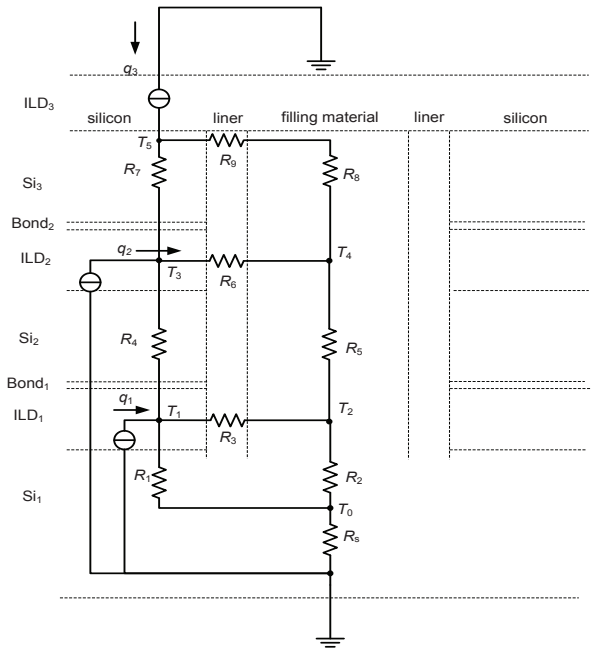

Fig. 2. Thermal model of a TTSV in a three-plane circuit (Model A).

on Kirchhoff's Current Law (KCL),

$$q_3 = \frac{T_5 - T_3}{R_7} + \frac{T_5 - T_4}{R_8 + R_9}, \tag{1}$$

$$q_2 + \frac{T_5 - T_3}{R_7} = \frac{T_3 - T_4}{R_6} + \frac{T_3 - T_1}{R_4}, \tag{2}$$

$$\frac{T_3 - T_4}{R_6} + \frac{T_5 - T_4}{R_8 + R_9} = \frac{T_4 - T_2}{R_5}, \tag{3}$$

$$q_1 + \frac{T_3 - T_1}{R_4} = \frac{T_1 - T_2}{R_3} + \frac{T_1 - T_0}{R_1}, \tag{4}$$

$$\frac{T_1 - T_2}{R_3} + \frac{T_4 - T_2}{R_5} = \frac{T_2 - T_0}{R_2}, \tag{5}$$

$$T_0 = R_{\rm s} \sum_{i=1}^{3} q_i. \tag{6}$$

The resistances R_2, R_5, and R_8 are the thermal resistances of the filling material ($e.g.$, copper) of the TTSV. The resistances R_3, R_6, and R_9 denote the lateral thermal resistances of the insulator liner ($e.g.$, SiO_2) of the TTSV. The resistances R_1, R_4, and R_7 denote the thermal resistances of the surroundings of the TTSV (see Fig. 1(a)) for each of the three physical planes. The thermal resistance of the silicon substrate of the first plane is denoted by $R_{\rm s}$ due to the considerably different thickness of the substrate. These thermal resistances based on the physical parameters of the TTSVs are determined by

$$R_1 = \frac{1}{k_1 A}\left(\frac{t_{\rm D}}{k_{\rm D}} + \frac{l_{\rm ext}}{k_{\rm Si}}\right), \quad A = A_0 - \pi(r + t_L)^2, \tag{7}$$

$$R_2 = \frac{t_{\rm D} + l_{\rm ext}}{k_1 k_{\rm f} \pi r^2}, \tag{8}$$

$$R_3 = \int_0^{t_{\rm L}} \frac{1}{2\pi k_{\rm L}(t_{\rm D} + l_{\rm ext})(r + x)}\, dx = \frac{\ln(r + t_{\rm L}) - \ln r}{2\pi k_2 k_{\rm L}(t_{\rm D} + l_{\rm ext})} \tag{9}$$

$$R_4=\frac{1}{k_1 A}\left(\frac{t_{\rm D}}{k_{\rm D}}+\frac{t_{\rm Si_2}}{k_{\rm Si}}+\frac{t_{\rm b}}{k_{\rm b}}\right), \quad (10)$$

$$R_5=\frac{t_{\rm D}+t_{\rm Si_2}+t_{\rm b}}{k_1 k_{\rm f}\pi r^2}, \quad (11)$$

$$R_6=\frac{\ln(r+t_{\rm L})-\ln r}{2\pi k_2 k_{\rm L}(t_{\rm D}+t_{\rm Si_2}+t_{\rm b})}, \quad (12)$$

$$R_7=\frac{1}{k_1 A}\left(\frac{t_{\rm D}}{k_{\rm D}}+\frac{t_{\rm Si_3}}{k_{\rm Si}}+\frac{t_{\rm b}}{k_{\rm b}}\right), \quad (13)$$

$$R_8=\frac{t_{\rm Si_3}+t_{\rm b}}{k_1 k_{\rm f}\pi r^2}, \quad (14)$$

$$R_9=\frac{\ln(r+t_{\rm L})-\ln r}{2\pi k_2 k_{\rm L}(t_{\rm Si_3}+t_{\rm b})}, \quad (15)$$

$$R_s=\frac{t_{\rm Si_1}-l_{\rm ext}}{k_1 k_{\rm Si} A_0}. \quad (16)$$

The footprint area of the investigated structure is denoted by A_0, as shown in Fig. 1(a). The radius of the TTSV and the thickness of the insulator liner are denoted by r and $t_{\rm L}$, respectively. The thickness of the silicon substrate, the BEOL layer, and the bonding layer are denoted by $t_{\rm Si}$, $t_{\rm D}$, and $t_{\rm b}$, respectively. The thermal conductance of these layers, the liner and filler materials of the TTSV are denoted by $k_{\rm Si}$, $k_{\rm D}$, $k_{\rm b}$, $k_{\rm L}$, and $k_{\rm f}$, respectively. Since the horizontal heat transfer is more complex than the paths described by R_3, R_6, and R_9, the fitting coefficients k_1 and k_2 are used to decrease the discrepancy of the model from FEM simulations. If the TTSV extends into the silicon substrate in the first plane, this extended segment is denoted by $l_{\rm ext}$.

Substituting (7)-(16) into (1)-(6), the resulting temperature in the three planes can be determined. Due to the space limitations, the expressions of the resulting closed-form solutions for temperatures are not listed herein. Note that Model A can be extended to any number of planes. For a 3-D IC consisting of N planes, the TTSVs in the first plane are modeled by R_1-R_3. The TTSVs in the $N^{\rm th}$ plane are modeled by R_7-R_9. The TTSVs in other planes are modeled similar to R_4-R_6.

III. Distributed Thermal TSV Model

As mentioned before, the fitting coefficients k_1 and k_2 are required in Model A. This situation is due to the transfer of heat within one plane, which is modeled by three primary paths 1, 2, and 3, as shown in Fig. 1(b). To eliminate the need of fitting coefficients, Model A is extended to a distributed TTSV model (Model B). The lumped thermal resistors of each plane in Model A are replaced by distributed segments of thermal resistors. The resulting structures in the second plane are illustrated in Fig. 3. As demonstrated in this section, this model can be used to capture the thermal behavior of TTSVs with reasonable accuracy without curve fitting.

As illustrated in Fig. 3, the second plane is modeled by n_2 π-segments. There are $n_{\rm D2}$ segments for the ILD layer and $n_{\rm S2}$ segments for the silicon layer, where $n_2=n_{\rm D2}+n_{\rm S2}$. For an N-plane circuit, assuming there are n_A π-segments in total, $n_A=\Sigma_{i=1}^{N} n_i$. Consequently, there are $2n_A$ temperature nodes $(T_1,...,T_{2n_{\rm A}})$ and $3n_A$ resistances $(R_1,...,R_{3n_{\rm A}})$ for the entire circuit, as exemplified in Fig. 3. The heat generated in each plane is denoted by q_i $(1\le i\le N)$.

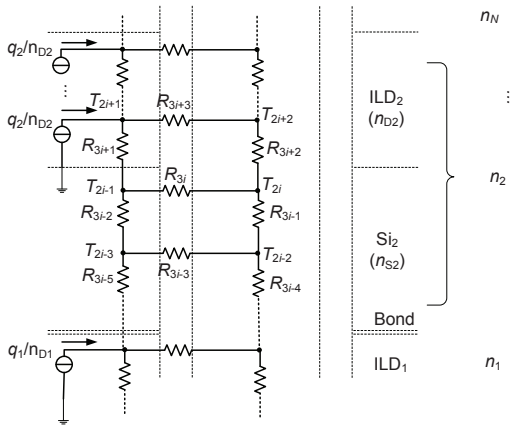

Fig. 3. Distributed thermal model of a TTSV in the second plane (Model B).

A set of expressions similar to (1) - (5) can be obtained at each temperature node using KCL. For example, for T_{2i-1} and T_{2i} in Fig. 3,

$$\frac{T_{2i+1}-T_{2i-1}}{R_{3i+1}}-\frac{T_{2i-1}-T_{2i}}{R_{3i}}-\frac{T_{2i-1}-T_{2i-3}}{R_{3i-2}}=0, \quad (17)$$

$$\frac{T_{2i+2}-T_{2i}}{R_{3i+2}}+\frac{T_{2i-1}-T_{2i}}{R_{3i}}-\frac{T_{2i}-T_{2i-2}}{R_{3i-1}}=0. \quad (18)$$

Consequently, a linear equation array can be obtained for a 3-D circuit,

$$\mathbf{A}\times\vec{T}=\vec{B}. \quad (19)$$

In (19), $\vec{T}$ is a $2n_{\rm A}\times 1$ vector corresponding to the temperatures $[T_1,T_2,...,T_{2n_{\rm A}}]'$. $\mathbf{A}$ is a $2n_{\rm A}\times 2n_{\rm A}$ matrix generated from the KCL expressions similar to (17) and (18). $\vec{B}$ is a $2n_{\rm A}\times 1$ vector corresponding to the heat input at each π-segment,

$$\forall_{1\le i\le 2n_{\rm A}}\, b_i\in\vec{B}, b_i=\begin{cases} q_j/n_{{\rm D}j}, & \text{if } b_i\in j^{\rm th}\text{ ILD},\\ 0, & \text{otherwise.}\end{cases} \quad (20)$$

The notation "$b_i\in j^{\rm th}$ ILD" implies that the node to which the $i_{\rm th}$ expression corresponds is in the $j^{\rm th}$ ILD layer.

The resistances $(R_1,...,R_{3n_{\rm A}})$ are the distributed resistances within each plane. For the $i^{\rm th}$ segment within the $j^{\rm th}$ plane, the related resistances are determined as follows,

$$\forall 1\le i\le n_{\rm A}, R_{3i-1}=R_{{\rm M}_j}/n_j,\ R_{3i}=n_j R_{{\rm L}_j}, \quad (21)$$

$$R_{3i-2}=\begin{cases} R_{{\rm ILD}_j}/n_{{\rm D}_j}, & \text{if } R_{3i-2}\in j^{\rm th}\text{ ILD},\\ R_{{\rm S}_j}/n_{{\rm S}_j}+R_{{\rm B}_j}, & \text{for the 1}^{\rm st}\text{ segment in S}_j,\\ R_{{\rm S}_j}/n_{{\rm S}_j}, & \text{otherwise.}\end{cases}$$

The horizontal resistance of the liner, the vertical resistances of the metal, the ILD, the silicon, and the bonding layer in the $j^{\rm th}$ plane are denoted by $R_{{\rm L}_j}, R_{{\rm M}_j}, R_{{\rm ILD}_j}, R_{{\rm S}_j}$, and $R_{{\rm B}_j}$, respectively. These resistances are obtained similar to (7) - (15) without k_1 and k_2.

Due to the limited space, the solution of the linear equation array (19) is omitted herein. By increasing $n_{\rm A}$, the heat transfer process related to the TTSV is more precisely described, while the time required to solve (19) also increases. A comparison of Model A and Model B is provided in the following section.

IV. Simulation Results and Discussion

The proposed models are compared with the results of a FEM tool [12]. The effect of the parameters related to TTSVs in the heat transfer process is also discussed in this section. Furthermore, a three-plane 3-D IC is thermally analyzed applying the proposed models.

The materials used for the ILD and bonding layers are assumed to be SiO_2 ($k_D = 1.4$ W/(m·K)) and polyimide ($k_b = 0.15$ W/(m·K)), respectively [6]. Since metal interconnects are embedded in the ILD, the k_D can be adapted to include the effect of the metal within the ILD layer. The liner of the TTSV is SiO_2 ($k_L = 1.4$ W/(m·K)). The footprint area, A_0, of the investigated 3-D circuit block is 100 μm $\times$ 100 μm. The thickness of the silicon substrate of the first plane is 500 μm and $l_{ext} = 1\,\mu$m. Without loss of generality, the temperature of the bottom surface of the circuit adjacent to the heat sink is assumed to be 27°C. The device heat sources are assumed to be uniformly distributed on the top surface of each silicon substrate and the power density is 700 W/mm^3 [13]. The heat generated by the interconnects is assumed to be uniformly distributed in each ILD layer with a power density of 70 W/mm^3. The filling material of the TTSV is copper ($k_f = 400$W/(m·K)). The reduction in temperature due to the TTSV is discussed in the following subsections where different parameters are varied. To emphasize the importance of considering the lateral heat transfer in the analytical thermal model of TTSV, the proposed models are also compared with a traditional 1-D heat transfer model [1], [2], [9].

A. Effect of the TTSV diameter

The effect of the diameter of the TTSV on the temperature reduction is discussed in this section. In the simulations, the radius of the TTSV, r, ranges from 1 μm to 20 μm. The other parameters are fixed except for t_{Si_2} and t_{Si_3}. Due to fabrication limitations, the aspect ratio of the TTSV (typically lower than ten [6], [15]) has to be adapted according to the variation of r. The plots "Model A", "Model B (100)", "1-D", and "FEM" denote the results of Model A, Model B with 100 segments in planes 2 and 3, the traditional 1-D model, and the FEM tool, respectively.

As illustrated in Fig. 4, the maximum temperature rise ΔT decreases as the diameter (or radius) of the TTSV increases. When r increases, as shown in (7)-(16), the resistances R_2, R_3, R_5, R_6, R_8, and R_9 significantly decrease. Consequently, the resulting temperature T_5 (see Fig. 2) decreases.

In Fig. 4, compared with the FEM, the maximum difference (absolute value) in the steady-state temperature of Model A, Model B (100), and 1-D model is 6%, 11%, and 21%, respectively. The average difference is 3%, 3%, and 13%, respectively. Model A is more accurate than Model B, since in the first model fitting coefficients are adopted to decrease the discrepancy. Model B, however, also achieves reasonably high accuracy without the need of fitting coefficients. The 1-D model also captures the relation between r and ΔT, but the error is higher when the aspect ratio is high. This situation is because as the aspect ratio increases, the lateral heat transfer becomes nontrivial as compared with the vertical flow of heat. Consequently, neglecting path 2 (see Fig. 1(b)) introduces a higher error.

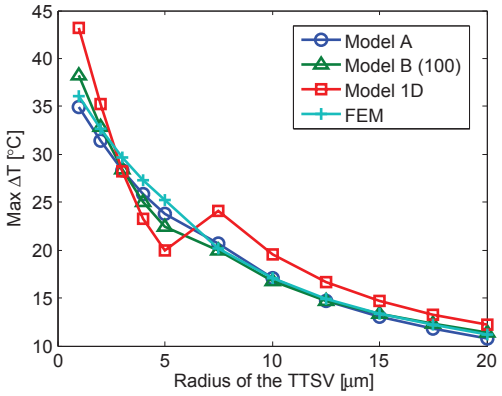

Fig. 4. Maximum temperature rise in a three-plane 3-D IC due to different TTSV radius. $t_L = 0.5\,\mu$m, $t_D = 4\,\mu$m, $t_b = 1\,\mu$m. For $1\,\mu\text{m} \le r \le 5\,\mu$m, $t_{Si_2} = t_{Si_3} = 5\,\mu$m; for $5\,\mu\text{m} < r \le 20\,\mu$m, $t_{Si_2} = t_{Si_3} = 45\,\mu$m. $k_1 = 1.3$, and $k_2 = 0.55$.

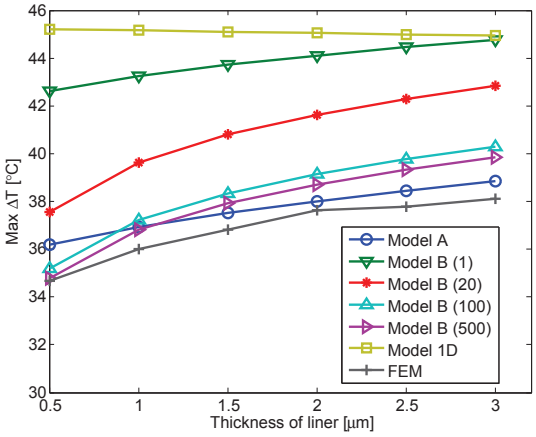

Fig. 5. Maximum temperature rise in a three-plane 3-D IC for different thickness of the dielectric liner, where $r = 5\,\mu$m. The other parameters are $t_D = 7\,\mu$m. $t_b = 1\,\mu$m, $t_{Si_2} = t_{Si_3} = 45\,\mu$m. $k_1 = 1.3$ and $k_2 = 0.55$.

B. Effect of the thickness of the dielectric liner

The effect of the thickness of the dielectric liner surrounding the TTSV on the temperature reduction is discussed in this section. The dielectric liner ranges from 0.5 μm to 3 μm. The other parameters are provided in Fig. 5.

As shown in Fig. 5, the thickness of the TTSV dielectric liner considerably affects the resulting temperature, a behavior not captured by the conventional 1-D thermal TTSV model. For different t_L, the ΔT from FEM differs up to 11%, which is approximately 4°C for this specific setup.

As expressed by (9), (12), and (15), the resistances R_3, R_6, and R_9 increase as t_L increases. The resulting temperatures, consequently, increase significantly. These resistances R_3, R_6, and R_9 increase linearly with $\ln t_L$. Consequently, the change of ΔT with t_L is smaller than the change of ΔT with r. Since the traditional TTSV model only considers vertical 1-D heat

TABLE I
THE ERROR AND RUN TIME VS. # OF SEGMENTS IN MODEL B.

Model	B (1)	B (20)	B (100)	B (500)	A	1-D
Max. Error	23%	12%	6%	5%	4%	30%
Av. Error	19%	11%	4%	3%	2%	23%
Time [ms]	1	3	32	2475	-	-

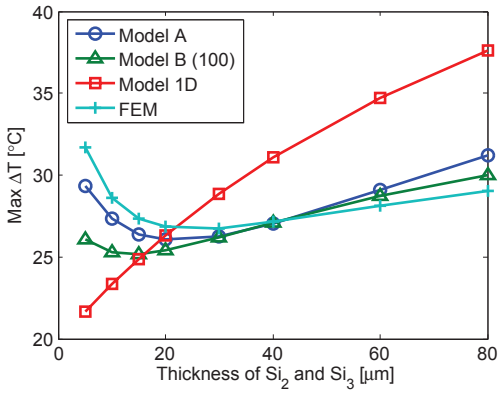

Fig. 6. Maximum temperature rise in a three-plane 3-D IC due to different thickness of the silicon substrate. The other parameters are $t_{\mathrm{L}} = 1\,\mu$m, $t_{\mathrm{D}} = 7\,\mu$m, $t_{\mathrm{b}} = 1\,\mu$m, $r = 8\,\mu$m, $k_1 = 1.3$ and $k_2 = 0.55$.

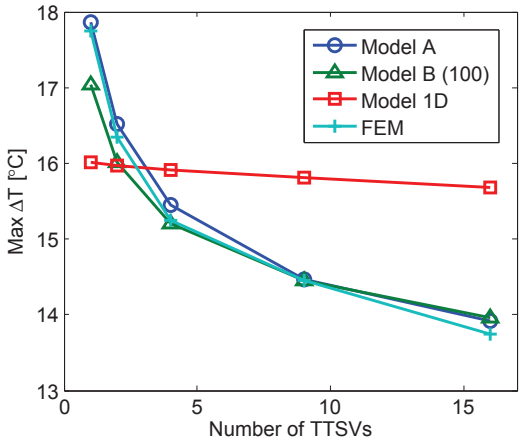

Fig. 7. Maximum temperature rise in a three-plane 3-D IC due to different thickness of the silicon substrate. $t_{\mathrm{L}} = 1\,\mu$m, $t_{\mathrm{D}} = 4\,\mu$m, $t_{\mathrm{b}} = 1\,\mu$m, $t_{\mathrm{Si_2}} = t_{\mathrm{Si_3}} = 20\,\mu$m, $r_0 = 10\,\mu$m, $k_1 = 1.3$, and $k_2 = 0.55$.

transfer through the liner [1], [7], [8], the lateral or horizontal heat transfer is ignored.

For various t_{L}, different number of segments are investigated for Model B. The numbers of segments within the first plane and the other planes are (1, 1), (2, 20), (10, 100), and (50, 500), respectively, as denoted by Model B (1) - Model B (500). The maximum and average difference in the temperature between the four cases and FEM are reported in Table I. The run time for these four cases is also reported. The accuracy of Model B increases with the number of segments within each plane, while the run time also increases significantly.

C. Effect of the thickness of the silicon substrate

The effect of the thickness of the silicon substrate ($t_{\mathrm{Si_2}}$ and $t_{\mathrm{Si_3}}$) on the temperature reduction is discussed in this section. For 1-D heat transfer models, the temperature increases as $t_{\mathrm{Si_2}}$ and $t_{\mathrm{Si_3}}$ increase. The results of FEM simulations, however, exhibit a different behavior.

The change of ΔT according to different $t_{\mathrm{Si_2}}$ and $t_{\mathrm{Si_3}}$ is illustrated in Fig. 6. The thickness of the silicon substrate ranges from 5 μm to 80 μm. The other parameters are listed in Fig. 6. ΔT changes non-monotonically with the thickness of the silicon substrates, another behavior that cannot be described by the 1-D heat transfer model. As illustrated in Fig. 6, within the range $5\,\mu\mathrm{m} \leq t_{\mathrm{Si_2}} \leq 20\,\mu$m, ΔT decreases as $t_{\mathrm{Si_2}}$ increases. For $t_{\mathrm{Si_2}} > 20\,\mu$m, ΔT increases with $t_{\mathrm{Si_2}}$.

Both Model A and Model B capture this behavior. As described by (10)-(16), the vertical thermal resistances (R_4, R_5, R_7, and R_8) in Fig. 2 increase as $t_{\mathrm{Si_2}}$ and $t_{\mathrm{Si_3}}$ increase, which implies that the thermal resistance along the vertical path of the heat transfer increases. Nevertheless, the horizontal thermal resistances described by (12) and (15) decrease as $t_{\mathrm{Si_2}}$ and $t_{\mathrm{Si_3}}$ increase, which indicates that the thermal resistance along the horizontal path of the heat transfer through the liner of the TTSV decreases. The combination of these two effects leads to the non-monotonic change in temperature. Consequently, thinning the silicon substrate cannot always improve the heat transfer within a 3-D IC with TTSVs, since wafer thinning limits the lateral spreading of heat within the substrate [14].

As shown in Fig. 6, the average error of Model A, Model B (100), and 1-D model is 4%, 6%, and 17%, respectively. The maximum error is 7%, 18%, and 32%, respectively. When the silicon layer is thin, all the models introduce a high error.

D. Effect of dividing a large TTSV into multiple thin TTSVs

The effect of dividing a large TTSV into a cluster of thinner TTSVs on the temperature reduction is discussed in this section. Several works have shown that by replacing a large-diameter TTSV with a cluster of small-diameter TTSVs, the temperature of a 3-D IC can be further reduced [13].

While dividing a TTSV into a cluster of thin TTSVs, the total area of the metal forming the TTSVs is assumed to be the same. As a result, if a TTSV with radius r_0 is divided into n TTSVs, the radius of the new TTSVs is $r_n = \frac{r_0}{\sqrt{n}}$. The other parameters remain the same. In the proposed model, the new cluster of TTSVs is modeled as an equivalent thermal resistance network $R'_i\,(1 \leq i \leq 9)$. Since the total metal area within the TTSVs remains the same, the vertical thermal resistances remain the same, $R'_i = R_i\,(i \neq 3, 6, 9)$. The horizontal resistances are updated from (9) as the total lateral surface of the TTSVs increases,

$$R'_3 = \frac{\ln(t_{\mathrm{L}}\sqrt{n} + r_0) - \ln r_0}{2n\pi k_2 k_{\mathrm{L}}(t_{\mathrm{D}} + l_{\mathrm{ext}})}. \tag{22}$$

R'_6 and R'_9 are updated similar to (22). In the simulations, a TTSV is divided into 2, 4, 9, and 16 TTSVs.

As shown in Fig. 7, ΔT decreases as a single TTSV is divided into more TTSVs. This behavior is because as a TTSV is divided into more TTSVs, the total lateral surface increases

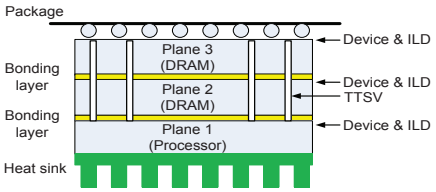

Fig. 8. A three-plane 3-D circuit with TTSVs. $t_{\mathrm{L}} = 1\,\mu\mathrm{m}, t_{\mathrm{D}} = 20\,\mu\mathrm{m}$, $t_{\mathrm{b}} = 10\,\mu\mathrm{m}, t_{\mathrm{Si}_1} = t_{\mathrm{Si}_2} = t_{\mathrm{Si}_3} = 300\,\mu\mathrm{m}$, $r = 30\,\mu\mathrm{m}$, $k_1 = 1.6, k_2 = 0.8$, and $c_{1,2} = 3.5$.

and more heat is conducted through the TTSVs. According to (22), as n increases, R'_3, R'_6, and R'_9 decrease, which causes the temperature to decrease. As depicted by the three plots, the decrease in temperature with the number of TTSVs saturates as n increases. Consequently, dividing a TTSV into more and thinner TTSVs exhibits a diminishing improvement after a specific n.

The average error of Model A, Model B (100), and 1-D model is 1%, 2%, and 8%, respectively. The maximum error is 1%, 4%, and 14%, respectively. As illustrated in Fig. 7, both of Model A and Model B correctly describe the expected behavior of dividing a TTSV. Since the area of the metal forming the TTSV remains the same for any n, the 1-D model cannot describe the temperature reduction with n.

E. 3-D DRAM-μP Case Study

The proposed models are used to evaluate the temperature rise in a 3-D circuit. The physical parameters of the circuit are based on [9], [13], where a 1-D heat transfer model is used for the system. The circuit consists of three physical planes with face-to-back bonding. The footprint area is 10 mm $\times$ 10 mm. The thickness of the silicon substrate (t_{Si}) in each plane is 300 μm. The power dissipated by the μP and DRAM planes is 70 W and 7 W, respectively. The TTSVs are uniformly distributed with a density of 0.5% of the total circuit area. The proposed models are embedded in the analytic thermal analysis model of the system. The FEM simulation and 1-D TTSV model are also implemented for comparison. The structure of the circuit and the other parameters are illustrated in Fig. 8.

Since $t_{\mathrm{Si}} = 300\,\mu\mathrm{m}$, the TTSVs in the second and third planes are divided into 1000 segments for Model B. For the investigated 3-D circuit, the resulting maximum temperature rise from the heat sink for Model A, Model B (1000), FEM, and 1-D model are 12.8°C, 13.9°C, 12°C, and 20°C, respectively. The runtime of FEM is 59 minutes. The fitting coefficients of Model A are determined by the simulation of a block of the investigated circuit as shown in Fig. 1, the runtime of which is 1.9 minutes. The runtime for Model B (1000) is 8.5 seconds. As demonstrated by this example, the proposed models are efficient and reasonably accurate while the 1-D model is highly inaccurate even for this first-order analysis.

V. Conclusions

Two analytic models for TTSVs are presented. Model A is more accurate in estimating the effect of the parameters of TTSVs on the temperature reduction. Model B provides concise expressions to estimate this effect without any fitting coefficients. The accuracy of these models is compared with FEM simulations. For an investigated three-plane circuit, the average error of the first and the second model for varying all TTSV physical parameters is 2% and 4%, respectively.

The effect of the diameter of TTSVs, the thickness of the dielectric liner, and the thickness of the silicon substrate are investigated, respectively. Ignoring these effects can result in significant overestimate of the temperature increase in 3-D ICs where TTSVs are utilized, as demonstrated by a first-order thermal analysis of a 3-D DRAM-μP system. Adapting a 1-D model, therefore, in a TTSV insertion/planning methodology can result in excessive usage of TTSVs (a critical resource in 3-D ICs), with an immediate increase in the cost of the total system.

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