Testing of High-Speed DACs using PRBS Generation with "Alternate-Bit-Tapping"

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***Abstract*—Testing of high-speed Digital-to-Analog Converters (DACs) is a challenging task, as it requires large number of high-speed synchronized input signals with specific test patterns. To overcome this problem, we propose use of PRBS signals with an "Alternate-Bit-Tapping" technique and eye-diagram measurement as a solution to efficiently generate the test-vectors and test the DACs. This approach covers all levels and transitions necessary for testing the dynamic behavior of the DAC completely, in minimum possible time. Circuit level simulations are used to verify its usefulness in testing a 4-bit 20-GS/s current-steering DAC.**

I. Introduction

To increase the capacity by improving spectral efficiency, multi-level modulation formats are being explored in wireless, wired and optical communication systems [1]–[3]. High-speed Digital-to-Analog Converters (DACs) become an important part of such systems as they are needed to generate the multi-level signals. While testing of high-speed DACs is in itself very challenging, generation of multi-level random test signals that thoroughly evaluate these new high-speed communication links is yet another difficult problem. For example, a very costly electrical-optical-electrical conversion technique had to be used in [4] to generate high-speed 8-level signals for a 64-QAM 112-Gb/s optical transmission experiment.

Ramp and sinusoidal signal generation techniques have widely been used for the purpose of DAC testing [5]–[7]. However, sinusoidal test pattern generation may consume a lot of area and power when implemented at high speeds. More importantly, these test schemes do not emulate the random nature of the data used in broadband communications links and are insufficient for determining the dynamic behavior of the DACs. For example, even when the magnitude response of a DAC is constant for different frequencies, the signal can get distorted due to group delay dispersion and/or dynamic non-linearity [8]. In particular, the dynamic behavior becomes important at high-speeds since small parasitic components in the circuits can significantly affect the high frequency components in the signals [9]. Hence, the existing test techniques cannot be used to fully predict the dynamic (linear as well as non-linear) behavior of a DAC and its affect when the DAC is used in a communication link.

To overcome this problem, exhaustive testing of high-speed DACs using PRBS (Pseudo Random Bit Sequence) data has been suggested in this paper to ensure their proper operation. Traditionally, PRBS generator has been used to test many digital and analog circuits [10], [11] but not for DAC testing as it does not cover all transitions between output levels although can cover almost all output levels. Additionally, the output of the DAC for random input bit-streams may not be easy to analyze in general. In this paper, we aim at using the PRBS generator in such a way that the DAC output can cover all possible output levels as well as transitions between them. This has been achieved by using a 2m-bit PRBS generator (with Maximum Length Sequence output) to test an m-bit DAC, using the proposed technique. To evaluate the multi-level pseudo-random DAC output, eye-diagram measurement can be used as the technique is very helpful in performing an intuitive analysis of system behavior such as slew rate [12]. Wide opening in the eye-diagram of the DAC output is required for obtaining good quality multi-level signal for a communication link. It may be noted that proposed technique can be useful only in evaluating low resolution DACs, as it would not be easy to measure the multi-level eye diagrams if the number of levels is very large because of limited resolution of the measurement instrument.

Please note that in the remainder of the paper; 'DAC' refers to high-speed DACs unless explicitly mentioned. The paper is organized as follows: Section 2 emphasizes on the need to have an exhaustive testing of high-speed DACs and describes our proposed "Alternate-Bit-Tapping" technique. In section 3, the technique has been implemented and presented simulation results have been discussed. Section 4 concludes the paper.

II. DAC testing using Proposed Approach

A typical m-bit PRBS generator made of LFSR (Linear Feedback Shift Register) can be used to generate $2^m - 1$ different sequences to test an m-bit DAC and cover all-but-one test-vectors. However, generated test-vectors follow a fixed transition pattern, hence all transitions cannot be covered. This is not a major concern when eye-diagram measurement is for low-speed applications where dynamic behavior is not important, but at high-speed it becomes vital. Integral Non-Linearity (INL), Differential Non-Linearity (DNL), offset and gain-error are a few parameters that characterize a DAC. But, in high-speed DACs the settling time also stands as a crucial deciding factor, as it decides the analog voltage level achieved at the output of DAC. The effect of transition time can be

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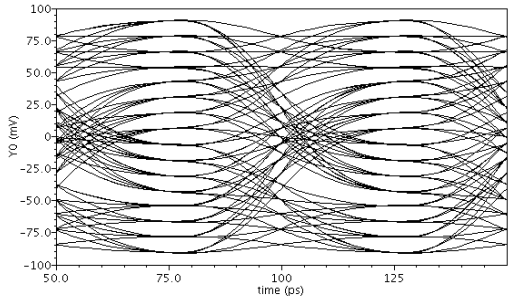
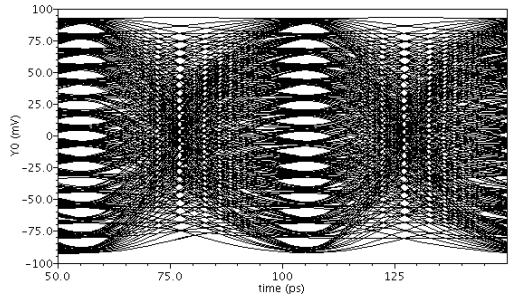


(a) A 4-bit DAC output tested by a 6-bit PRBS (or an incorrectly tapped $\geq$ 8-bit DAC)



(b) A 4-bit DAC output tested by an 8-bit PRBS.

Fig. 1. Eye-diagram comparison for the output of a 4-bit DAC when tested with (a) not all transitions (b) almost all transitions using our proposed technique.

easily seen in the form of eye opening in any eye-diagram. If all transitions are not covered then it makes it difficult to visualize the device performance. Simulation results in Fig. 1 show the importance of covering all transitions by means of an eye-diagram.

Figure 1(a) shows the simulation result for a 4-bit DAC run by a 6-bit LFSR, covering only 63 out of 256 transitions between test-vectors. (PRBS generator' and 'LFSR' have been used interchangeably at many places in the paper; they in this paper mean a PRBS generator using LFSR configuration producing a Maximum Length Sequence (MLS)). Figure 1(b) shows the same DAC tested with an 8-bit LFSR covering 255 out of 256 possible transitions. The eye-opening in Fig. 1(a) is 9.93mV–12.10mV whereas it is 6.07mV–6.76mV in Fig. 1(b) for almost same output swing. Hence, from the above comparison we can conclude that improper testing (Fig. 1(a)) can lead to wrong characterization of the device under test and hence this makes the proper testing (Fig. 1(b)) vital. Wrongly tapped 8-bit LFSR will also result in incomplete transitions like a 6-bit LFSR.

A. Alternate-Bit-Tapping Technique

The aim of this *"Alternate-Bit-Tapping"* technique is to test high speed DACs using PRBS generator with all test-

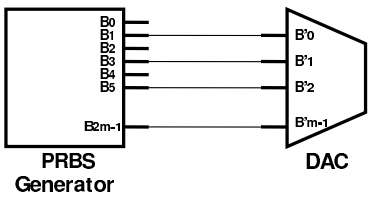


Fig. 2. A 2m-bit PRBS generator (with MLS output) for testing an m-bit DAC by our proposed technique.

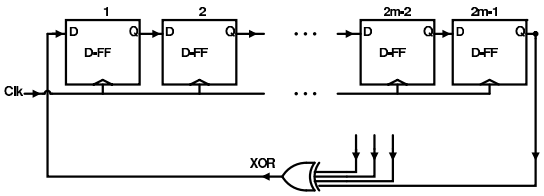


Fig. 3. An m-bit PRBS generator using an LFSR.

vectors and transitions between these test vectors (except 0-0 transition), in minimum number of cycles. It states that *"For testing of an m-bit DAC with all transitions between all possible output levels of DAC covered (except 0-0 transition), a 2m-bit LFSR (with Maximum Length Sequence output) is required with its bits tapped alternately and fed to the DAC input"*. These bits can be all even or all odd bits of PRBS generator. It also guarantees to be the necessary and sufficient condition for the same and is done within minimum time (discussed later). Also, all DACs of m-bit or less can be tested reusing the same PRBS generator of size 2m-bit, adding to the advantages of this technique.

B. Linear Feedback Shift Register (LFSR)

If an m-bit PRBS generator is constructed using an LFSR, the maximum sequence length that can be obtained is $2^m - 1$ [13]. As shown in Fig. 3 a PRBS generator made from LFSR consists of a shift-register made up of cascaded memory element like a flip-flop with the output of the last element XORed with that of one or more intermediate memory element outputs, and fed to the input of the shift-register to get the PRBS.

C. Maximum Length Sequence (MLS)

For an m-bit LFSR, the maximum possible outcome can be 2^m bit-vectors or states. But, a state with bit-vector containing all '0's, will keep on repeating itself not allowing any other state to occur (as the XOR output will always be '0'). Hence, the maximum number of states that can occur is limited to 2^m-1, which is the time-period of the MLS generated by LFSR.

An important thing to note at this point is that all XOR tapping configurations do not lead to MLS, but only a few do. To get these MLS of period 2^m-1, a primitive polynomial h(x) of degree m is required [14]. The algebraic terms occurring in this polynomial represent the LFSR tapping positions for MLS. A primitive polynomial is an irreducible polynomial of

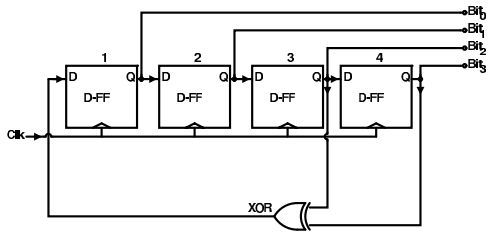


Fig. 4. A 4-bit PRBS generator using an LFSR.

TABLE I
PRIMITIVE POLYNOMIALS FOR $m \leq 39$ USED TO OBTAIN MLS FOR AN LFSR [16]

m	*h(x)*	*m*	*h(x)*
2	$x^2 + x + 1$	21	$x^{21} + x^{19} + 1$
3	$x^3 + x^2 + 1$	22	$x^{22} + x^{21} + 1$
4	$x^4 + x^3 + 1$	23	$x^{23} + x^{18} + 1$
5	$x^5 + x^3 + 1$	24	$x^{24} + x^{23} + x^{21} + x^{20} + 1$
6	$x^6 + x^5 + 1$	25	$x^{25} + x^{22} + 1$
7	$x^7 + x^6 + 1$	26	$x^{26} + x^{25} + x^{24} + x^{20} + 1$
8	$x^8 + x^6 + x^5 + x^4 + 1$	27	$x^{27} + x^{26} + x^{25} + x^{22} + 1$
9	$x^9 + x^5 + 1$	28	$x^{28} + x^{25} + 1$
10	$x^{10} + x^7 + 1$	29	$x^{29} + x^{27} + 1$
11	$x^{11} + x^9 + 1$	30	$x^{30} + x^{29} + x^{26} + x^{24} + 1$
12	$x^{12} + x^{11} + x^8 + x^6 + 1$	31	$x^{31} + x^{28} + 1$
13	$x^{13} + x^{12} + x^{10} + x^9 + 1$	32	$x^{32} + x^{30} + x^{26} + x^{25} + 1$
14	$x^{14} + x^{13} + x^{11} + x^9 + 1$	33	$x^{33} + x^{20} + 1$
15	$x^{15} + x^{14} + 1$	34	$x^{34} + x^{31} + x^{30} + x^{26} + 1$
16	$x^{16} + x^{14} + x^{13} + x^{11} + 1$	35	$x^{35} + x^{33} + 1$
17	$x^{17} + x^{14} + 1$	36	$x^{36} + x^{25} + 1$
18	$x^{18} + x^{11} + 1$	37	$x^{37} + x^{36} + x^{33} + x^{31} + 1$
19	$x^{19} + x^{18} + x^{17} + x^{14} + 1$	38	$x^{38} + x^{37} + x^{33} + x^{32} + 1$
20	$x^{20} + x^{17} + 1$	39	$x^{39} + x^{35} + 1$

that degree. For example, for a 4-bit LFSR, tapping the output of 4th and 3rd register (Fig. 4), the primitive polynomial is h(x) = $x^4 + x^3 + 1$. Change in primitive polynomial leads to change in the occurring output sequence.

Reference [15] gives a detailed analysis that, there surely exists a primitive polynomial of degree m for every m. In other words, every LFSR will have at least one configuration with an MLS. Table I shows these primitive polynomials for $m \leq 39$ starting from $m = 2$, made from the tapping data taken from [16]. Much higher degree primitive polynomials have been found by Zierler & Brillhart [17].

D. Example: Testing of a 2-bit DAC using a 4-bit LFSR

This example aims at giving an insight to the working of the technique. Table II shows the states of a 4-bit LFSR with a maximum length sequence (MLS). The binary output of the LFSR is displayed in the STATE column of Table 2. The B_2 and B_0 of LFSR are tapped and fed to DAC input. Now, considering the state 3 in the table which represents a binary equivalent of $(9)_{10}$ in LFSR, this output is fed as a binary equivalent of $(1)_{10}$ to the DAC. It is clearly visible from the table that in state 4, the DAC input i.e. $(2)_{10}$ comes from $B_2 = 1$ and $B_0 = 0$, which is just a time-shifted version of state 3 with $B_3 = 1$ and $B_1 = 0$. Hence, it can be said that the bit-vector in state 3(value=$(9)_{10}$) contains both the current state value $(1)_{10}$ as well as the next state value $(2)_{10}$ available at

TABLE II
OUTPUT SEQUENCE OF A 4-BIT LFSR USED TO TEST A 2-BIT DAC

State No.	STATE B_3	B_2	B_1	B_0	LFSR Output (BASE 10)	DAC INPUT (BASE 10)
0	1	0	0	0	8	0
1	0	1	0	0	4	2
2	0	0	1	0	2	0
3	1	0	0	1	9	1
4	1	1	0	0	12	2
5	0	1	1	0	6	2
6	1	0	1	1	11	1
7	0	1	0	1	5	3
8	1	0	1	0	10	0
9	1	1	0	1	13	3
10	1	1	1	0	14	2
11	1	1	1	1	15	3
12	0	1	1	1	7	3
13	0	0	1	1	3	1
14	0	0	0	1	1	1
15=0	1	0	0	0	8	0
16=1	0	1	0	0	4	2

the DAC input, or in other words represents a transition. From the appearance of similar exclusive states in LFSR table it can be concluded that it gives rise to an exhaustive appearance of all transition in the period of MLS. In full table, the input to DAC appears to be $(1)_{10}$ at four places for different LFSR outputs, and hence covers all four possible transitions. This last part has been further clarified in the next section.

E. Sufficient & Necessary Condition

By sufficient condition, we mean that this technique covers all test-vectors and transitions between them (except 0–0 transition). Whereas, necessary means that it is not possible to test an m-bit DAC using a PRBS generator which is less than 2m-bit long without any other additional circuitry.

1) Sufficient Condition: Each state in an MLS produced by 2m-bit LFSR represents a unique bit combination $[B_0B_1B_2B_3B_4B_5B_6B_7B_{2m-2}B_{2m-1}]$, for a 2-m bit LFSR [10]. This bit-vector repeats itself only after the period of this MLS, i.e. $2^m - 1$ cycles. Now, dividing the LFSR output into odd and even bit-vectors we get: $[B_1B_3B_5B_7B_{2m-1}], [B_0B_2B_4B_6B_{2m-2}]$; which is a unique bit-vector pair, occurring only once in an MLS period. Now, suppose that $[B_1B_3B_5B_7B_{2m-1}]$ represents the current state input being fed to DAC and the next state input be $[B'_1B'_3B'_5B'_7B'_{2m-1}]$. As in a typical LFSR, leaving the inputs fed at B_0, rest of the bits are shifted by one in the next transition (Fig. 5). Which means, $[B'_1B'_3B'_5B'_7B'_{2m-1}] = [B_0B_2B_4B_6B_{2m-2}]$. So, from this it can be concluded that each LFSR bit-vector of length 2m represents a bit-vector transition. By the property of LFSR stated before, this (and hence all) transition can be assured to occur once in an MLS cycle.

For example, an 8-bit LFSR with a bit-vector [1 0 0 0 1 0 1 1] represents DAC current state input, S_i = [0 0 0 1] and a next

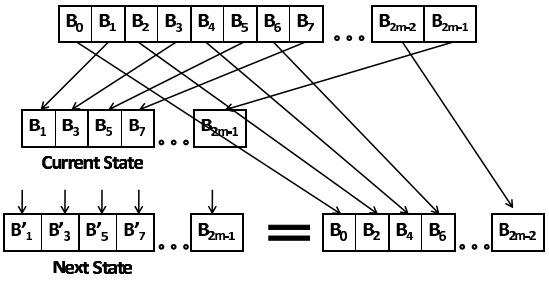


Fig. 5. State of a 2m-bit LFSR, representing transition between mutually independent current and next state of an m-bit DAC input

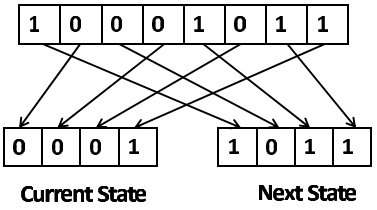


Fig. 6. Example of a state of 8-bit LFSR representing a transition between mutually independent current and next state of a 4-bit DAC input

state input, S_{i+1} = [1 0 1 1] (Fig. 6). As all 8-bit combinations (except [0 0 0 0 0 0 0 0]) will be covered (at least & only once) in one cycle of MLS. This means that the states S_i and S_{i+1} can and will take all possible values independent of each other. Thus, they will represent all possible transitions from all current states to all next states required to test a 4-bit DAC.

2) Necessary Condition: For the testing of an m-bit DAC, if an LFSR of less than 2m bit is taken, then at least one or more tapped bits will be adjacent, except for the case of a 2m-1 bit LFSR discussed in the next section. Now, as the next state binary value of an LFSR is just a shifted version of current state binary value; this adjacent tapping puts a limitation on the possible next state values.

For example, consider a 6-bit LFSR testing a 4-bit DAC with output bits tapped at B_1, B_3, B_4 & B_5. Let the current state be [1 0 1 0] (Fig. 7). For this current sate the LFSR outputs will be [X 1 X 0 1 0], where X represents an unknown output. The LFSR next state output (after shifting all bits by one) leads to the possible next state of [X X 0 1], freezing the last bits to '0' and '1'. Hence, we can say that this DAC input may have only one-fourth of the possible next states, or in other words a DAC input of $(A)_{16}$ can only be followed by $(2)_{16}, (6)_{16}, (9)_{16}$ or $(E)_{16}$. This restricts the transitions and makes "alternate-bit-tapping" a necessary criterion to cover almost all transitions. By analogy, all LFSRs which do not satisfy the stated criteria will lead to lesser number of transitions.

Even a PRBS generator greater than 2m-bit can be used for testing an m-bit DAC but this increases the testing time (which is the period of MLS) and required area. So, this means that if we have more than one DAC on chip, then for BIST purpose we can reuse the same LFSR provided its size is $\geq 2m$ where

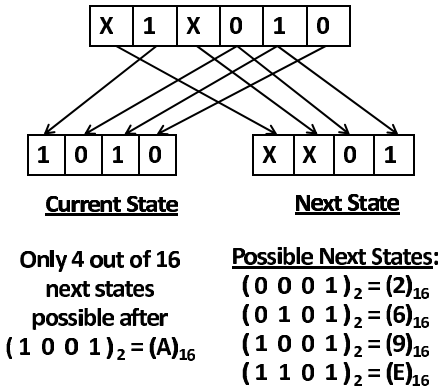


Fig. 7. Example showing possible next states after $(A)_{16}$ for a 4-bit DAC when tested by 6-bit LFSR. Not following the proposed technique leads to missing transitions.

m is the number of bits of maximum-size DAC.

F. 2m-1 bit LFSR for m-bit DAC

In this special case of alternate bit tapping, the bits are tapped alternately from edge to edge, like tapping bits $[B_0B_2B_4B_6]$ for an LFSR with $[B_0B_1B_2B_3B_4B_5B_6]$. Even with alternate bits, this configuration does not cover all transitions as it uses a less than 2m-bit LFSR to test an m-bit DAC. Suppose, the current (2m-1)-bit LFSR output to be $[B_0B_1B_2B_3B_4 \ldots B_{2m-2}]$. This means that the current state will be $[B_0B_2B_4 \ldots B_{2m-2}]$ and next state $[YB_1B_3 \ldots B_{2m-3}]$, where Y represents the XOR output. This Y is hence a dependent value which is a function of current and next state values.

For example, consider a 7-bit LFSR with MLS used to test a 4-bit DAC (Fig. 8). Let, the current DAC input be [1 0 0 1] and hence the LFSR output be [1 X 0 X 0 X 1]. As from table I, the XOR output, $Y = B5 \bigoplus B6$, possible Y values can be evaluated. Hence, possible next states allowed after [1 0 0 1] are [1 X X 0] & [0 X X 1]. Thus, states [1 X X 1] & [0 X X 0] are never allowed to follow [1 0 0 1]. Similarly, other states too will have transitions missing.

There can be an alternate way to look at this. As stated before, in "alternate-bit-tapping" an LFSR bit-vector represents a transition. Hence, maximum possible transitions in this case = $2^{2m-1} - 1$. Total required transitions to cover all transition-pairs for an m-bit DAC= $2^m * 2^m = 2^{2m}$. Thus, this case of 7-bit LFSR to test a 4-bit DAC covers only around half of the required transitions.

G. Minimum time testing

An m-bit DAC has 2^m levels, which leads to total $2^m * 2^m = 2^{2m}$ transitions, and $2^{2m} - 1$ transitions on leaving 0–0 transition. By our proposed technique we can cover $2^{2m} - 1$ LFSR states, where each state represents a unique transition as stated before. Thus, all possible $2^{2m} - 1$ transitions occur exclusively and exhaustively in $2^{2m} - 1$ cycles. So, this proves that this technique makes use of minimum time required to cover all transitions.

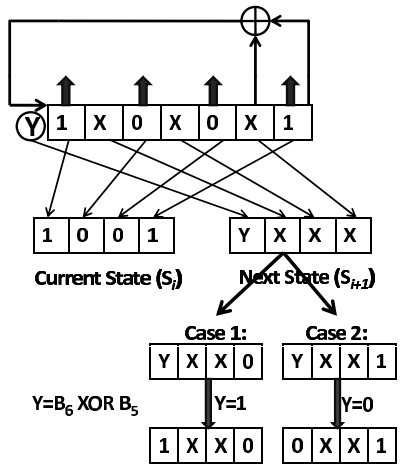


Fig. 8. Missing transitions when an m-bit DAC is tested by (2m-1)-bit LFSR.

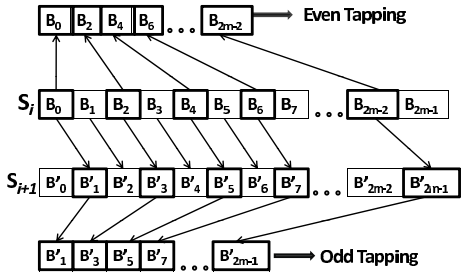


Fig. 9. DAC testing by tapping odd and even bits of an LFSR. Odd bits are just one clock delayed values of even bits.

H. Discussion

As the occurrence of a 0–0 transition would mean that both the current and next-state are bit vectors with all bits '0'. This is possible only when all LFSR bits are '0', which does not occur in the MLS (hence a period of $2^{bits} - 1$). This makes the 0–0 a non-occurring transition for our testing methodology. However, the 0–0 transition is not really required for characterizing the dynamic behavior of the DAC. Hence, nothing is actually lost by losing 0–0 transition.

Tapping at odd or even bits of LFSR makes no difference as odd bits represent just one clock delayed version of the bit-vector available at even bits (Fig. 9).

The eye-diagram can also be used to calculate DNL, INL and other static characteristics of DAC. Eye-diagram technique is very well suited particularly for testing of low-resolution high-speed DAC applications which require $DNL < 1LSB$.

All the analysis performed in this paper assumes that the next state value is affected only by the current state value and not by the states before. If in any case we encounter a circuit where this assumption fails and the next-state value depends on the current state and the state before current state as well, we can analogically go for a 3rd bit tapping technique which will hold equally good for the corresponding situation. This technique can be further extended to nth-bit tapping technique using an nm-bit LFSR to test an m-bit DUT which depends on n-1 states before current state to cover almost all possibilities.

TABLE III
STATE TRANSITION TABLE OF A 4-BIT DAC TESTED USING AN 8-BIT LFSR BY 'ALTERNATE-BIT-TAPPING' TECHNIQUE IN MATLAB

Current State \ Next State	S_0	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}	S_{15}
S_0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S_1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S_2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S_3	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S_4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S_5	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S_6	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S_7	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S_8	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S_9	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S_{10}	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S_{11}	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S_{12}	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S_{13}	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S_{14}	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S_{15}	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Along with these applications, this technique can be extended to testing of analog memories and detection of floating gate faults. References [18]–[20] show a few architectures of a typical analog memory cell, from which it is quite evident that the settling time and hence the achieved analog value by analog memory cells depends on the previous value, thus making an exhaustive testing necessary (as in a high-speed DAC). A floating gate fault has been discussed in [21]. The value in such a fault is influenced by its environment consisting of potentials and capacitances [18] and the previous value, thus making it behave like a sequential circuit. This change may or may not be visible at the circuit output depending upon the other inputs. Thus, "alternate-bit-tapping" can be a good solution to test such faults.

III. SIMULATION RESULTS

The above stated methodology was verified by simulation using MATLAB for up to 8-bit DAC using 16-bit LFSR using possible LFSR-4 and LFSR-2 combinations.

Table III shows the transition-table plotted from MATLAB for a 4-bit LFSR to run 2-bit DAC. The rows of the table represent the current state while the columns represent the next state of DAC under test. The '0' at left-top represents the non occurring 0–0 transition, whereas '1' in other cells confirms the occurrence of that transition.

A 4-bit DAC with current-steering architecture (Fig. 10) was designed in UMC-90nm technology using cadence-virtuoso & was tested with an ideal 8-bit LFSR tapping its alternate bits. The DAC runs at 20-GS/s & drives a 2pF output load. The input for testing this DAC was provided by a ideal LFSR with 20ps rise/fall time. This DAC (DUT) is the same DAC used in section 2 (Fig. 1(a) & 1(b)) simulated under same conditions, with some modifications in the inductor value to get better results (Fig. 11). So, it can be seen that by improper testing the

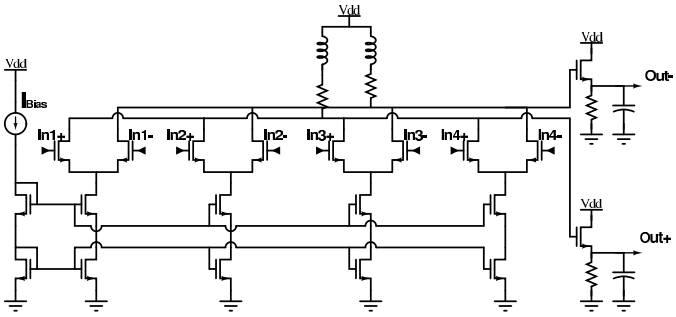


Fig. 10. A 4-bit current-steering DAC circuit run by an 8-bit LFSR used to verify the working of 'Alternate-Bit-Tapping' technique.

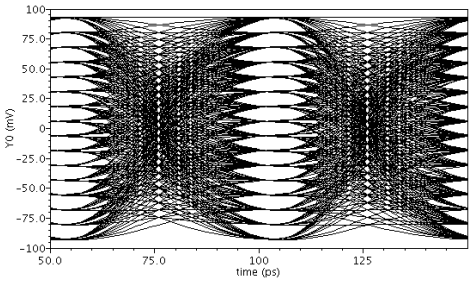


Fig. 11. Eye-Diagram of the output of a 4-bit DAC operating at 20-GS/s driving a 2pF load when driven by tapping alternate bits of an 8-bit LFSR.

DAC would have been misinterpreted to be working fine (Fig. 1(a)), but after performing an exhaustive test the eye opening was found to be less (Fig. 1(b)). By using the "Alternate-Bit-Tapping" technique for proper characterization, it was possible to increase the minimum eye opening from 6.07mV (Fig. 1(b)) to 11.47mV (Fig. 11) for almost same output swing. So, new proposed technique was helpful in improving the dynamic performance of our high-speed DAC.

IV. Conclusion

Testing high-speed DACs is challenging, and if all transitions are not covered in the test, it can lead to incomplete characterization. The new PRBS generation with "Alternate-Bit-Tapping" technique to effectively evaluate the dynamic behavior of a high-speed DAC was proposed. In this technique, to test an m-bit DAC in minimum possible time, a 2m-bit LFSR (with MLS output) is required with its alternate bits tapped and fed as input to DAC to cover almost all transitions between all possible states. Proper characterization using this approach can be helpful in improving the dynamic performance of the device. A 4-bit 20-GS/s DAC was designed and tested in simulations using the "Alternate-Bit-Tapping" approach, and the obtained results were used to improve the eye opening and hence its dynamic behavior. The DAC static characteristics can also be evaluated from the obtained eye-diagram ignoring the need to perform a separate test to calculate its DNL, INL etc. The proposed technique can also find use in testing of analog memories and detection of floating gate faults. Pseudo-random signals generated by a DACs using the proposed approach can also be used to test high-speed communications links with multi-level modulation formats.

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