

Embedded Tutorial: Addressing Critical Power Management Verification Issues in Low Power Designs

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Abstract--Power management techniques that leverage voltage as a handle are being extensively used in power sensitive designs. These techniques include power gating, power gating with retention, multiple supply voltages, dynamic voltage scaling, adaptive voltage scaling, multi-threshold CMOS, and active body bias. The use of the power management techniques also imply new challenges in validation and testing of designs as new power states are created. We look into verification issues along with the solutions to these issues using a verification strategy that involves power-aware simulation, rule-based structural checking, formal tools, and methodology recommendations. We detail our varied experiences with various design teams in addressing these low power verification issues for applications such as the wireless handset, low power microprocessors, and GPS.

Presentations

Introduction to Power Management Techniques and Associated Verification Issues

Bhanu Kapoor, Mimasic, USA

SoC Power Management Challenges

John Goodenough, ARM, USA

Best Practices in Low Power Design Verification Methodology

Prapanna Tiwari, Synopsys, USA

Future Trends in Power Management Design and Verification

Shireesh Verma, Conexant, USA