3D-Integration of Silicon Devices: A Key Technology for Sophisticated Products

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Abstract—**3D integration is a key solution to the predicted performance increase of future electronic systems. It offers extreme miniaturization and fabrication of More than Moore products. This can be accomplished by the combination of Through-Silicon-Via (TSV) technologies for shortened electrical signal lines and Solid Liquid Interdiffusion (SLID) for highly reliable assembly. Depending on the chosen technology concept, TSVs are filled with either tungsten or copper metal. Thinning of silicon as part of the process flow enables devices as thin as 30 µm, so multilayer stacking will result in ultra-thin systems. All these 3D integration concepts focus on wafer level processing to achieve the highest miniaturization degree and highest processing reliability as well as enabling high volume cost-effective fabrication.**

Keywords; Through-Silicon-Via, Solid Liquid Interdiffusion

I. 3D-INTEGRATION TECHNOLOGY

A Through-Si-Via connection is a conductive connection between both sides of a Si wafer that is electrically isolated from the substrate and from other TSV connections. Isolation is done by the so called TSV liner. This layer also determines the TSV parasitic capacitance. In order to avoid diffusion of metal from the TSV into the Si-substrate, a barrier layer is used between the liner and the TSV metal.

For 3D-integration basic technology modules are needed:

- Through-Si-Via process sequence
- Concept and ability of thin wafer handling
- Wafer thinning and backside processing
- 3D-stacking process or 3D-assembly

The TSV process sequence can be part of the device wafer fabrication process or a pure back-end-of line module. So in principle there can be distinguish between

- "Via-first": fabrication of TSV's before the Si front-end (FEOL, Front-End-Of-Line) device fabrication processing.
- "Via-middle": fabrication of TSV's after the Si front-end (FEOL) device fabrication processing but before the back-end (BEOL, Back-End-Of-Line) interconnect process,
- "Via-last": fabrication of TSV's after or in the middle of the Si back-end (BEOL) interconnect process. In this case there is the possibility to start TSV processing from the top surface of the wafer ("Frontside processing") where the active transistor layouts are placed. Starting from the thinned wafer backside is labeled as "Backside processing".

The "via-last" route is the most important one out of these three.

The device orientation within a stack is mainly defined by the application and leads to a classification of stacking as

- Face-to-Face (F2F) or
- Back-to-Face (B2F)

Depending on the availability of devices as wafers or chips and the sizes to be combined, 3D-bonding is performed as

- Wafer-to-Wafer (W2W) bonding
- Die-to-Wafer (D2W) bonding
- Die-to-Die (D2D) bonding

Of course in terms of process costs wafer level process flows are zu bevorzugen.

Key processing technologies for 3D integration are the various temporary or permanent bonding and debonding operations. The requirements for the materials and processes use may vary significantly, pending on the chosen routes.

II. LINER FORMATION WITH SUB-ATMOSPHERIC CVD (SACVD) DEPOSITION OF SIO2

A. Processing

The electrical isolation properties of silicon dioxides vary in a wide range, depending on the process technology of the deposition or thermal grow of such layers. Metal-filled Through Silicon Vias (TSVs) need sufficient electrical isolation to the surrounding bulk silicon. Principally, many thermal oxidation processes would deliver a sufficient dielectric layer for the electrical isolation of the Si-substrate to the metal within the TSVs. But for "via-last" it is not possible to run processes with temperatures above 400 °C due to the presence of metallisation layers on the device substrates. Therefore, CVD based SiO2 films at moderate temperatures in the range between 200 °C and 400 °C are often used for electrical isolation of the TSVs. A SACVD (Sub-Atmospheric CVD) film is well suited for the requirements of the 3D integration in terms of process temperature and conformality. The latter is of great importance when HAR TSVs shall be isolated.Sub-atmospheric Ozone-TEOS CVD is typically done in a conventional PECVD single wafer chamber, which is mechanically altered in order to handle high chamber pressures safely. The process runs without plasma and uses a mixture of

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TEOS - Tetra-Ethyl-Ortho-Silicate - Si(OC2H5)4 - and Ozone (O3) in a pressure range of 100 -600 Torr.

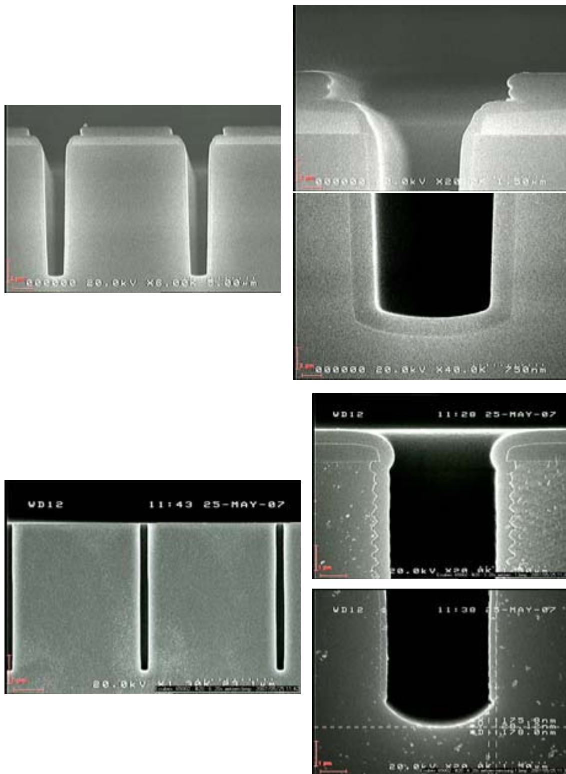

Figure 1. top: Conformality of a 260 nm SACVD O3/TEOS film deposited in a TSV with an AR = 7:1; taper angle of the trench hole ~ 89° (HBr based process)

bottom: Conformality of ~43 % - SACVD O3/TEOS film deposited in a TSV with an AR >16:1; taper angle of the trench hole ~ 89,5 - 90°C (Bosch process)

At Fraunhofer IZM, early work on TEOS/O3 based SiO2 layers for 3D integration has been published in 1995 [1]. Electrical isolation of HAR TSVs (high aspect ratio through silicon vias) with aspect ratios of 10:1 and higher requires a film conformality in the range of 50-60% in order to sufficiently isolate the bottom part of a metal-filled TSV (Figures 1). The maximum achievable conformality of the SiO2 film depends strongly on the taper angle of the trench hole for a given aspect ratio. This assumption is also valid for the subsequently deposited metal-organic CVD layers like TiN, W or even Cu. Depending on the type of etch process which is used to build the HAR trench holes, the achievable taper angle of the TSV varies in the range from ~85° up to 90°or slightly higher.

Besides the achievable taper angle of the etched TSVs, the aspect ratio of the formed trench holes defines the achievable O3/TEOS conformality in a wide range. HAR TSVs with aspect ratios of 15:1 or above are usually etched with the so-called "Bosch etch process", which in term leaves more or less rough sidewalls with a "scallop" like form. Using a SACVD process, sidewall roughness can be tremendously reduced, if the deposited SiO2 film thickness is equal or thicker than the size of the trench sidewall scallops. Smoothening of the scallops can only be expected with the O3/TEOS SACVD process due to its unique growing properties during deposition, as long as the scallop size stays below the absolute film thickness deposited.

Other influencing factors on the quality of the deposited SACVD SiO_2 films are the condition of the trench surfaces prior to deposition. For example, moisture or even insufficient polymer removal from the preceding trench etch process might hinder a conformal and uniform film deposition.

B. Dielectric film properties

SiO2-based dielectric film properties depend mainly on the reactive species used for deposition, on the deposition temperature, pressure regime and plasma enhancement. Regarding the reactive species, thermally grown oxide delivers by far the highest film quality, since there is only O2 and/or H2 involved during film growth. Within-wafer uniformity, surface roughness, wet etching rate in HF and electrical break down voltage are unsurpassed compared to CVD-films. One disadvantage of thermally grown oxide, however, is the comparably high extrinsic film stress of 400 MPa and more. Silane-based CVD films contain hydrogen; the amount depends mainly on the deposition temperature and the N2O/SiH4 ratio). Also TEOS-based films are known to contain O-H groups [2] and tend to absorb H2O over time. Due to the required film conformality for 3D purposes, ozone-based SACVD films deliver acceptable results regarding within-wafer uniformity, surface roughness and extrinsic film stress.

O3/TEOS SACVD films can be deposited with a measured electrical breakdown voltage of 361 V/µm for SACVD O3/TEOS films (~ 7 times lower compared to thermally grown oxide films). With a typical film thickness of ~ 150 nm SiO2 the breakdown voltage of an O3/TEOS SACVD film in a HAR TSV can be estimated to be > 50 V. Electrical measurements of W-filled TSVs with a 260 nm thick SACVD-based SiO2 have shown electrical leakage current values in the fA range (9).

Ozone/TEOS based films are quite sensitive to the surfaces on which the film has to be deposited. Therefore, appropriate wet/dry cleaning of the wafer surfaces after DT etching is mandatory for repeatable deposition results, especially concerning the film conformality in HAR trenches. Quantifying the possible influence of pre cleaning on the achievable conformality is difficult, because the surfaces of the trench holes, the trench depth, trench size, AR and taper angle all influence the deposition result.

III. TSV METALLIZATION BY CHEMICAL VAPOR DEPOSITION (CVD)

In order to build vertical electrical interconnects between thinned chip stacks or wafer stacks, TSVs with high aspect ratios are used in several currently presented 3D process flows [3-6]. For this purpose, the required metallization needs to be deposited after the electrical isolation of Through Silicon Vias (TSV) in such a way, that reliable electrical interconnects are formed. Mostly the TSV metallization consists of a bi- or multilayer stack of a thin diffusion barrier, adhesion layer

and/or seed layer and the conductor material like tungsten (W) or copper (Cu). In general different deposition techniques are available to realize metal deposition: electrochemical deposition (ECD, electroplating), chemical vapor deposition (CVD), electroless plating and physical vapor deposition (PVD: Sputtering). Apart from PVD all processes have the potential to fill high aspect ratio (HAR) patterns. Figure 2 shows the applicability of different deposition processes and filling concepts depending on the TSV diameter. The pure metal CVD approach is suited for complete TSV fill with lateral width of up to ~3 µm at high aspect ratios. It is currently not clear to which extend the electroplating technology is able to substitute MOCVD (metal-organic chemical vapor deposition) processes for HAR TSV metallization [7, 8]. However, if aspect ratios of larger than 7:1 are to be filled with a conducting material, CVD is the process with the highest currently available conformality. Up to now, CVD of poly-Si, tungsten or copper have been used to completely fill TSVs. In the region above 3 µm lateral size, several factors limit the application of metal CVD, like high film stress for W CVD and process limitations for Cu CVD. In this case, filling can be performed by electroplating. CVD can be used to deposit a so-called seed layer only, which then acts as a base layer to grow metals by following electroplating techniques. This is especially of great interest since even most advanced PVD tools are hardly able to cover vias with aspect ratios larger than 7:1 [9, 10]. Depending on the chosen metallization scheme, a thin conducting CVD layer such as W or Barrier/Cu can be used as a seed layer for the subsequent electroplating process.

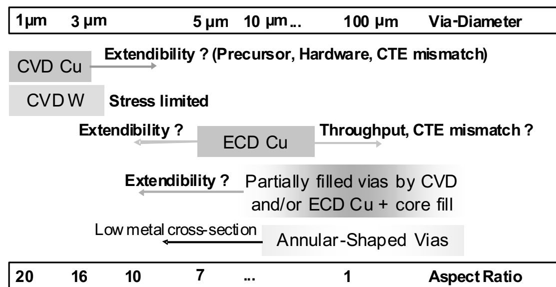

Figure 2. Overview of deposition processes and concepts for metallization of TSVs

TSV dimensions vary in a wide range from ~ 2 µm up to 100 µm and beyond. An increasing demand for TSVs with HAR will probably require an increasing amount of metal CVD applications now and in the future, because the use of metal-PVD for a seed layer is strongly limited by the desired AR. For completely filled Cu TSVs with large diameters the mismatch in the coefficient of thermal expansion (CTE) of copper and silicon should be considered. This leads to vertical movement of Cu plug in the TSV during repeated thermal cycling in further BEOL processes [11]. With the hybrid method, where the TSVs are only covered by Cu at the sidewalls and are backfilled by a composite material, the damage of dielectric layers due to thermal mismatch is prevented [11]. At the same time this has the potential to provide a low cost process which avoids the complexity of the void free complete fill by ECD. The annular shaped TSV in contrast to cylindrical TSV is a further approach to reduce the impact of the thermal mismatch due to the reduction of metal volume in the TSV and to produce low resistance vias at the same time [11].

In this chapter we focus on the CVD of W and metal nitrides (TiN). Metal-CVD or metal-organic.CVD (MOCVD) is typically done in a conventional CVD single wafer chamber (cold wall reactor). The deposition process is a strictly chemically based, temperature driven reaction of the decomposed precursor material on the wafer surface. Since moisture causes metal oxides, a load lock based system is required to accomplish repeatable and stable process conditions.

The availability and the choice of a precursor is one of the most delicate issues of the metal deposition by CVD. The precursor choice decides on the quality of the deposited films (impurities, adhesion), deposition parameters (temperature, pressure, reactants) and therefore influences the reliability of the 3D integrated TSVs. Most commonly used metals for 3D integration are currently tungsten and copper for TSV filling and often TiN and also TaN as barrier/seed layer films.

A. Barrier deposition

For tungsten CVD, a TiN layer is used to provide an adequate nucleation and adhesion layer. For Cu filling it acts as barrier against Cu diffusion.

TiN depositions can be done in commercially available CVD reactors with plasma capability. The precursor, TDMAT, is delivered by a bubbler system. The as-deposited film by pyrolysis of TDMAT contains substantial amounts of impurities (C,H) and is not stable at air. Therefore, a plasma densification treatment is needed after the deposition step. For CVD-W this step is also essential to promote the required adhesion for the highly stressed W films. The TiN barrier layers are produced by a multi-step process consisting of alternating pyrolysis steps and plasma treatment steps. The TiN layer is plasma-densified after depositing ~5 nm TiN, resulting in a final thickness of ~ 2.5 to 3 nm after plasma treatment, depending on treatment time. The number of cycles is determining the thickness of the entire barrier, e.g. 8 cycles for ~20 nm thickness.

The step coverage in high aspect ratio TSVs depends on their geometry and diameter size as well as their depth. Vias with a width of 20 µm diameter and greater are uncritical with respect to the step coverage. On the contrary, in slot holes with a length of 20 µm, a width of 1 µm to 5 µm, and 30 µm depth TiN films show a step coverage of 30 % to 70 % at the bottom of the via, depending on the width of the slot hole. In vias with circular cross-section the same dependence was found. Higher step coverage is observed on sidewalls particularly in the upper via range (more than 100 %). Since the plasma treatment is quite directional, the densification is not very effective at surfaces parallel to the incident direction of the ions.

B. W-CVD Metallization

The complete process sequence is done as follows. After the isolation of the TSVs is completed, a full in situ process

sequence under vacuum, consisting of an Ar pre-sputtering step in the W etch back chamber (RIE), multiple deposition/etch steps to achieve a 20 to 30 nm thick, plasma densified TiN seed layer in the TiN-MOCVD chamber, followed by ~ 1100 nm W CVD (400 °C), cool down under vacuum and partial etching of the W in the W etch back chamber is performed.

Since relatively thick W-layers are required to fill the TSV-holes, a partial blanket W etch back to a remaining film thickness < 500 nm is carried out, thus avoiding any peeling or delamination of the W-layer. A conventional RIE plasma chamber with an SF6-based etch chemistry can be used for the partial blanket W-etch step as well as for the following structured W-etch step described below. The partial etch back also helps decreasing the wafer bow to a moderate level, so wafers can be handled normally into a lithography tool, i.e. a wafer stepper. By use of a photo resist mask, a PR-structured W etch is done afterwards in order to remove the remaining W after in-situ partial W etch back. The remaining W film is structured in such a way that the area of the original TSV plus some overlap is fully covered with photo resist (light field mask). Therefore, excessive etch attack on the W inside the TSV is avoided during W-etch. The first stop layer is the thin TiN-layer, preventing the underlying oxide to be etched excessively during the W over etching step. Finally, the remaining TiN layer is etched with a chlorine-chemistry, so the TSVs are electrically isolated from each other and can be further integrated.

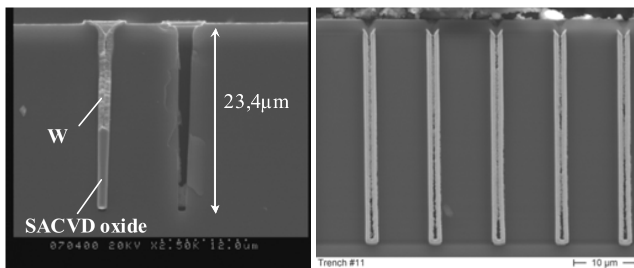

Figure 3. Figure 3: left: SEM-image (left) and top-view micrograph image (right) of a W-filled TSV, AR > 10:1, taper angle 88° (HBr-chemistry) after a structured W-etch step

right: SEM-image of a W-filled TSV, AR > 15:1, taper angle 89,5° (SF6/C4F8-chemistry), after blanket W etch back

Figure 3 shows a typical W-filled TSV (20 µm depth) after the completed W-structuring sequence as a cross-section. The achievable conformality of the W-CVD step depends mainly on the taper angle and the aspect ratio of the TSV and is > 80% for a TSV with a 10:1 AR at 3 µm lateral size (trench width). The left W-filled TSV shows part of the formerly done dielectric isolation layer (Ozone-TEOS based SACVD film) and also the W-film inside of it at the upper part of the TSV (Due to its stiffness and hardness the W-film in the right tungsten filled plug was completely removed while cleaving the sample).

A void free W-fill result is difficult to achieve for HAR TSVs; the taper angle of the formerly fabricated TSV is the main parameter for the size of the void. Figure 9 shows a SEM image of a W-filled TSV with an aspect ratio > 15:1 and a taper angle of 89.5°, resulting in a noticeable void.

Besides the above mentioned possibility of an W etch back process, CMP of W could also be applied to polish the remaining bulk tungsten until the underlying dielectric layer is reached, thus resulting in electrically isolated TSV with negligible topography.

IV. BACKSIDE PROCESSING OF THINNED SILICON

Most 3D process flows require Si-thinning from the wafer backside until the TSVs are opened. Once this point of the thinning sequence is reached, either by Si-CMP (chemical-mechanical polishing) or by Si dry etching, the TSVs have to be electrically contacted from the back by an additional metal layer, in most cases an additional Cu or AlSiCu structure. In order to keep the electrical isolation still intact, the former trench bottom of the TSV – seen from the front side – which in turn becomes the freshly opened "tip" of the metal-filled TSV, must have enough SiO2 isolation to withstand the etch attack of the Si-etch back step, see figure 4.

This SiO2 thickness depends mainly on two parameters: The prior deposited absolute SiO2 film thickness and its achieved film conformality. If a maskless technique is used to continue the 3D integration after "touching" the tips of the TSVs, the SiO2 film thickness at the TSV tip should be in the range of >200 nm. Modern Si-dry etching processes can achieve selectivities up to 50:1 between Si and SiO2. If, for example, a Si recess of ~ 2 µm is targeted, the estimated total SiO2 removal will be ~ 40 nm, thus leaving ~ 160 nm SiO2. In case of a backside photoresist mask, which is used to structure a previously deposited backside SiO2 film, even thicker SiO2 films are advisable due to known alignment accuracies of stepper lithography or mask aligners.

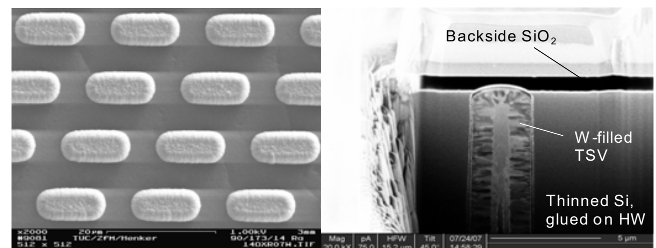

Figure 4. left: Backside view (SEM) of a Cu-filled TSVs, just opened from the back after Si-etching. O3/TEOS film still covering the Cu-metallization. TSV depth 40 µm; nominal size 3x10 µm at front side.

right: FIB image of a 50 µm thin Si substrate glued on a handling wafer, with W-filled TSV; SiO2 CVD-film (Silane-based) deposited at 150 °C on backside of handling wafer stack

Once the Si-thinning has been completed, a backside dielectric film is required to fully isolate the thinned Si-substrate from the metal-filled TSVs. For this purpose, Silane-based PECVD oxides at low deposition temperature are preferable. In most cases the thinned silicon substrate has to be temporarily glued onto a handling substrate, otherwise the Si-substrate couldn't be handled safely anymore. Therefore, the glue material, often a thermoplastic or wax, which can be chemically removed later, requires a maximum processing

temperature in the range of 180°C or lower, otherwise delamination between handling wafer and thinned substrate will occur. Since PECVD of TEOS - or other precursors like HMDS – tends to show early condensation of the TEOS vapour at low deposition temperatures, some reactor types would not allow running a deposition process below 250 °C. Therefore, Silane-based PECVD processes at temperatures down to 150 °C can be used instead. The achievable SiO2 film quality is of course lower than that of standard processes. However, film thickness can well be increased above 1 µm, thus compensating for the lower electrical breakdown voltage of a low temperature film. Figure 4 shows a FIB-image of thinned Si with a 50µm deep W-filled TSV, covered with 1 µm backside SiO2 (Silane-based PECVD, 150 °C deposition temperature).

V. Bonding with Intermetallic Compounds

To achieve compact and rigid stacks made from different layers of active devices or passive element in silicon, an easy technology without a complex mix of different materials like polymers, metal and probably fillers in polymer would be desirable.

To stack silicon layers in an economic way, the process steps necessary to achieve this should be modular. One possible influence while stacking could be the active shifting of underlying layers by re-melting the metal connections when placing the next layer on top. This shift can result in short cuts of electrical contacts at low pitch designs. Therefore these metal bonds should not re-melt after stacking. This can be realized by the use of high melting inter-metallic phases that are formed in place. The process utilizes the diffusion of solid metal into the liquid phase of a lower melting metal and is reported by Bernstein et al. for the applications for bonding processes in integrated-circuit fabrication already in 1966 [12, 13]. His created acronym SLID (solid liquid inter diffusion) stands for this type of metallic bonding.

The SLID process was applied for mechanical and electrical interconnects in combination with a through-silicon-via technology at the Fraunhofer IZM and introduced as ICV-(Inter-Chip-Via) technology as a fully modular concept for vertical system integration optimized for chip-to-wafer stacking [14, 15].

A. Technological Concept

Due to the different thermal expansion coefficients of the devices and the metallic bond system, thermally induced stress is created depending on the formation temperature. To lower the influence of this possible cause for reduced reliability, the melting point of the lower melting metal should be as low as possible. On the other hand, reliability of the metallic bond is increased by high re-melting temperatures, for mechanical creeping is related to this re-melting point during temperature cycling. As a consequence the ideal metallic bonding system consists of a very low melting metal that vanishes completely by dissolving the high melting partner, resulting in a high melting alloy, the inter-metallic phase.

B. Basic material selection

There are some metals that fulfill the characteristic “low melting”. Usually low melting is oriented on the stability of aluminum within a device, meaning a maximum temperature of 400 °C. Lead (Pb; 327 °C), bismut (Bi; 271 °C), tin (Sn; 231 °C) and indium (In; 156 °C) are the candidates, while lead is no longer accepted due to its toxicity when incorporated as metal or compound. Often used refractory metals in the backend of device technology are nickel and gold (wire bond pads) and copper as multi layer metallization in the device itself. Silver as pure metal sometimes is used as thin capping layer to prevent copper from oxidation. These metals can be combined as SLID systems to form inter metallic compounds with resulting high melting points. The temperature of these inter metallic compounds exceed the melting point of the lower melting metal (Cu_3Sn, 676 °C; $AgIn_2$ or Ag_2In, 765-780 °C)

C. Principal processing scheme

To avoid polymeric underfillers, electrical contacts and mechanical joints can be formed at the same process steps. Temperature increase above the melting point of the lower melting metal and contacting opposite sides leads to symmetric interdiffusion and intermetallic compound formation.

The higher melting part of the metal layers is consumed by interdiffusion into the liquid (figure 5). The ratio of this metal and the low melting metal should be chosen high enough to have a remaining amount above the adhesion layers. Consuming all of the higher melting metal could result in adherence problems on the adhesion layer.

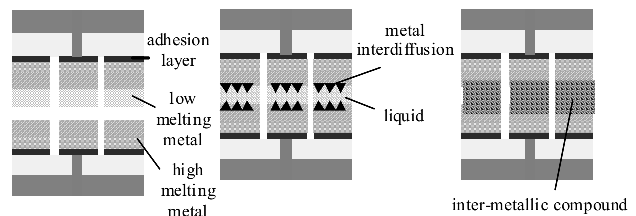

Figure 5. Schematics of a binary metal system. Electrical contacts with TSV and mechanical joints are formed at the same process steps. Temperature increase above melting point of lower melting metal and contacting opposite sides leads to symmetric interdiffusion and intermetallic compound formation (source Fraunhofer IZMM)

The formation of intermetallic compounds roughly is devided into two periods of time and reaction speeds. In the first period liquid metal has contact to the refractory metal. Dissolution in the liquid and diffusion is very fast. At seed points on the surface of the refractory metal the intermetallic compound with the highest formation energy is deposited. The consumed metal is further supplied by dissolution in the liquid. The deposited areas are growing until the liquid phase is cut off from the refractory metal surface. From this point of time the second period of the bonding process is starting. The reaction speed is dominated by diffusion of refractory metal through the intermetal compound of period one. This of course is more

time consuming and it takes longer until the lower melting metal is completely consumed. The liquid phase solidifies when the concentration of refractory metal shifts the melting point above the actual processing temperature. On further heating this solidified phase transforms to the energetically next favored intermetallic compound. An example is shown in figure 6. Here we have a cross section of a three level silicon stack with two bond layers from Cu/Sn/Cu. The first layer had seen the process cycle of its own and the cycle of the second layer, while the second layer was heated only once. Therefore in the first layer only the final state of intermetallic compound formation is visible. In the case of Cu/Sn this means Cu3Sn in contact with copper interfaces. In the second layer this transformation is not completed. Here the Cu6Sn5 compound is sandwiched between Cu3Sn and only further heating will complete the formation.

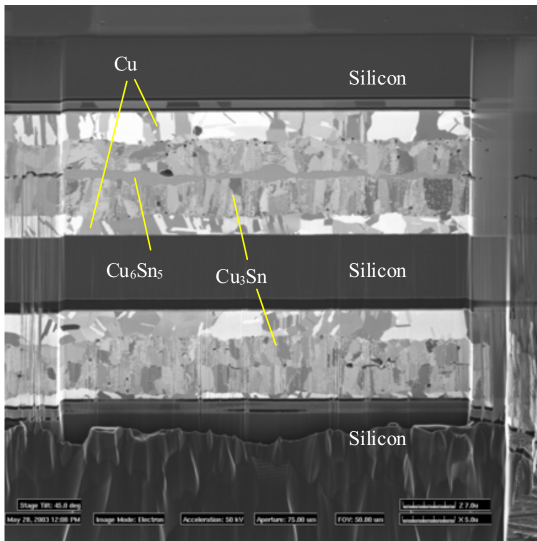

Figure 6. FIB-cross-section of a three level silicon stack with two bond layers from Cu/Sn/Cu. The first layer (lower part) was temperature cycled twice, while the second layer (upper part) was heated only once. The first layer shows only the final state of intermetallic Cu3Sn in contact with copper interfaces. The second layer has not completed its transformation; Cu6Sn5 compound is still sandwiched between Cu3Sn (source Fraunhofer IZMM)

Process temperature influences the appearance of the intermetallic compounds. In the presented example the temperature was 70 °C above the melting point of tin, that means 300 °C peak value of a ramped process cycle. Cu3Sn in this case is crystalline and shows grain growth perpendicular to the refractory metal copper.

The molecular volume of the intermetallic compounds is smaller than the sum of the volume of the metals before compound formation. This results in shrinkage of the total bond layer thickness. Applying pressure is recommended to make sure the interfaces do not separate during the bonding process. But this is only valid, if the shrinkage amount is equal all over the surface (that can mean the total wafer area). As soon as there are problems with topography variations, pressure doesn't help. Pressure mainly supports to overcome the bow of two substrates when bonding large areas. As a consequence of the volume shrinkage of the compound, voids and crevices are formed

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