A Compact Digital Amplitude Modulator in 90nm CMOS

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***Abstract*—This paper presents a 90 nm CMOS digital amplitude modulator for polar transmitter. It reaches an output power of -2.5 dBmRMS using a WLAN OFDM 64QAM modulation at 2.45GHz achieving -26.1 dB EVM and 18% efficiency. To reduce the aliases due to the discrete-time to continuous-time conversion a 2-fold interpolation has been implemented. The amplitude modulator has a segmented architecture. This results in a very compact 0.007 mm^2 chip area.**

I. INTRODUCTION

Modern communication schemes achieve a high spectral efficiency by modulating both amplitude and phase, but traditionally require highly linear power amplifiers due to the high peak-to-average-power-ratio (PAPR) of these schemes. Traditional linear amplifiers are therefore used well below their saturating output power, at the cost of reduced power efficiency and battery life.

More power efficient transmission is expected to come from polar transmitter architectures using highly efficient non-linear PAs. These are phase modulated at their saturation level, and therefore achieve a high efficiency. The amplitude information is then added through a separate path. The latter has to be achieved in an efficient way, in order not to degrade the overall efficiency.

In a polar transmitter the Cartesian coordinates *I(t)-Q(t)* are converted into envelope and phase component, *A(t)-φ(t)* according to:

$$(1) \quad A(t)=\sqrt{I^2(t)+Q^2(t)} \qquad \varphi(t)=tg^{-1}\left[Q(t)/I(t)\right].$$

Due to this non-linear conversion, the bandwidths of both the amplitude and phase components are increased [1]. Hence a wideband amplitude modulator is needed.

This paper presents an inherently broadband digital amplitude modulator that combines DAC, mixer and PPA into one structure [2]. It consists of multiple parallel basic unit amplifiers, which are turned on and off when needed. Their output powers are then combined in the load. This approach results in a high power efficiency. To reduce the aliases inherent to the DAC operation, 2-fold interpolation is included in the PA.

The amplifier features a segmented implementation for the digital decoding, with a matched but dense layout, which results in an extremely area efficient implementation, saving up to 75% of area compared with pure thermometric addressing.

The organization of the paper is as follows. In Section II the circuit topology is described. Moreover mismatch effects, and 2-fold interpolation are analyzed. In Section III methods resulting in very dense 90nm CMOS chip area are explained. Section IV presents the characterization results like AM/AM, AM/PM, DNL, and INL. Finally measurements in term of EVM, spectrum and efficiency are presented, in the case of transmitting WLAN 54Mb/s 64QAM at 2.45GHz.

II. CIRCUIT DESCRIPTION

The basic amplifier structure is a cascoded common source amplifier. Multiple basic amplifiers are then combined into a steering DAC, as depicted in Figure 1. The bottom transistor acts like the current source and it is driven by the RF phase-modulated signal. The cascode transistor is digitally controlled acting like a switch that turns the unit amplifier on and off, according to its digital input. The unit cells are digitally controlled by the amplitude code, and their output currents are combined to shape the RF output. As the current in each branch is switched off when the signal current is blocked from reaching the output, good efficiency is obtained. The open-loop structure and the absence of high impedance switched nodes, guarantee to this architecture a wide bandwidth. These features (simple unit cell, good efficiency, and broadband structure) make it an attractive solution to be employed in a polar architecture.

A Simulink model was implemented to determine the required specification of the amplitude modulator. A 64QAM symbol is processed through a model of a polar system, and the resulting EVM and ACPR are analyzed. The model of the amplitude

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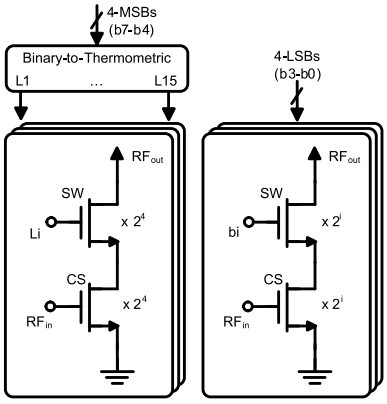

Figure 1. Digital Amplitude Modulator Architecture.

modulator includes number of bits and sampling rate. Realistic AM/AM and AM/PM distortion, based on Spectre simulations, was added to the model. This distortion is then, as it is in the real application, compensated by a LUT-based predistortion.

From the model, 6 bit resolution are needed to meet 64QAM linearity requirements [2]. In practice, the effective number of bits will be reduced by various non-idealities. For this reason, a number of 8 bits has been chosen.

The simplest way to address the 8 bits is by pure binary encoding. However, this does not guarantee monotonicity, and results in potential poor DNL, especially at the MSB code steps. This can be solved by using thermometric coding. This results however in a complex decoding scheme, and a large area overhead [3]. A solution is to combine partial binary and thermometric coding to combine the advantages of both, while limiting the disadvantages [3].

The size of the basic CS transistor is a compromise between loading of the previous stage and mismatch. For loading, the size has to be minimal. To assess the effect of transistor mismatch, a statistical model was added to the simulink model to investigate the results of transistor mismatch for a binary, a thermometer and a segmented controlled array. Modeling each current source as a Gaussian random variable with mean I and variance σ^2, the relative variance of a unit current source (realized with a MOS transistor in saturation region) depends on its dimensions W and L according to the Pelgrom model [4].

In this statistical analysis the other source of non-idealities (e.g. AM/AM and AM/PM) where not considered in order to highlight the only mismatch effects on the ideal DAC transfer function.

From this analysis a 50% segmentation degree (4-MSB's thermometric, 4-LSB's binary) is chosen as an optimal. For a given transistor mismatch, the expected EVM degrades only by a few dB, while the decoding can be performed in an area efficient way as will be explained. The basic cell is sized minimally to obtain monotonicity according to the Monte Carlo simulations. The major drawback of combining the envelope DAC function with the upconversion, as in this topology, is that the DAC aliases are present at RF and cannot be filtered in baseband, as in more traditional transmitters.

As a result, aliases of the transmitted signal are present at multiples of the clock frequency around the RF signal, violating the constraints on out-of-band emission.
These aliases are directly dependent on the clock frequency and the single side modulating signal bandwidth. In order to respect IEEE 802.11a/g spectral mask, aliases should be 40db below the wanted RF signal. This is theoretically possible at very high DAC oversampling rates according to:

$$Alias_{dBc} = 20Log\left[\sin c(f_{clk} - f_{sig} / f_{clk})\right] \quad (2)$$

where f_{clk} is the sampling frequency and f_{sig} is the monolateral signal bandwidth. In practice, the required oversampling is too high, especially when targetting high bandwidth standards.

The aliases can be effectively reduced by applying a linear interpolation between 2 consecutive samples. This adds a supplemental sinc filter to the DAC output spectrum [5]. In practice, this linear interpolation can be approached in discrete steps, resulting in an intermediate filtering (Figure 2). The presented amplitude modulator implements 2-fold interpolation, which can very easily be integrated by clocking 2 parallel arrays on the opposite clock edges (Figure 4).

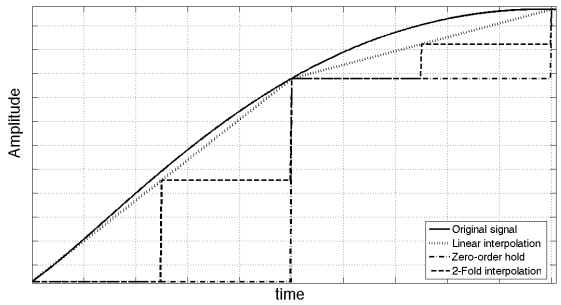

Figure 2. Zero-order hold, 2-fold interpolation, linear interpolation.

III. PHYSICAL IMPLEMENTATION

The 8bits amplitude modulator is segmented into 4 binary coded LSBs and 4 thermometric coded MSBs. The thermometric unit cell consists of 16 LSBs unit cells. To reduce mismatch errors due to process gradients, the cells are carefully centered around the central diagonal resulting in a matrix of 16X16 LSBs. Dummy cells were added to each side of the matrix to avoid boundary effects.

The binary controlled unit cells corresponding with the smallest digital values are all placed on the central diagonal of the array. They are distributed such that their center of gravity is in the middle. The thermometric coded cells consist of 16 LSB cells. These are spread on the adjacent diagonals. Note that as these diagonals don't have a size of 16 units, the thermometer cells are all spread over 2 diagonals. The thermometer cells are again spread around the centre diagonal to minimize systematic mismatch. Eeach unit is spread over 2

diagonals. These are spread around the centre diagonal to minimize systematic mismatch (Figure 4).
The unit cells are flipped both vertically and horizontally to share the RF and the supply lines. The digital control lines are routed along the diagonals. As no internal decoding logic is needed, as in thermometer-coded implementations [2,6-7], the resulting structure is very compact. The RF input and output are routed on alternating horizontal lines, avoiding the crossing of the RF signals in the structure. All crossing of digital control lines with RF signals was shielded to avoid cross-talk.

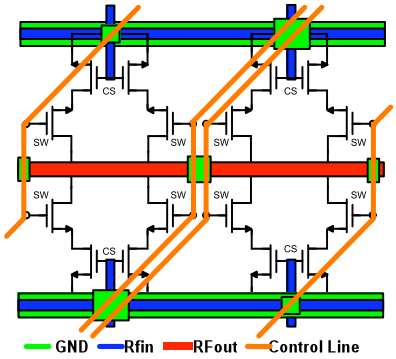

Figure 3. 4X2 unit cells routing.

The final block diagram of the polar amplitude is shown in figure 4. It consists of 2 identical arrays flipped around the centre. The digital control is applied through latches for synchronization of the toggling. The latches controlling both arrays are controlled on an opposite clock phase to obtain the 2-fold interpolation. The area of the digital circuitry is limited and the additional power is insignificant compared to the total. An extra latch is added in the folding digital path to time the digital code correctly.
The chip has been realized in 90nm CMOS technology. The unit cell consists of a 700nm/200nm (W/L) common source NMOS (CS) and a 700nm/100nm switch NMOS (SW). The microphotograph of the chip is shown in figure 5. The effective area of the polar amplitude modulator is 110x65um^2.

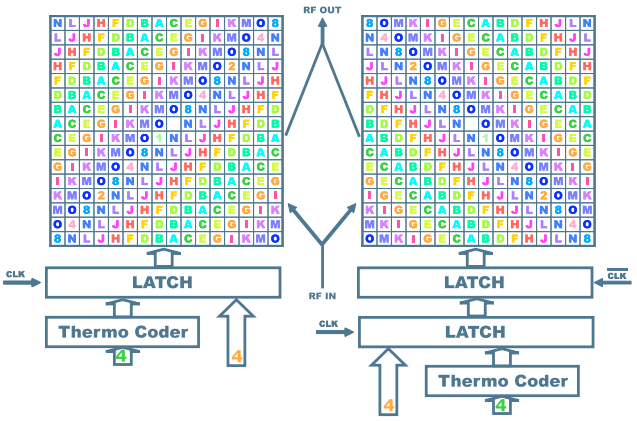

Figure 4. Block Diagram of the Digital Amplitude Modulator.

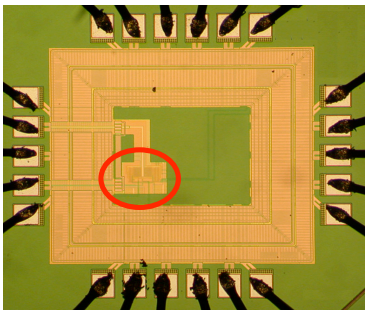

Figure 5. Chip microphotograph: active circuit (110um x65um).

IV. Experimental Results

For the measurements, the prototype was bonded directly on a printed circuit board (PCB). An external inductor is used as a load for the amplifier. All measurements have been performed on a single-ended 50Ω terminated output. The analog and digital voltage supply is 1.2V. Both 'static' and dynamic measurements were performed. For the 'static' measurements, an un-modulated RF signal is applied to the RF input, and the output power is measured for a constant digital code. The dynamic measurements include phase and amplitude modulation.
For the static performance, figure 6 shows the AM/AM and AM/PM measured. At full scale, the saturated output power is 5dBm at 23% drain efficiency. The non-linear AM/AM curve is mainly due to the varying output impedance of the amplifier with the digital code. The AM/PM curve is relatively flat at the highest codes, but changes rapidly at the lowest codes. This is probably due to a relative higher contribution of LO feedtrough. Both curves can be effectively compensated by digital predistortion: the AM/AM curve directly in the digital code to the amplitude modulator, the AM/PM curve has to be compensated with the phase modulation. In our dynamic measurements, only the amplitude compensation is applied. The measured DNL is between ±1 LSB, which demonstrates the monotonic behavior of the segmented coded amplitude modulator.
For the dynamic measurement a WLAN 64 QAM OFDM signal with a bandwidth of 20 MHz is used. The measurement setup for the dynamic polar modulated amplifier is given in

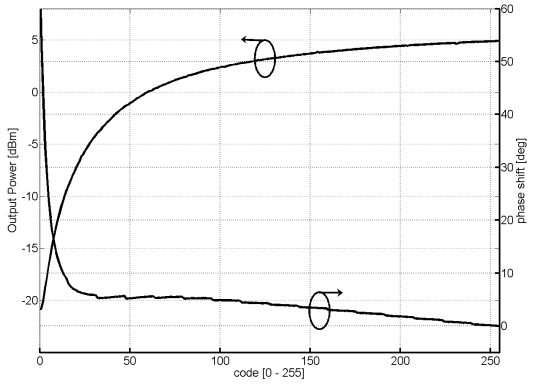

Figure 6. AM/AM and AM/PM.

figure 7. The phase modulated RF signal is generated by a high speed (10Gs/s) Arbitrary Wave Generator (AWG). The data for this AWG is generated with Matlab. The AWG also generates the 40 MHz clock for the digital pattern generator, ensuring that the latter is completely synchronous with the RF phase signal. The pattern generator provides the digital data to the amplitude modulator. It also feeds back a pulse to the AWG to synchronize the start of the symbol. By tuning the position of this pulse with respect to the amplitude digital data and by tuning the initial phase of the RF signal, both amplitude and phase can be aligned at the amplifier, despite the completely different paths.

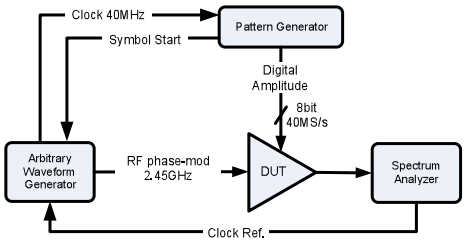

Figure 7. Measurement Setup.

For the measurements, a WLAN 64 QAM OFDM signal with 20MHz bandwidth is generated in Matlab. The amplitude and phase component are then extracted. The phase is used to create a phase modulated RF carrier at 2.45GHz. The amplitude data is first predistorded according to a look-up-table that was generated during the static measurements, based on the AM/AM curve. This table was measured once and was then used for all dynamic measurements performed. The predistorded amplitude information is sampled at 40 MHz to be fed by the pattern generator. This 40MHz is a limitation of the pattern generator and limits the achievable EVM and degrades the output Spectrum. Indeed, from simulations, up to 200MHz operation is feasible with the modulator. Measurements with this configuration (2.45GHz carrier and 40 MHz Amplitude sampling) result in an EVM better than -26dB, for a transmitted 64 QAM WLAN OFDM signal with 20 MHz bandwidth (Figure 9).

As discussed, this EVM is limited by the 40 MHz of the generator. This is also the case for the spectral mask, where the oversampling of the amplitude data with respect to the channel bandwidth is insufficient (Figure 8). Note that the aliases at the sampling frequency (40MHz) are effectively reduced by the 2-fold interpolation.

Measurements with smaller baseband bandwidth signals demonstrate that the modulator is indeed limited by the pattern

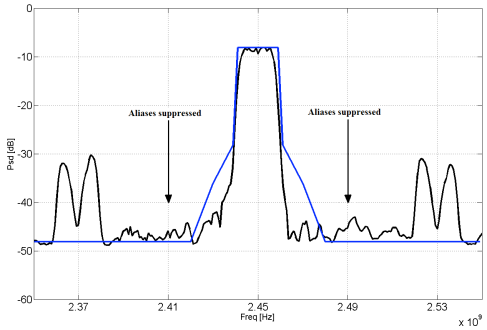

Figure 8. OFDM Output Spectrum.

generator's sampling rate (e.g. -27.2 dB EVM with 10MHz bandwidth).

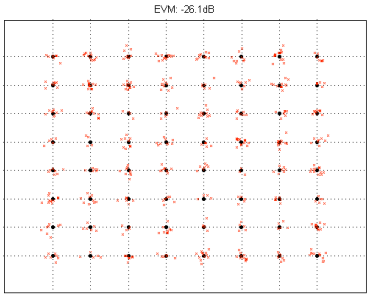

Figure 9. Error Vector Magnitude.

Table I. Summary and Performances Comparison

Ref.	Supply Voltage [V]	Chip Area [mm^2]	Pout [dBm]	η_D [%]	EVM [dB]
[2], 180µm	1.7	-	13.6	12	-26.8
[6], 90nm	1.2	0.17	9	8.1	-26.2
[7], 90nm	1.2	0.023	-5	2.5	-26
This work	1.2	0.007	-2.5	18	-26.1

V. CONCLUSIONS.

In this paper a digital amplitude modulator with 2-fold interpolation for alias reduction for OFDM WLAN has been presented. It is based on a segmented-coded matrix with a very simple basic cell, only two transistors, without any local decoding logic. This results in an extremely compact implementation (Table I). It reaches a power of -2.5 dBm RMS for a 20MHz 64QAM WLAN OFDM signal. The corresponding drain efficiency is of 18%.

Thanks to segmented digital decoding and to an accurate dense layout, silicon area results in only 0.007mm^2 in 90nm CMOS.

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