

An High Voltage CMOS Voltage Regulator for automotive alternators with programmable functionalities and full reverse polarity capability

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Abstract—This paper presents an innovative and effective approach to design and test a regulator for an automotive alternator with programmable functionalities. The prototype system consists of two different parts: an integrated circuit (IC) and a FPGA. The IC, implemented in austriamicrosystems HVCMOS 0.35 μm technology, includes all the high voltage parts and a power switch with very low ON resistance. It is able to manage full reverse polarity on every pin, including the reverse battery condition, and over voltages up to 50 V. The programmability is guaranteed through the FPGA. This prototype system can be used to develop a new type of intelligent smart and flexible regulators which implement many additional programmable functions that give the car maker a better control and allow to reduce vehicle fuel consumption and CO₂ emissions. In the demonstrator all the implemented functions, including regulation, can be changed during the development phase and many properties, including loop stability, can be checked before releasing a final version of the regulator. The proposed system is also included in a standard brush-holder that can be mounted on Valeo Engine and Electrical System mechatronic alternator and verified directly in a real application.

Regulator for automotive alternators; programmable regulator; reverse polarity; HV CMOS voltage regulator

I. INTRODUCTION

The recent evolutions of the vehicles are mainly led by the reduction of fuel consumption and this requires to improve the efficiency of all the subsystems. A major contribution is related to the alternator, which is the electro-mechanical machine that converts part of the mechanical energy into electrical energy [1-2] needed to supply all the electrical loads. The efficiency of that machine can be improved in three ways: - electrical engineering design of the machine - rectifying losses [3-4] - regulator behavior [5]. The regulator is the smart part of the alternator that, on the first hand, controls external (user) functions such as Load Response Control (LRC) and, on the second hand internal functions, such as regulation loop. There are two main kinds of regulators: - *Stand alone regulators* that manage by themselves how the alternator behaves in the car, - *Interfaced regulators* which are more or less slaved to the Engine Control Unit (ECU). Due to car maker fuel consumption reduction programs, the market share of

interfaced regulators has drastically increased over the last 10 years to become now the majority. Thus the demand of customized internal functions has increased too. The regulator functions are fully integrated in the mechatronic module, which includes an application specific integrated circuit (ASIC).

Alternator regulators are then among the most complex automotive System on Chip (SoC) where increasing time-to-market constraints make their development more and more challenging. Effectively, car maker development programs are about 12 to 18 months meanwhile the ASIC-mechatronic developments are about 24 to 36 months. Considering ASIC side only, each change needs schematic and layout redesign followed by masks and dice manufacturing; basically a couple of months for design and 3 months standard processing, sometimes less time if only a couple of metal masks are necessary. After receiving parts, the validation and the product qualification or re-qualification according to automotive standards takes roughly 6 months for production parts delivery.

The challenge for the new generation of alternator regulators is to reduce ASIC development time and to combine the harshest requirements, including full reverse polarity capability, with a low cost CMOS technology that, at the same time, increases the flexibility, allowing software configuration for multiple car platforms and improve energy efficiency during operation.

In order to improve the development lead time, the functions can be developed in two steps. The first step is related to the electronics for interfaces, which realize the signal adaptation and conversion and is standard or easily adapted to the specification. These interface functions are usually analog and the most difficult to design because the system has to fulfill the automotive requirements and, in particular, the Electro-Magnetic Compatibility (EMC) and Electro-Static Discharge (ESD) constraints. Furthermore very harsh requirements in terms of temperature, voltage and current, lead to use high cost technologies for dice manufacturing. The electronics for interface is evaluated and assembled in the mechatronic mock-up to be connected to the electronics for algorithms, which manage the regulation functions. This mock-up is then functional, can be mounted on a standard alternator and finally

on vehicle. This last action, one of the most important, is to directly check the specification, the adjustment with power train system and the interaction with the ECU in order to validate the product on system before launching the final silicon. The second step is to implement the algorithms within the final silicon, validate and qualify the product as usual.

In this paper we present the development of a demonstrator, achieved combining an IC implemented in austriamicrosystems AG (AMS) HVCMOS 0.35 μ m technology and a Valeo Engine and Electrical Systems mechatronic regulator standard module mounted on an alternator, that can be used to develop a new type of smart and flexible regulators which implement many additional programmable functions that give the car maker a better control to reduce vehicle fuel consumption and CO₂ emissions. In the demonstrator all the implemented functions, including regulation, can be changed during the development phase and many properties, including loop stability, can be checked before releasing a final version of the regulator. The regulation principle is based on a closed loop, which maintains the reference voltage on the alternator output, sensed on the positive terminal of the battery, acting on the amplitude of the excitation magnetic field of the rotor coil through the power stage of the SoC. Since the regulation functions are integrated within the chip, but the loop includes the alternator and the connected loads (battery) that picks up the mechanical power on the engine and the rectifier, the analysis of the stability during the design phase is critical. The risk is to have a not stable regulator when the designed SoC is used in different vehicle platforms equipped with different equipments.

The paper is organized as follows: section II describes the state of the art of the voltage regulators used in automotive alternators, section III describes the implementation of the demonstrator system, section IV describes the IC design, section V presents the measurement results on silicon and section VI includes the conclusions.

II. VOLTAGE REGULATORS FOR AUTOMOTIVE ALTERNATORS

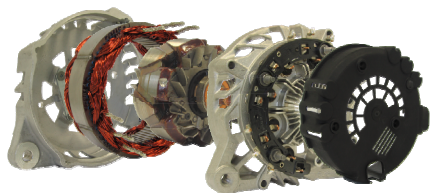


Figure 1. Alternator front bracket, stator, rotor, rear bracket - rectifying bridge, rear cover

The automotive alternators transform the mechanical power, picked up on the engine, in electrical power to be delivered to the battery and to the electrical loads of the car. The power machine (Figure 1) consists of the rotor and stator coils, that generate an alternating voltage, and the rectifier diode bridge, whose output is the DC voltage for battery and loads. The rotor coil, belt driven by the pulley and rotating with the engine, generates a magnetic field that is induced in the single or double three phase stator. Amplitude of the alternating voltages on the phases of the stator, and then the direct output voltage, depends on the amplitude of the biasing current of the

rotor coil and on its rotational speed. The biasing current is supplied to the rotor through a pair of brushes, which realize the electrical contact between static and rotating parts. This contact pair is included in a brush holder that is plugged on the power machine and contains the ASIC die, where the regulator functions are integrated.

The regulated alternators operate modulating the field current in the rotor coil, through the ASIC internal circuitry, to maintain an ad hoc voltage at the output of the rectifier bridge. This regulated voltage is sensed using directly the regulator supply voltage or a dedicated connection from the battery to an input pin of the ASIC. The regulator is woken up, through the ignition wire connection, as soon as the car driver turns the key ON. When the driver cranks the engine, the alternator is not running yet, then the battery delivers the power and its voltage decreases. When the alternator speed reaches a speed threshold, it delivers the electrical power and the regulator starts to regulate the battery voltage to its reference voltage. This speed threshold is necessary to avoid torque effect that could stall the engine during the cranking. When the key is turned OFF, the engine speed decreases and when the alternator speed becomes lower than a speed threshold, the alternator stops the power delivery. Two phases from the stator outputs are connected to the ASIC die in order to monitor the speed and the level of phase signals. The regulator communicates with the ECU through a dedicated connection and, in case of malfunction, alerts the driver switching on a lamp on the dashboard. Figure 2 shows physical blocks of a regulated alternator and electrical connections on the vehicle.

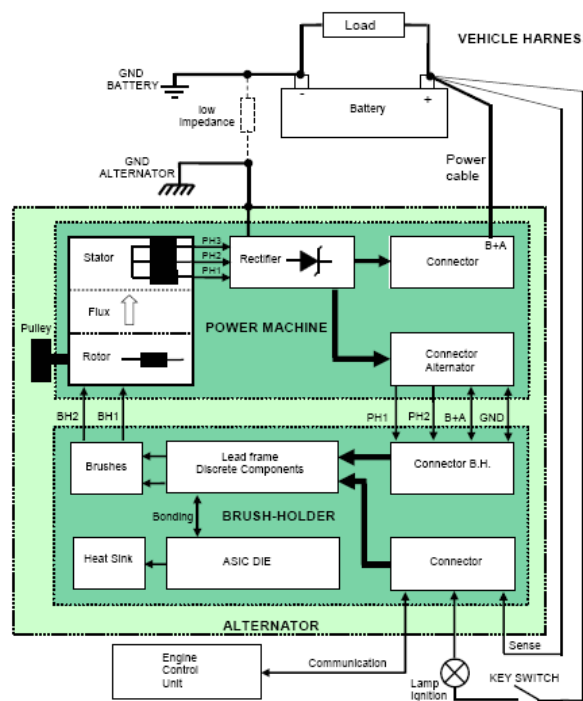


Figure 2. Regulated Alternator blocks and electrical connections

The mechatronic brush holder (Figure 3) includes on one hand the bare ASIC die silver glued directly on a heat sink and wire bonded on a lead-frame, and on the second hand the brushes and the connectors to the power machine of the alternator and to the vehicle engine control unit.

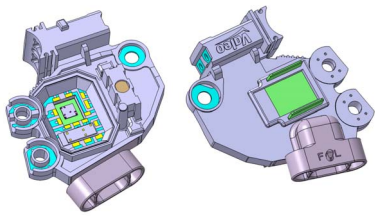


Figure 3. Mechatronic top and bottom views

The regulation principle is based on a closed loop, as depicted in the Figure 4.

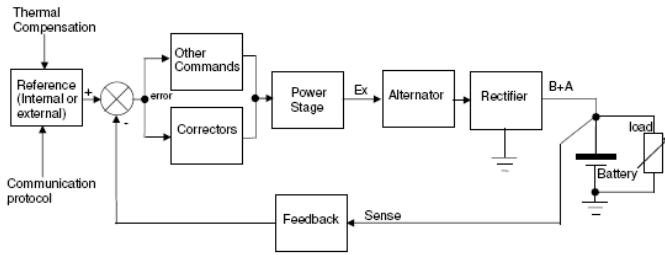


Figure 4. Regulation loop principle

The direct chain of the loop includes a proportional or proportional-integral error corrector, which acts on the amplitude of the excitation field generated by the rotor coil. The amplitude is controlled by the excitation duty cycle managed by the power stage. The excitation field induces a stator voltage that delivers current to the battery through the bridge rectifier. The feedback chain of the loop picks up the voltage amplitude signal on the battery, through the sense connection, and, after a proper and anti-aliasing filtering, converts it to the digital domain for comparison with the reference. Note that some regulator loops are fully analog. The result of the comparison is applied to the direct chain. The reference voltage is set by the internal or external reference. The feedback chain and the error corrector are integrated in the ASIC die, which power stage includes the rotor coil driving circuit. As Figure 5 shows, the rotor excitation coil is driven by an high side driver switch and a low side free wheeling diode.

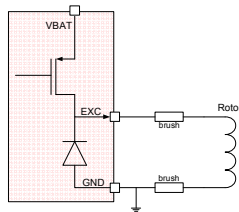


Figure 5. Rotor excitation driver

The gate of the high side switch is driven by a square wave fixed frequency signal in a range of 60Hz to 400Hz depending on a trade-off behavior stability versus power losses. Some regulators used free excitation frequency with a fixed duty cycle. Rotor current is modulated changing the duty-cycle of the square wave signal from minimum DC (0 % to 5%) to 100% (maximum field). Those differences are directly linked to customer specifications that have to be implemented in their dedicated product.

Alternator regulators are among the most demanding automotive SoC applications with respect to the combination of

harshest reliability requirements, such as temperature, voltage and current. The complete alternators are mounted in the engine compartment, where the under roof ambient temperature requirement (-40°C to 125°C) leads to a maximum operating junction temperature which is currently 150°C and up to 180°C - 200°C for future applications. The rotor coil that generates the excitation field of the alternator requires very high currents (up to 4 A) with a well controlled duty cycle to guarantee the regulation accuracy. During cold and cranking condition, the rotor current can even go up to 8 A. Fast current spikes up to 15A are observed in case of rotor short circuit. At present the maximum voltage requirement is 65V, which is the battery voltage overshoot limit due to alternator zener diode rectifying maximum voltage in case of unexpected harness surges. Note that all regulator pins shall be protected against sudden surges such as ESD and others sparkling pulses due to harness coupling. Considering that actually the swap of the battery pins can be one of the main causes of failure in alternators, the battery pin of the regulator has to withstand -3.2 V , which is the maximum voltage across the series of two power diodes of the rectifier bridge of the alternator in forward biasing conditions. All the other HV pins shall withstand a reverse polarity voltage of -15 V without damage in case of error during maintenance. Furthermore a ground shift can appear between the ground of the alternator and the negative terminal of the battery because of the high currents delivered by the alternator to the battery or sunk from the battery by the starter during cranking.

III. DESCRIPTION OF THE IMPLEMENTED SYSTEM

The implemented new type of intelligent and flexible alternator regulator with programmable functionalities is based on two different electronic parts: an IC (*electronics for interfaces*) and a FPGA (*electronics for algorithms*). The IC is used to manage the interfaces between the alternator, the power train signals and the FPGA and includes the power stage that supplies the current to the rotor. The FPGA, assembled on a mezzanine board, is the programmable brain of the regulator and communicates with IC through a 3-wire serial protocol. Both are located inside a standard brush-holder, making possible the test of the alternator directly inside a current car in a real environment (Figure 6).



Figure 6. Assembled brush holder with the IC (left) and mezzanine board with the FPGA (right)

The target is to use this demonstrator system to develop a new generation of regulators, with improved performances and higher flexibility, where the electronics for algorithms already validated in the demonstrator is transferred to the digital part of the IC. This approach reduces the risks and the costs of design changes and increases the possibility to adapt the product to the new requirements.

Figure 7 shows the proposed system architecture and the interconnections between the blocks.

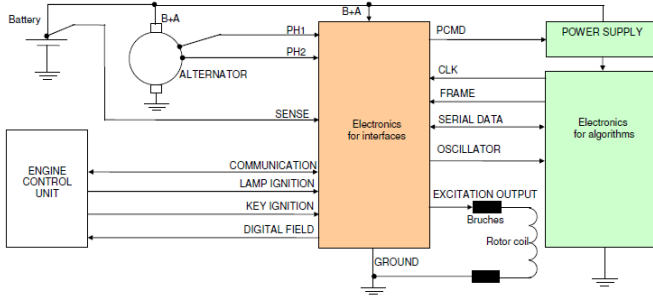


Figure 7. Electronics System block definition

A. Electronics for interfaces

The electronics for interfaces is in charge of signal adaptation and conversion and is connected directly to the alternator and to the ECU. It converts the sensed battery voltage to the digital domain (ADC) and sends, via the serial communication channel, the feedback data of the regulation loop to the electronics for algorithms. It also sends the information regarding the status of the alternator in the car, like key insertion, engine rpm and data received from communication with ECU. This part receives from the FPGA the information to manage the regulation function and the data to send to the ECU. The electronics for interfaces includes all the power stages: the power MOS for field excitation, the free wheeling diode and the power transistor for the lamp stage.

B. Electronics for algorithms

The flexibility of the FPGA, which is fully programmable in a very short time, allows the possibility to test on the system various algorithms as, for instance, different control loop solutions. The electronics for algorithms implements the regulation control loop making use of the data received from the electronics for interfaces (feedback voltage converted to digital) and generating the signals to drive it (duty cycle of the rotor excitation driver). Since this algorithm is programmable, the proposed mixed signal architecture solves many stability issues that arise during regulator development or when the designed regulated alternator is transferred from one vehicle platform to another with varied equipments and a different electrical power network.

The FPGA controls the functionalities of the entire alternator. Furthermore it manages the communication with ECU, coding and decoding the information, decides the state of the alarm lamp, turning it on when something goes wrong, and sends the power off signal when the engine is stopped.

IV. IC DESIGN

The IC was developed using the H35 technology from Austriamicrosystems. It is an high performance low cost HV-CMOS technology able to integrate on the same die low voltage and high voltage devices. The design has taken into account the required maximum junction temperature (at least 150°C), the maximum absolute voltage (at least 65V) and the reverse polarity requirements on pins. To guarantee the lifetime

of the battery charge when car is long time stopped it has been necessary to introduce a standby condition with reduced current consumption of the IC.

The implemented IC can be divided into 7 main blocks. A simplified block diagram of the IC is shown in figure 8:

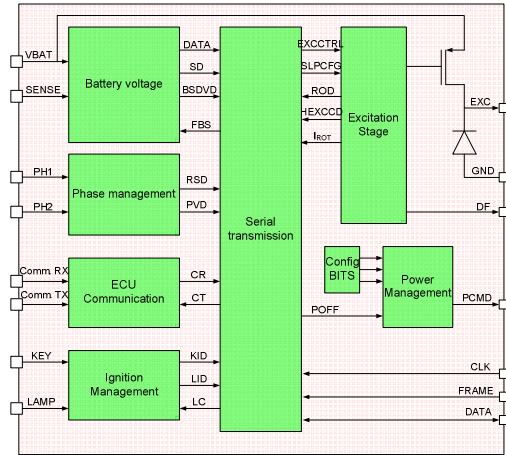


Figure 8. Simplified block diagram

1) Battery Voltage Block

The main task of this block is to generate a digital value from the voltage sensed on the positive battery contact, which is the feedback of the regulation loop. A 10bit ADC is used. The voltage drop on power cables caused by the large flowing currents is not included in the ADC conversion because a sense pin on battery contact (SENSE) is used. Depending on the car maker charge strategy and on diagnostic, the FPGA can select if the loop has to use the sense path or directly the supply path on the battery pin (VBAT) of the IC. Furthermore this block monitors the sense path and generates two digital signals (SD, BSDVD) that indicate if a failure on this path occurs. The SD signal informs the FPGA when the sense cable is connected or disconnected. This information can be used to control the close loop on the battery pin (VBAT) instead on the sensed output of the rectifier bridge. The BSDVD checks the voltage difference between the sense and the battery pins of the IC and it is used to indicate when an abnormal voltage is present between VBAT and SENSE. For instance a resistive path on sense can give a battery voltage sensing to the regulation loop lower than expected and the alternator voltage can increase. Consequently and for safety, the algorithm forces the control of the close loop to the battery voltage pin of the IC, avoiding electrical damages and overloaded battery.

2) Phase Management Block

This block measures the amplitude and the frequency on two of the three stator phases. The frequency on phases is measured as soon as possible when the alternator is in motion in order to manage the lamp status signal and the transition between pre-excitation mode (without regulation, a small current is supplied to the rotor, used to increase the magnetic field amplitude) and normal mode (with regulation). As soon as the amplitude voltage on phases is sufficient, the block starts to generate digital signals for FPGA with information about the rotational speed frequency of the engine (RSD signal) and the amplitude of the magnetic field (PVD signal). Particularly

these signals indicate to the electronics for algorithms when the amplitude on the phases is enough to wakeup from standby mode because alternator is rotating without ignition, and when the frequency to start the regulation mode is achieved. Furthermore the information on the rotational speed can be used by the algorithm to improve the performance of the system and sometime used for the driver speedometer.

3) ECU Communication Block

The ECU Communication block is composed by a receiver, a transmitter and an activity detector. The receiver and the transmitter operate as level shifter, translating from ECU levels to FPGA levels and vice versa. The activity detector is used in order to wakeup the IC when the ECU transmits some data.

4) Excitation Stage Block

The excitation stage is in charge to manage the current flow inside the rotor and includes the high side switch and the low side free-wheeling diode. In order to withstand reverse voltage on the battery side, a PMOS HV device, with a bulk driver circuit that avoids parasitic well diodes conduction in forward conditions (on the right in Figure 9), has been used as high side. In order to minimize power dissipation on the IC, the switch has a very low on resistance.

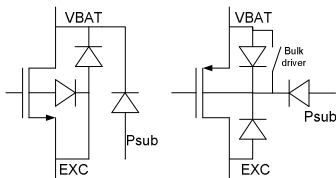


Figure 9. NMOS (left) and PMOS (right) parasitics diodes

The FPGA sends to this block the order to increase or decrease the rotor current changing the duty cycle of the EXCTRL signal, the PMOS gate control. The excitation stage turns ON or OFF the Power-PMOS according to the received order. Fast transients in the current sunk from the battery can generate undesired overshoots, oscillations and ringing on the battery voltage. To avoid them, for EMC compliance, the current through the high side has a slope controlled transient during the switching ON and OFF transitions, as shown in the section V. The FPGA, through a slope configuration signal, can select between a faster and a slower current slope, depending on the SLPCFG state. Furthermore this block can read the current flowing in the Power-PMOS, sending this information to the FPGA, and generates two error flags: one detects when the excitation is not connected to the rotor (ROD signal) and one turns off the Power-PMOS and alarms the FPGA in case of current too high through the Power-PMOS (HEXCCD signal). EMC conducted emissions are also reduced in this stage since a PMOS is used and the charge pump, necessary to drive the high side NMOS devices, is not needed.

5) Power Management Block

The power management block has the task of wake-up or shutdown the IC and the FPGA. In stand-by mode the current consumption of the IC is reduced below 200 μA and the FPGA is switched off. When the key is turned on, activity from ECU is detected or the engine starts rotation, this block sends the wakeup signal to the IC and the FPGA. In order to improve the IC wakeup strategy, it is also possible to decide, via a configuration bonding wire on the IC, which signal can not

wakeup it. Only the key ignition signal can not be left out. When the *electronics for algorithms* detects no activity on the signals, after a certain delay, it sends an order to the power management block, turning off the power supply. Figure 10 shows how it works.

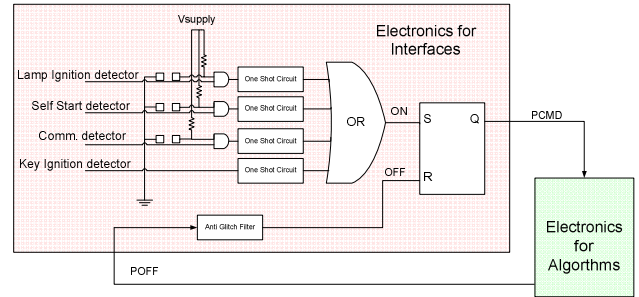


Figure 10. Power up strategies

6) Ignition Management Block

The ignition management block is in charge of detection when an ignition condition happens. It monitors the state of the key using two ways. The first monitors directly the key status indicating to the FPGA when the key is plugged and engaged, activating the KID signal. The second monitors the key with an alert lamp in series. In this way, is possible to monitor when the key is engaged (LID signal) and to drive an alert lamp that indicates to driver when something is abnormal, through the LC signal.

7) Serial Interface Block

The serial interface is in charge to manage the communications between IC and FPGA. It uses a 3-wire serial protocol with a clock frequency of 2.816 MHz. Two wires are used to receive the system clock and the communication direction (called frame) from FPGA to IC and the third wire is used for data exchange. The frame exchanged between IC and FPGA is composed by 43 bit (36 from IC to FPGA and 7 from FPGA to IC). Clock frequency has been chosen considering the number of bits inside a frame (N_{bit}) and both the quantization error on the duty-cycle of the excitation signal and the sample rate of the sensing ADC. For a good regulation the system needs a minimum sample rate of about 64 kHz and a resolution of about 1 by 256 on the excitation field duty-cycle. Considering (1), equation (2) was used to calculate the system clock frequency.

$$F_{exc} = 250\text{Hz}, N_{bit} = 44, N_{frame} = 256 \quad (1)$$

$$F_{clk} = F_{exc} \cdot N_{frame} \cdot N_{bit} = 250 \cdot 256 \cdot 44 = 2.816\text{MHz} \quad (2)$$

V. MEASUREMENT RESULTS

Finally the IC has been manufactured and assembled on the brush-holder together with the FPGA and has been measured. Measurements verified the correct functionality of the entire system, the standby current, the communication, the slope control and the reverse voltage protection. Other measurements evaluated the performance parameters, like ON resistance of the power MOS. This section presents the results on some IC parameters.

To check the slope control, the commands to turn on and off the power MOS have been sent to the IC from the FPGA, recording with an oscilloscope the voltage and the current

flowing in the PMOS. Figures 11 and 12 shows the excitation voltage (top) and the high side current (bottom) waveforms recorded with VBAT=12V. The IHS rotor current switches from 0 to about 2.8 A, while the EXC voltage is switching between -1V (free wheeling diode is conducting) and VBAT.

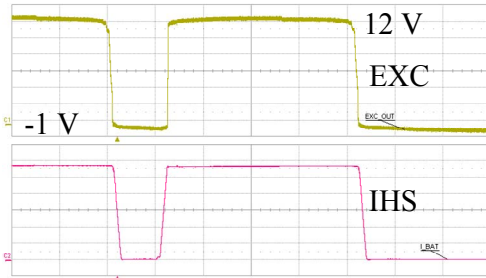


Figure 11. High side current switching transient

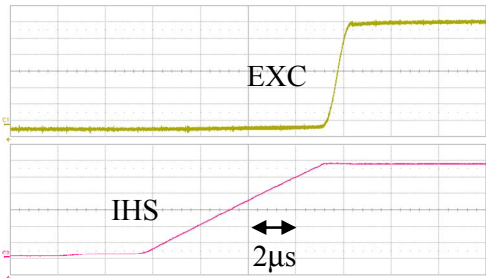


Figure 12. High side on sequence

Considering that the total current in the rotor inductor is almost constant and corresponds to the sum of high-side and free wheeling currents through the EXC pin, in fig 12 two main sequences are distinguished:

- At the beginning of the high side switching on phase the controlled current increases in the high side until the EXC voltage is negative (diode is conducting). During this time the freewheeling diode current decreases accordingly (the constant current in the rotor keeps roughly the voltage at -1V). At the end of the switching transient the current in the high side becomes constant, indicating that there is no more current in the diode and all the rotor current is coming from VBAT through the high-side switch.
- The voltage increases with a slope controlled by freewheeling diode capacitor and other parasitic components connected to the excitation node. During this time, an extra power is generated that can also be managed by the slope control.

Measurements show that the required slope controlled current switching from the high-side to the freewheeling diode is achieved.

The main heating part of an alternator regulator is the high side power MOS. To limit the heat produced is necessary to have a low ON resistance, according to (3). In table II the values measured at 3 different temperatures are shown. These values are below the maximum allowed resistance, fixed at 125 mΩ at 150°C.

$$P_{dis} = R_{on} I_{rot}^2 \quad (3)$$

TABLE I. ON RESISTANCE PMOS

ON Resistance PMOS			
Temperature (°C)	-40	27	150
Simulated R (mΩ)	45	61	82
Measured R (mΩ)	47	62	96

As required, the IC can withstand a reverse battery voltage of -3.2 V and a reverse voltage on the external pins of -15 V without any damage for itself. In table I the current absorbed in case of reverse bias is shown for each significant pin.

TABLE II. REVERSE VOLTAGE PROTECTION

Reverse voltage protection			
Pin	Voltage (V)	Simulated current (uA)	Measured current (uA)
VBAT	-3.2	12	14
PHASE1	-15	220	226
PHASE2	-15	220	226
COMM. RX	-15	4292	4346 ^a
COMM. TX	-15	14	14
DF	-15	14	14
SENSE	-15	59.3	61
KEY	-15	3000	3054 ^b
LAMP	-15	3815	3968 ^b

a. Internal pull-up resistor

b. Internal pull-down resistor

VI. CONCLUSIONS

The alternator regulator is an important device in the power train system as shown by the recent evolution during the last ten years in order to decrease fuel consumption. One major challenge is to meet the time-to-market expectations while keeping the flexibility to implement all the upcoming customer requirements to enhance the performances and to optimize the behavior for every car platform. The innovative approach using simulation and FPGA presented in this paper is an important step in that direction.

Today the demonstrator is performing as required in particular for reverse battery. The regulation loop has been simulated and now tested on bench with different algorithms. These tests have proven that the demonstrator is at the expected level for development of new concepts and functionalities. The test on vehicle is foreseen after this validation step.

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