Pseudo-CMOS: A Novel Design Style for Flexible Electronics

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Abstract

Flexible electronics have attracted much attention since they enable promising applications such as low-cost RFID tags and e-paper. Thin-film transistors (TFTs) are considered as an ideal candidate to implement flexible electronics on low-cost substrates. Most TFT technologies, however, have only mono-type – either n- or p-type – devices and thus modern design technologies for silicon-based electronics cannot be directly applied. In this paper, we propose a novel design style Pseudo-CMOS for flexible electronics that uses only mono-type TFTs while achieving comparable performance with the complementary-type designs. The manufacturing cost and complexity can therefore be significantly reduced while the circuit yield and reliability are also enhanced with the built-in capability of post-fabrication tuning. Some standard cells have been designed and fabricated in p-type organic and n-type InGaZnO (IGZO) TFT technologies which successfully verify the superiority of the proposed Pseudo-CMOS design style. To the best of our knowledge, this is the first design solution that has proven superior performance for both types of TFT technologies.

1. Introduction

Flexible electronics are emerging as an alternative to silicon electronics for applications such as low-cost RFID tags, sensors, e-paper, and flexible displays [1], [2], [3], [4]. TFTs are considered as an ideal candidate to implement flexible electronics, because of its compatibility with the low-temperature and low-cost processes on flexible substrates. Most TFT technologies summarized in Figure 1, however, have only mono-type – either n- or p-type – devices, due to their material properties. Complementary TFT circuits implemented with either homogeneous [5], [6] or heterogeneous TFT technologies [7] usually need to incorporate significantly slower and less reliable TFTs (e.g. n-type organic TFTs) or complex process integrations (e.g. organic and inorganic TFTs hybridization). This inevitably degrades the circuit performance, yield, and manufacturability. Furthermore, TFTs manufactured using low-cost printing methods, such as ink-jet print-
ing and roll-to-roll imprinting, often suffer from large process variations and degradations, which result in significant performance deviations and poor long-term reliability. A robust design solution to overcome these limitations and to be used as fundamental building blocks is therefore highly desirable.

Conventional mono-type digital designs such as diode-load or resistive-load inverter designs often suffer from high static power consumption and poor noise margin due to their ratioed-logic nature. Several designs based on mono-type TFTs have been proposed to resolve this problem but can only be used under certain TFT technologies [1], [8]. A comprehensive design solution is still missing. In this paper, we propose a novel design style, called Pseudo-CMOS, that has the following key features: 1) using only mono-type TFTs, 2) including gate-level built-in post-fabrication tunability to compensate for process variations and device degradations, 3) applicability to either enhanced or depletion-mode TFTs, and 4) operability under a low supply voltage (as low as 2V). Three different sets of circuit samples have been designed, fabricated, and measured to evaluate and validate the proposed solution. These samples use: 1) p-type self-assembled-monolayer (SAM) OTFTs on a silicon wafer, 2) n-type transparent IGZO TFTs on a plastic substrate, and 3) IGZO TFTs on a glass substrate.

The organization for the rest of the paper is followed. Section 2 will illustrate the device characteristics and structures of SAM-organic and IGZO TFT technologies. Section 3 describes the Pseudo-CMOS design style and measurement results based on p-type SAM OTFTs, including a comparison with other existing designs. More details of circuit analysis can be found elsewhere in [1], [9]. Measurement results of Pseudo-CMOS circuits based on n-type IGZO TFTs on both glass and polyimide plastic substrates will also be shown and analyzed. Section 5 concludes the paper with our future research.

2. Background – TFT Technologies

2.1. 2V SAM OTFTs

Figures 3(a) and (b) show the device structure and photo of a 2V SAM OTFT [10]. is shown in Figure 3(b). The gate dielectric is accomplished by first exposing the gate terminal Al to O₂ plasma ashing to grow AlOₓ (~ 6-nm) and the entire sample is then treated with the SAM solution (n-octadecylphosphonic acid) to provide a high gate capacitance while keeping a low gate leakage current. The semiconductor layer Pentacene is deposited using the thermal evaporation for higher carrier mobility (~ 0.5cm²/Vs). Thanks to the high gate capacitance of SAM-dielectric (~ 600µF/cm²), the SAM OTFTs can be operated with a gate voltage (V₉szę) at only 2V, which enables the use of the same supply voltage of CMOS LSIs for SAM OTFTs [10]. Figure 3(b) also shows the device layout with multiple source/drain (S/D) fingers that can increase the conduction current (I_DS) without a large area overhead. The I_DS-V₉szę plot in the log scale is shown in Figure 4(a) and the I_DS-V_DS plot in the linear scale is shown in Figure 4(b), where the device width W is 500 µm and the device length L is 50 µm. From these plots we can observe that the threshold voltage (V_TH) for this state-of-art OTFT technology is around 0.5V and the on/off current ratio is around 10⁵.

2.2. Transparent IGZO TFFs

IGZO TFTs are emerging as a promising technology candidate for display and sensor applications since 86% of visible lights can penetrate IGZO TFTs that makes the device transparent to human eyes. Figure 5(a) shows the device structure of a transparent IGZO TFT and Figure 5(b) shows a circuit sample on a plastic polyimide substrate that is attached to a 6-inch glass
Figure 5. (a) The sideview of an IGZO TFT, and (b) a circuit sample on a plastic polyimide substrate. (Glass wafer is used as the base for ease of circuit fabrications.)

Figure 6. $I_{DS} - V_{GS}$ relationship in the log scale for IGZO TFTs on (a) a glass substrate ($V_{TH} \sim 25V$), and (b) a polyimide plastic substrate ($V_{TH} \sim 0.1V$). Wafer, which is used to ease circuit fabrication. Two different substrates (glass and polyimide plastics) are used to fabricate our test circuits for the validation purpose. Figure 6(a) shows the $I_{DS} - V_{GS}$ plot for IGZO TFTs on a glass substrate in which six different curves correspond to six different dies from the same sample. The results reveal the excellent device uniformity on a glass substrate. The threshold voltage $V_{TH}$ is around 25V and the on/off current ratio is around $10^4$ for the glass sample. To further study the IGZO TFT characteristics on plastics, we have fabricated a circuit sample on a polyimide substrate and the $I_{DS} - V_{GS}$ plot is shown in Figure 6(b). Comparing this plot with Figure 6(a), we can see that the IGZO TFTs on a plastic substrates can still have a high carrier mobility ($\mu \sim 3cm^2/Vs$) and a high conduction current ($I_{DSAT} \sim 10^{-6}A$), but the gate leakage current rises significantly (from $10^{-12} \rightarrow 10^{-10}A$) and the threshold voltage $V_{TH}$ is reduced significantly (from 25V $\rightarrow$ 0.1V). The resultant circuit performance will be illustrated in Section 4.

3. Pseudo-CMOS in SAM-OTFTs

3.1. Pseudo-CMOS Inverters

To address the design challenges of using only mono-type TFTs, we proposed a novel design style called Pseudo-CMOS. More details of circuit analysis and simulations can be found elsewhere in [1], [9]. Figure 7 shows the schematics of Pseudo-CMOS inverters. There are two versions of Pseudo-CMOS inverters: Pseudo-E and Pseudo-D inverters. The differences between the Pseudo-E and Pseudo-D inverters are the gate connection of $M_2$ and the sizing ratio $W_1/W_2$. For the Pseudo-E inverter, $M_1$ and $M_{UP}$ work simultaneously to pull the output to high when the input is low. In the meantime, $V_{IM}$ is pulled to high so the $M_{DP}$ is switched off to prevent a direct current from $VDD$ to Ground in the $M_{UP}$ and $M_{DP}$ pair. On the other hand, the Pseudo-D inverter works in the same manner as the Pseudo-E inverter while $M_2 (V_{GS}=0V$ in the Pseudo-D inverter provides a much weaker ($\frac{R_{M2}}{R_{M1}} > 10^4$ in Fig. 7 ) pull-down force to discharge $V_{IM}$ to VSS when the input is high . This subtle difference will actually make a significant difference on the circuit performance. Furthermore, by adjusting VSS voltages, $V_{IM}$ can also be adjusted to control the pull-down force with $M_2$, which can be useful to enhance the circuit yield and reliability. Key characteristics of these mono-type and other complementary-type inverters [5], [6] are summarized in Table 1. Note that the static noise margin (SNM)
Figure 8. The inverter VTCs of proposed Pseudo-E and Pseudo-D inverters. Different curves correspond to VTCs under different VSS. The maximal achievable inverter gain is tunable and can be >20 for Pseudo-D inverters.

Figure 9. The inverter VTCs under different tuning voltages. (VSS = 0V and -2V)

Figure 10. Schematics of Pseudo-E and Pseudo-D NAND gates based on p-type TFTs

Figure 11. The transfer function of a two-input Pseudo-D NAND gate with one input fixed at VDD (a) When input B is fixed at VDD, and (b) when input A is fixed at VDD. The nearly identical curves reveal good input symmetry of the NAND gate.

Figure 12. The effects of VSS for a Pseudo-D NAND gate: (a) its transfer curves, and (b) the small-signal gain and its corresponding input voltage. (For the ideal case, the maximum-gain input voltage should be VDD/2.)

3.2. Pseudo-CMOS NAND Gates

To further study the potential of Pseudo-CMOS designs for larger scale integration, we designed and...
Figure 13. Schematics of Pseudo-E and Pseudo-D inverters based on n-type TFTs. ($\beta \sim \frac{1}{3}$ for Pseudo-E and $\beta \sim 4$ for Pseudo-D inverters.)

She fabricated 2-input NAND gates based on 2V SAM OTFTs, which is the most basic building block for digital design. The schematics of Pseudo-E and Pseudo-D NAND gates are shown in Figure 10. To evaluate the performance of a NAND gate, we fix one input of the NAND gate to be $V_{DD}$ and vary the other input to obtain a transfer curve similar to the inverter VTC. The resulting VTCs are shown in Figure 11. Figures 11(a) and (b) show the transfer curve of a Pseudo-D NAND gate when keeping input B and input A high, respectively. These two graphs indicate that this Pseudo-D NAND gate has a good input symmetry. The post-fabrication tunability of this NAND gate is illustrated in Figure 12. By adjusting the tuning voltage $V_{SS}$, the transfer curve, the small-signal gain, and the maximal-gain input voltage are tunable. This feature enables compensation for process variations and aging as well for enhancement of circuit performance. These results demonstrate that the Pseudo-CMOS NAND gates based on p-type TFTs, such as the SAM OTFTs, are sufficiently robust as a fundamental building block for larger scale digital design.

4. Pseudo-CMOS in IGZO TFTs

4.1. Pseudo-CMOS Inverters on Glass

To further verify the effectiveness of Pseudo-CMOS designs in n-type TFTs, we designed and fabricated digital cells based on IGZO TFTs on both glass and plastic substrates. Figure 13 shows the schematics of n-TFT-based Pseudo-E and Pseudo-D inverters. To compare different inverter designs, we designed, fabricated, and measured several inverters and the measurement results are shown in Figure 14. Based on Figures 14(a) and (b), it is clear that without using extraordinary large sizing ratio ($\beta > 5$), the small-signal inverter gain of the conventional Diode-Load and Phillips-RFID [1] designs is smaller than one, which fails to meet the minimum requirement of a workable inverter. On the other hand, fabricated on the identical substrate with the same technology, both Pseudo-E (Figure 14(c)) and Pseudo-D (Figure 14(d)) inverters achieve an inverter gain greater than 2, which make these inverters sufficiently robust. It should be noted that an even greater performance can be achieved by tuning the $V_{SS}$ voltage.

4.2. Pseudo-CMOS inverter on Plastics

The Pseudo-E and Pseudo-D inverters are also fabricated on a polyimide plastic substrate with identical design parameters as those on the glass substrate. Figure 15 shows the inverter VTC of a Pseudo-E inverter on a plastic substrate. The small-signal inverter gain ($\sim 6$) of this inverter is even greater than that on a glass substrate ($\sim 2.5$) and is therefore also sufficiently robust to be used as fundamental building blocks for larger scale of digital design based on IGZO TFTs.
Figure 15. The inverter VTC of a Pseudo-E inverter on a polyimide plastic substrate. Small-signal gain is around 6.

5. Conclusion

In this paper, we compare TFT technologies and illustrate the design challenges of TFT circuits. We also designed, fabricated, and measured some standard logic cells in Pseudo-CMOS design style based on three different TFT technologies: 1) p-type SAM OTFTs on silicon, 2) n-type IGZO TFTs on glass, and 3) IGZO TFTs on polyimide plastics.

The measurement results of logic cells based on 2V SAM OTFTs show that Pseudo-CMOS inverters and NAND gates can achieve performance comparable to their complementary-type counterparts, while with a lower manufacturing cost and greater reliability. In addition, the built-in post-fabrication tunability can compensate for the process variations and device degradation, as well as enhance the circuit performance. The measurement results of cells based on n-type IGZO TFTs also show the superiority of Pseudo-CMOS designs in comparison with prior art. To the best of our knowledge, this is the first comprehensive design solution that can be used for larger scale of circuits in flexible electronics.

Our future works include the development of an analog-to-digital converter (ADC) that is based on Pseudo-CMOS cells and the circuits applications will be in flexible sensors and displays.

References


