2009 EDAA PhD Forum at DATE

The EDAA/DATE PhD Forum offers the opportunity for PhD students to present their thesis work to a broad audience in the design automation and test community from both academia and industry. During the presentation at the DATE Conference it helps students to establish contacts when entering the job market. Also, representatives from industry and academia get a glance of state-of-the-art research in design automation and test. This year 47 submissions were accepted for presentation at a dinner reception. The review process was conducted by 17 internationally renowned reviewers. Our thanks goes to all presenters, the PhD Forum Committee, EDAA and the DATE organizers.
Peter Marwedel (Chair, 2009 EDAA PhD Forum at DATE)

PhD Forum Committee
P. Marwedel (Chair), TU Dortmund, Germany
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S. Stuijk, TU Eindhoven, Netherlands,
R. Ernst, TU Braunschweig, Germany

Accepted Presentations
J. Herter, Saarland University, »Precise WCET Analysis in the Presence of Dynamic Memory Allocation«
J. Reineke, Saarland University, »Predictability of Cache Replacement Policies«
U. Bordoloi, National University Singapore, »Interactive Design Space Exploration of Real-Time Embedded Systems«
P. Banerjee, ISI, Kolkata, »Faster Placement and Floorplanning in FPGAs«
W. Heirman, Ghent University, »Reconfigurable Optical Interconnection Networks for Shared-Memory Multiprocessor Architectures«
D. Göhringer, FGAN-FOM, Ettlingen, »Multi-Processor-based High Performance Computing utilizing dynamic reconfigurable Hardware»
K. Alsayeg, TIMA Laboratory, Grenoble, »Direct mapping of sequential QDI controllers«
M. Rashid, Thomson Research, »Design Space Exploration in Heterogeneous Embedded Systems«
A. Kumar, TU Eindhoven, Eindhoven, »Analysis, Design and Management of Multimedia Multiprocessor Systems«
A. Tisan, North University Maia Mare, »Contributions to the analysis, synthesis and implementation of applications with intelligent sensorial systems: The electronic nose«
H. Lipskoch, Carl-von-Ossietzky University Oldenburg, »Optimisation of battery operating life considering software tasks and their timing behaviour«
Q. Liu, Imperial College, London, »Data Reuse and Parallelism in Hardware Compilation«
H. Devos, Ghent University, »Loop Transformations for the Optimized Generation of Reconfigurable Hardware«
C. Moser, ETH Zürich, »Performance Optimization in Energy Harvesting Embedded Systems«
J. Keinert, Fraunhofer Institute Erlangen, »Data Flow Based System Level Design and Analysis of Image Processing Applications«

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J. C. Campos Costa, INESC-ID, Lissabon, »Coverage-Directed Observability-Based Validation Method for Embedded Software«
P. Lokuciejewski, TU Dortmund, »WCET-aware Source Code and Assembly Level Optimization Techniques for Time Critical Systems»
O. Boncalo, University of Timisoara, »Simulation Based Reliability Assessment of Quantum Circuits«
A. Hansson, TU Eindhoven, »A Predictable and Composable On-Chip Interconnect«
I. Loi, University of Bologna, »Synthesis of Low-Overhead Configurable Source Routing Tables for Network Interfaces«
B. Akesson, TU Eindhoven, »Designing Real-Time Systems-on-Chip Using Predictable and Composable System Services«
B. Prasad das, Institute of Science Bangalore, »Delay Variability: Modeling and On-chip Measurement«
L. Fossati, Dipartimento di Elettronica e Informazione, Milano, »Optimization and Design Space Exploration of MPSoCs«
A. Marongiu, University of Bologna, »OpenMP Support for MPSoCs with Explicitly Managed Memory Hierarchy«
A. Bartolini, University of Bologna, »DBS4video: Dynamic Luminance Backlight Scaling based on Multi-Histogram Frame Characterization for Video Streaming Application«
T. Beyrouthy, TIMA laboratory, Grenoble, »Secure Asynchronous FPGA for embedded systems«
F. Rogin, Fraunhofer Institute, Dresden, »An Integrated Approach to Utilize Designer‘s Debug Capacity in System-on-a-Chip Designs«
R. Klemm, TU Dresden, »A Processor Architecture and Compiler for Bitstream Processing«
S. Eggersgluess, Bremen University, »Robust Algorithms for High Quality Test Pattern Generation using Boolean Satisfiability«
S. Medardoni, University of Ferrara, »Designing Regular Network-on-Chip Topologies under Technology, Architecture and Software Constraints«
J.J. Murillo, Barcelona University, »A lightweight MPI-based programming model and its HW support for NoC-based MPSoCs«
A. Courtay, LabSTICC, Lorient, »On-chip interconnects energy consumption: High-level estimation and architectural optimizations«
G. Di Guglielmo, University of Verona, »On the Validation of Embedded Systems through Functional ATPG«
J. Lallet, IRISA-ENSSAT, Lannion, »Mozaïc: generic framework for modeling and design of dynamically reconfigurable architectures«
M. Ruggiero, University of Bologna, »Cellflow: a Parallel Application Development Environment with RunTime Support for the Cell BE Processor«
M. Modarressi, Sharif University, Teheran, »A Hybrid Packet-Switched and Circuit-Switched On-Chip Network Based on Spatial-Division Multiplexing«
S. Schliecker, TU Braunschweig, »Performance Analysis for Multiprocessor Systems-On-Chip«
C. Paci, University of Bologna, »How to Live with Uncertainties: Exploiting the Performance Benefits of Self-Timed Logic In Synchronous Design«
M. Palla, Bremen University, »Reduction of Crosstalk Pessimism with the consideration of logic and timing correlations«
K. Petersén, KTH/ICT/ECS Kista, »A highly scalable and (almost) c-testable BIST for NoCS«
V. Rana, Milano University, »A Reconfigurable NoC-based Communication Infrastructure for Multi-Processor SoCs«
M. Rößler, TU Chemnitz, »Parallel Hardware- and Software Threads in a Dynamically Reconfigurable System on a Programmable Chip»
C. Baloukas, University of Thrace, »Data structures optimization methodology of Dynamic Applications in Embedded Systems«
P. Bertels, University of Ghent, »Analysing Communication Leads to More Effcient Systems«
S. Garg, Siddharth, CMU, Pittsburgh, »Variability Analysis and Mitigation at the System Level«
C.-C. Kuo, University of Taiwan, »Efficient Bottom-up Approaches to Build Variation-aware PLL Behavioral Models«
S. Golshan, UC Irvine, »Novel Algorithms to Mitigate Soft Errors in SRAM-based Programmable Systems«