Efficient Reliability Simulation of Analog ICs Including Variability and Time-varying Stress

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***Abstract*—Aggressive scaling to nanometer CMOS technologies causes both analog and digital circuit parameters to degrade over time due to die-level stress effects (i.e. NBTI, HCI, TDDB, etc). In addition, failure-time dispersion increases due to increasing process variability. In this paper an innovative methodology to simulate analog circuit reliability is presented. Advantages over current state of the art reliability simulators include, among others, the possibility to estimate the impact of variability and the ability to account for the effects of complex time-varying stress signals. Results show that taking time-varying stress signals into account provides circuit reliability information not visible with classic DC-only reliability simulators. Also, variability-aware reliability simulation results indicate a significant percentage of early circuit failures compared to failure-time results based on nominal design only.**

I. Introduction

Increasing reliability challenges due to high electric fields in modern CMOS technologies raise the need for reliability-aware design. According to the ITRS roadmap both analog and digital ICs start to suffer from die-level reliability phenomena, e.g. Negative Bias Temperature Instability (NBTI) and Hot Carrier degradation (HC) [1], [2]. Statistical circuit analysis through accelerated stress testing (i.e. Test For Reliability or TFR) becomes too expensive due to an increasing demand for very low failure rates.

To cut the costs and solve reliability problems in the design phase of an IC, a need for process variability-aware reliability simulators arises (i.e. Design For Reliability or DFR). Both the TFR and DFR design cycle are indicated on Fig. 1. Bestory et al. [3] used behavioral circuit models to calculate the circuit reliability under process variations. This approach, although it is fast, lacks accuracy especially in nanometer CMOS when short-channel effects, usually not included in behavioral models, come into play. Others [4], [5] used circuit simulations based on SPICE netlists to increase simulation accuracy, but focused their work on digital circuits, performing only a DC operating point analysis to calculate the degradation. For analog circuits DC-only analysis is too inaccurate and provides little or no information regarding true circuit reliability.

Section II of this paper discusses the development of degradation models for the most important die-level reliability issues degrading analog circuits. Sections III and IV propose a variability-aware reliability simulation methodology optimized for the simulation of analog ICs in nanometer technologies. A Monte-Carlo loop is used to include statistical variations

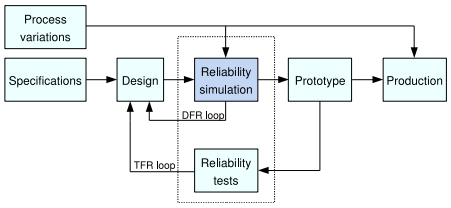

Fig. 1. Design cycle with DRF loop.

while simulating the reliability of a circuit. This allows to perform a failure rate analysis for any failure criterion. The methodology is demonstrated on a very common analog circuit in section V. Results show that, although simulations with nominal component values do not always indicate a reliability problem, variability-aware simulation can reveal a significant part of the initially working devices to fail early. Finally conclusions are drawn in section VI.

II. Degradation Models

In this work we discuss models for HC degradation and NBTI, which are considered to be the most important phenomena for analog circuits. Both phenomena affect different transistor parameters (e.g. the threshold voltage V_{TH}, the carrier mobility β and the output conductance g_o). However, since expressions for all degrading transistor parameters can be derived from the threshold voltage V_{TH} [6], we will continue to work with V_{TH} from here on. The time-dependent behavior of V_{TH} can, for both HC and NBTI, be described as a power-law function of time [7]:

$$V_{TH} = V_{TH0} + At^n \quad (1)$$

$$A = f(V_{DS}, V_{GS}, V_{TH0}, T, W, L, \dots) \quad (2)$$

where V_{TH0} is the initial threshold voltage (for an unstressed device) and n is a degradation parameter related to the type of degradation effect (about 0.5 for HC and 0.18 for NBTI). A is a function of geometrical (e.g. L), environmental (e.g. temperature T) and process-related (e.g. V_{TH0}) transistor parameters. Although we consider both degradation effects to be deterministic on their own (they are controlled by a deterministic diffusion process [7]), degradation dispersion occurs due to statistical variations of process-related and

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geometrical transistor parameters:

$$\sigma^2(\Delta V_{TH}) = \left[1 + \frac{dA}{dV_{TH0}} t^n\right]^2 \sigma^2(\Delta V_{TH0}) + t^n \sigma^2(\Delta A) \tag{3}$$

Equation (3) is already quite complex, although it assumes no correlation between different transistor parameters and only a small deviation of V_{TH} from V_{TH0}. The equation indicates how different, statistical transistor parameters induce dispersiveness in the degradation of different, identically designed, transistors.

The degradation models in this work are based on what is available in literature today. Both NBTI and HC increase exponentially with the stress voltage [2]. Therefore, the effect of time-varying stress signals must be included in the model to assure a sufficiently accurate degradation calculation. Also, prior degradation already present in the transistor must be taken into account. A general degradation model, valid for both NTBI and HC, can be deducted from [8]:

$$V_{TH}(t) = \left[{V'_{TH}}^{1/n} + \left(C exp\left(\frac{\beta V_{GS}}{\alpha}\right)\right)^{1/n} (t - t') \right]^n \tag{4}$$

where V'_{TH} represents the degradation present at time t' and α is a process-dependent parameter, to be determined through measurements. β is a parameter including the effect of time-varying stress signals with an average value V_{GS}. C is a parameter that is a function of other transistor parameters (e.g. V_{DS}, T, L, ...) and is different for either degradation phenomenon. We already presented a HC degradation model in previous work [6]. For NBTI, values for the process-related parameters in equation (4) are extracted from measurement results in [9].

III. Reliability Simulation for Analog Circuits

Here we present a novel and efficient method for reliability simulation. It uses a short transient simulation that provides accurate information about the stress at every circuit node, while a degradation extrapolation ensures a fast simulation result. Fig. 2 gives a schematic representation of this reliability simulation algorithm. The input to the simulator is a fresh (i.e. unstressed) netlist. A transient simulation over time T_{tr} with step size t_{tr} is performed on the input netlist. As circuit input a periodic time-varying signal, $v_{in}(t)$, with period T_{in} is applied.

$$T_{tr} = n_p T_{in} \text{ with } v_{in}(t) = v_{in}(T_{in} + t),\ \forall t \tag{5}$$

$$t_{tr} = T_{tr}/n_{tr} \tag{6}$$

where n_p is the number of periods of the input signal and n_{tr} the number of transient simulation points. Typical values are $n_p = 1$ and $n_{tr} = 10$. The impact of completely arbitraty (i.e. non-periodic) input signals can only be calculated using a transient analysis over the entire operating period of the circuit; obviously this is not feasible. However, the operation of most electronic systems is based on the execution of periodically executed algorithms (e.g. MPEG encoding). The restriction to periodic input signals is therefore not considered as a real limitation to this reliability simulation method. Once the stress pattern on every transistor node is calculated from this initial simulation, it is extracted and passed on to a degradation model (also see Fig. 2). The degradation model is set up as described in section II and extrapolates the transistor degradation to the desired circuit operation time. Finally, a degraded version of the netlist is created as an output [10]. A designer can use this output to study the impact of degradation on the circuit specifications.

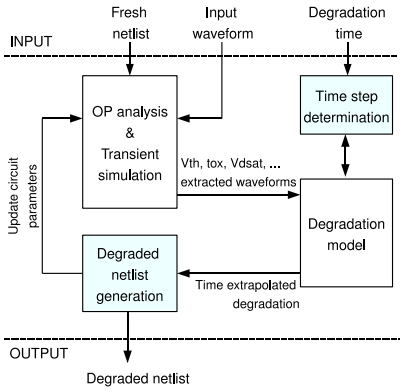

Fig. 2. Schematic representation of the presented degradation simulation method with short transient simulation and degradation extrapolation.

The simulation algorithm has a linear complexity $O(n)$ with respect to the number of transient simulation points n_{tr} per simulation time-step n_s (see equations (5) and (6)):

$$t_{sim} \sim n_s n_{tr} n_{mos} \tag{7}$$

where n_{mos} is the number of transistors in the circuit and t_{sim} the circuit simulation time. A good value for n_s strongly depends on the topology of the circuit and the nature of the input signals, but is typically around 10.

IV. Variability-aware Reliability Simulation

Modern nanoscale CMOS technologies exhibit an increasing process variability which sharpens dispersion of the failure-time. In section V we will shown that a fair amount of product samples can have an early failure-time due to local and global process variations.

Algorithm 1 gives a pseudo-code version of how process variability is dealt with in this paper. A Monte-Carlo (MC) simulation is used to obtain n_{mc} random samples of the same circuit. On each MC version of the circuit a reliability analysis is performed using the reliability simulator described in section III. For every specification P, the MC-based simulation generates a $P^{n_s \times n_{mc}}$ matrix (with n_s the number of time points in every reliability simulation). At every time point k from 1 to n_s an appropriate distribution function (PDF) f_k is found using the data in $P^{n_s \times n_{mc}}[k, :]$. The top picture of Fig. 3 gives the parameter density function for a performance specification P of an arbitrary, non-existing, circuit at time $T_d = 0$ and after an arbitrary stress time. Clearly, the distribution is shifted with

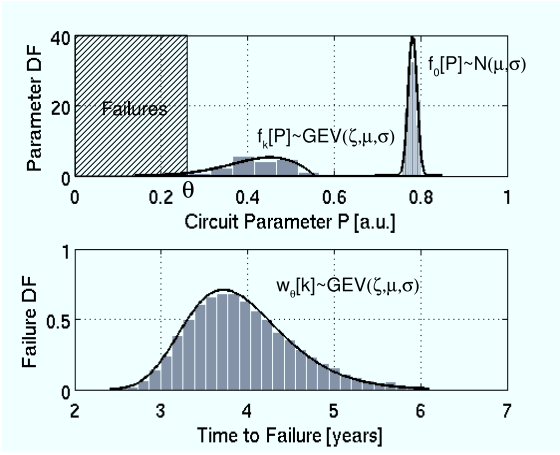

Fig. 3. Illustration of PDF time-behavior for a performance specification P and the resulting failure DF with failure criterion θ.

time and some samples now fail the performace criterium θ. To find a good expression for f_k, a chi-square goodness-of-fit test is used with test statistic:

$$X^2 = \sum_{i=1}^{n} \frac{(O_i - E_i)^2}{E_i} \tag{8}$$

where O_i is the observed frequency for bin i and E_i is the expected frequency for bin i. Finding f_k allows to get a more accurate prediction of the failure rate $w_\theta[k]$, with θ the failure criterion for specification P. The bottom picture of Fig. 3 illustrates how a failure density function $w_\theta[k]$ is fitted with a generalized extreme value (GEV) distribution, indicating the failure-time distribution of the circuit.

In contradiction to [3], this work uses a SPICE-netlist-based reliability simulation (see section III) to analyze the failure rate. This provides a more accurate and detailed picture of how a circuit will behave under degradation, especially for nanometer CMOS where short-channel effects are emerging. Today's computer power allows us to simultaneously perform multiple Monte-Carlo simulations, enabling reasonably fast simulation times.

V. Results

To illustrate and validate the variability-aware reliability simulation methodology presented in this paper, a typical analog circuit, being an LC-VCO, is analyzed. The degradation models for both HC and NBTI used in the simulator are verified and characterized through measurements on single devices [9], [6]. The example is simulated in a 90nm technology. Using one core of an Intel Dual Xeon Quad 2833 one MC run took, for this example, only 30 seconds.

Fig. 4 shows a schematic of the LC-VCO under study. Large voltages at the drains of the cross-coupled transistor-pair cause these transistors to suffer from hot carrier degradation. Fig. 5 shows the effect of degradation on both the oscillation frequency and the output swing for nominal design parameters (no statistical variations). The frequency of the LC-oscillator

Algorithm 1 Variability Aware Simulation

1: **for all** MC samples q in range 1 to n_{mc} **do**
2: Perform Monte Carlo simulation and calculate degraded specifications using section III
.MC runnb=q
$\overrightarrow{P_q} = f\left(\overrightarrow{\Delta V_{TH_j}}, \overrightarrow{\frac{\Delta g_{o_j}}{g_{o_j}}}, \overrightarrow{\frac{\Delta \beta_j}{\beta_j}}\right)$
with $j = \{1, 2, \ldots, n_{mos}\}$ and $\overrightarrow{P_q} \in \mathbb{R}^{n_s}$
3: **end for**
4: Create performance array
$P^{n_s \times n_{mc}} \in \mathbb{R}^{n_s \times n_{mc}} = \{\overrightarrow{P_0}; \overrightarrow{P_1}; \ldots; \overrightarrow{P_{n_{mc}}}\}$
5: **for all** time-steps k in range 1 to n_s **do**
6: Define Cumulative Distribution Function (CDF) array
$F_k = \{\underbrace{\text{EXP,NORM,GEV,}\ldots}_{n_d}\}$
7: **for all** distributions d in range 1 to n_d **do**
8: Determine appropriate distribution
$\forall u \in \overrightarrow{P_k} = P^{n_s \times n_{mc}}[k, :],\ u \sim F_k[d]$
$\Leftrightarrow X^2_{k,d} \geq X^2_{(\alpha, n_{mc}-\kappa)}\ \&\ X^2_{k,d} > X^2_{k,d'}, \forall d' \neq d$
with γ the degrees of freedom for $F_k[d]$,
significance level α and $X^2_{k,d}$ using equation (8)
9: **end for**
10: Calculate failure rate CDF
$w_\theta[k] = F_k[d](x = \theta)$
11: **end for**

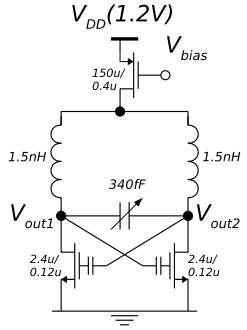

Fig. 4. Low phase noise LC-VCO.

is not affected by degradation; the output swing, however, decreases over time. After 6 months, the oscillator output swing has already reduced to less than 75% of the original output swing and in one year time the oscillator stops working due to transistors subjected to time-varying stress signals.

Fig. 5 indicates how the oscillator output swing has already reduced to less than 75% of the original output swing after only 6 months.

Also drawn on Fig. 5 is the simulation result for a DC-only reliability simulation, not showing this degradation behavior at all. To estimate the impact of transistor degradation under process variability, a formula for the variance of the output

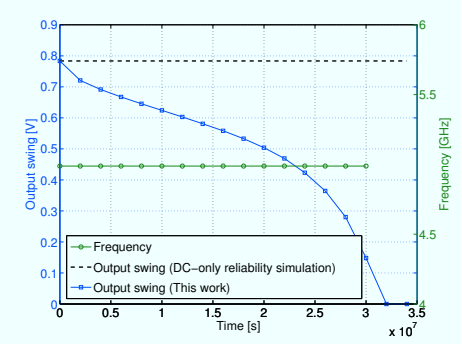

Fig. 5. Nominal time-dependent frequency and output swing behavior of the VCO under hot carrier stress.

voltage swing can be derived:

$$\sigma^2\left(\frac{\Delta V_{out}}{V_{out}}\right) = \sigma^2\left(\frac{\Delta\beta}{\beta}\right) + \left(\frac{2}{V_{GS}-V_{TH}}\right)^2 \sigma^2\left(\Delta V_{TH}\right) \tag{9}$$

where $\sigma^2\left(\Delta V_{TH}\right)$ is given by equation (3) and $\sigma^2\left(\Delta\beta\right)$ can be derived from (3) using [6]. Equation (9), however, provides little or no insight in the effect of process variability on the degradation of the circuit specifications. The methodology presented in this paper provides a solution to that problem. Fig. 6(a) shows the behavior of the oscillator, when subjected to process variability. 300 statistical samples were simulated over a time-span of 1.2 year in time-steps of 20 days. To study the failure rate of this circuit, a device is considered as defective when $V_{out} < 0.6$V. Fig. 6(b) shows the failure time dispersion of the oscillator due to local and global errors of transistor parameters. Fig. 6(c) gives a Cumulative Distribution Function (CDF) of the failure rate, fitted with a weibull distribution. Although a reliability simulation of the nominal circuit (not including variability) indicates a failure time of 6 months (see Fig. 5), running a variability-aware reliability simulation shows that 20% of the circuits already fail in less than 4 months (also see Fig. 6(c)).

VI. Conclusions

In this paper, we have proposed an efficient reliability simulator for analog circuits including the effect of time-varying stress using a short transient simulation with degradation extrapolation. Additionally a Monte-Carlo-based statistical analysis provides failure rate data for any given circuit specification. Results have shown this approach to have many advantages over the current state of the art in reliability simulators: the simulation methodology presented in this work indicates failures that DC-only, nominal-only simulation algorithms cannot detect.

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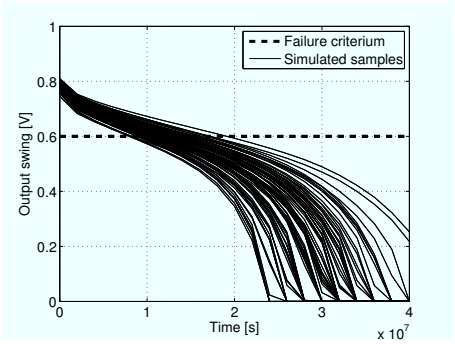
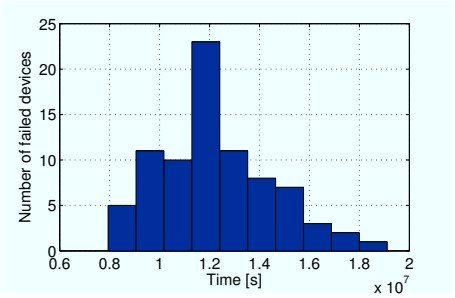
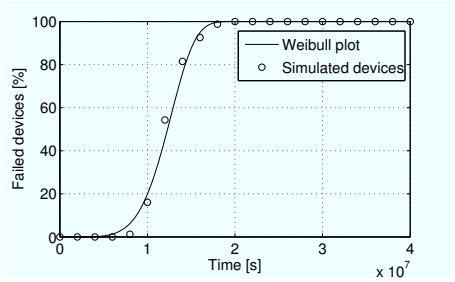


(a)



(b)



(c)

Fig. 6. Variability-aware reliability analysis of an LC-VCO. Dispersion of the output swing for 300 samples (a). A histogram of the failure rate (b) and a CDF of the failure-time (c) with failure criterion $V_{out} < 0.6V$.

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