# Package Routability- and IR-Drop-Aware Finger/Pad Assignment in Chip-Package Co-Design

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***Abstract*—Due to increasing complexity of design interactions between the chip, package and PCB, it is essential to consider them at the same time. Specifically the finger/pad locations affect the performance of the chip and the package significantly. In this paper, we have developed techniques in chip-package codesign to decide the locations of fingers/pads for package routability and signal integrity concerns in chip core design. Our finger/pad assignment is a two-step method: first we optimize the wire congestion problem in package routing, and then we try to minimize the IR-drop violation with finger/pad solution refinement. The experimental results are encouraging. Compared with the randomly optimized methods, our approaches reduce in average 42% and 68% of the maximum density in package and 10.61% of IR-drop for test circuits.**

## I. Introduction

In traditional design methodology, the core and package of the chip are designed separately, as shown in Fig. 1(A) and (B). Core designers assume that the package problem would not affect the performance of the chip, however the performance, complexity and noise of the package critically affect the chip[13]. In the new chip design paradigm such as 3D-IC[8], the package design absolutely determines the final quality of the chip. Therefore, a high quality package design is needed in the modern chip design.

As Very Large Scale Integration(VLSI) technology enters the nanometer era, chips contain more functions and are expected to have much better performance. At the same time, finger/pad[1] counts continue to increase. This adds up more routing complexity in the package design. In early package technologies, the number of available finger/pad count is small, such as Dual In-line Package(DIP) or Pin Grid Array(PGA). The Ball Grid Array(BGA) is a popular package technology in the modern package design because it can handle the high finger/pad counts to connect to the Printed Circuit Board(PCB). The package design flow can be divided into several parts, as shown in Fig. 1(A). The major problem in package design is routing. Many researches [16][7] have proposed various approaches to solving the routing problem in package design. Using finger/pad assignment to improved the package routing is another alternative. In [6][11][2], the authors proposed many assignment algorithms to improve routing problem. Because these methods can only handle the small finger count($< 20$), the modern chip design can not utilize these methods to improve the routing issue in the early stage. A better planning method which can handle great finger/pads is needed in modern package design.

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[1]Finger is called landing pad in some parts of package papers and patents.

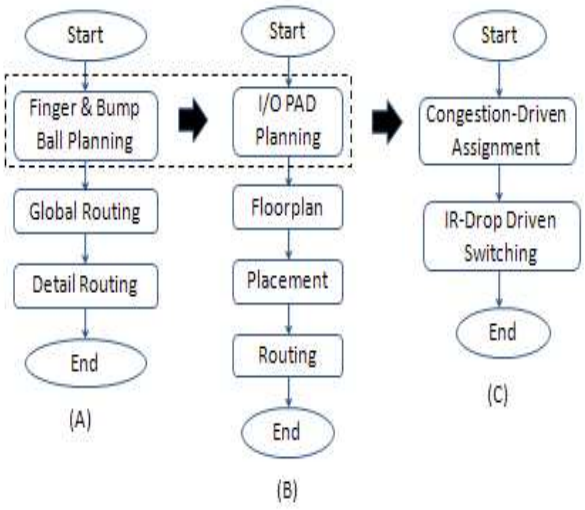


Fig. 1. (A) The flow chart of the package design. (B) The flow chart of the IC physical design. (C) Our Co-design Methodology. The package and core designs are independent in the traditional design flow. The co-design method can simultaneously solve package and core problems, and the developed time of the chip can be shortened.

Many package designers only consider the package issue when they plan the finger/pad location. In reality, the finger/pad not only affects the package routing, but also impacts the noise margin of the core. In modern chip designs, supply voltages continue to drop, which helps to reduce power dissipation, but also decreases the noise margin of devices. Noise margin interference will sometimes lead to erroneous chip functions, seriously reducing chip performance. As a result, the integrity problem has become one of the major factors affecting chip yield. Basically, integrity issues can be categorized into signal integrity problems and power integrity problems. IR-drop is one of the important parts in power integrity. Many researches have proposed various approaches to solving this problem in every design stage, the power/ground (P/G) network design [10] [15] [14] [4] is one of the effective ways to address IR-drop problems. IR-drop can be greatly improved by a better P/G network with minimal penalty cost. Besides planning the power/ground (P/G) network, adjusting power pad location is a common approach to reducing IR-drop noise. In [3], authors proposed a pad assignment method to improve IR-drop.

As we mentioned earlier, the core and package problems are solved separately. In modern chip design, this principle would cause the over-design problem. Package designers usually use a finger planning method to improve package routing, and core designers propose a noise-driven I/O planning method to improve IR-drop of

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a core. To build a functionally correct chip, we should over-design the chip to mitigate routability(noise)-related issues in the finger planning(I/O planning) step. The over-design brings two disadvantages: longer cycle time of the chip design and more design cost. If we perform chip-package co-design to simultaneously compute the interdependent influence of IR-drop and package routing across die and chip, the disadvantages can be easily eliminated.

In this paper, we develop a two-step approach to simultaneously improving the package routing and IR-drop of the core at the finger/pad assignment step. This method includes one congestion-driven assignment and one IR-drop driven exchange approach, as shown in Fig. 1(C). Our contributions presented in this paper are summarized as follows.

- We present a finger/pad assignment method to minimize the maximum wire congestion, and propose a finger/pad exchange method to improve IR-drop of the core. The assignment result can certainly lead to a legal routing solution.
- We propose an efficient estimation to analyze the wire congestion before routing. This method does not need to analyze the whole substrate, and it can directly find the most congested region.
- We have developed a co-design methodology to simultaneously consider the package and core in finger/pad planning. The cycle time of the chip design and the chip cost is shortened.

The rest of this paper is organized as follows. Section II describes the package architecture, finger/pad assignment design with congestion and IR-drop consideration, and the problem formulation. Section III presents two congestion-driven assignment methods and one finger/pad exchange method to improve wire congestion and IR-drop. Section IV shows experimental results, and Section V presents conclusions.

## II. Congestion and IR-Drop Violation Minimization in Finger/Pad Planning

As VLSI technology enters the nanometer era, chips contain more functions and are expected to have much better performance. To deliver large amount of signals, finger/pad counts are continually increased and the complexity of package routing is greatly raised. The finger/pad not only affects the package routing, but also impacts the IR-drop of the core. This study focuses primarily on these problems. We firstly introduce our package model, and then the sources of the package routing and the IR-Drop problems are described. Finally, we formulate the target problem in this work.

### A. BGA Package : Architecture and Routing

According to modern package technology, we can utilize multiple layers for package routing. In our package model, there are two layers for routing, die on the top layer of substrate, and the bump balls on the bottom layer of substrate. The fingers, which are the relay from the pad to the package substrate, are placed as a closing rectangle on Layer 1. The pads are connected to fingers by wire-bond and flip-chip[1] technologies. Wire-bond packages are cheaper than flip-chip packages, therefore we adopt the wire-bonding technology to connect the die and the package substrate in our package module. The detailed architecture is shown in Fig. 2. Fig. 2(A) is the vertical view and (B) is the profile. Bump balls, which are connected to the printed circuit board, are uniformly distributed on Layer 2. The net between the finger and the bump ball is implemented within a package substrate on Layer 1 and Layer 2. The function of the via is to connect a wire on Layer 1 and another wire on Layer 2, as shown in Fig. 2(B). In addition, we partition the package area into four parts and solve the package problem individually. We also assume that the fingers order and the pads order are the same.

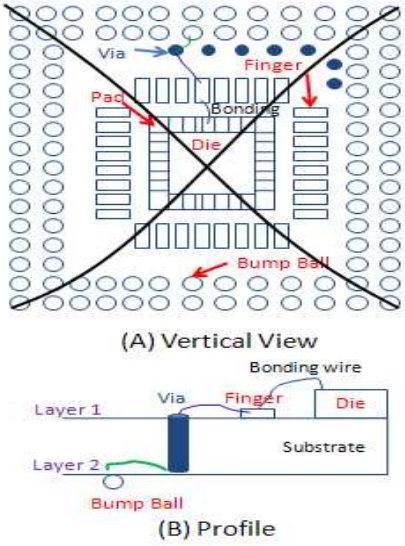


Fig. 2. The architecture of two-layer ball grid array package used in this paper. (A) is the vertical view and (B) is the profile. We partition the package area into four parts, and solve the package problems individually.

Because the via number affects the performance and the area of the package, the via number of each net is set as 1 in our package routing. Besides, candidate locations of vias are around the bump ball. The number of the via between four adjacent bump balls is at most one. In [7], the authors proposed a global routing method to plan the via location and the net path, and the routing result complies the monotonic characteristic. The monotonic characteristic is that the net from the finger to the bump ball intersects every horizontal grid line only once. Therefore, the detour routing would not occur and the wire length can be reduced. We adopt the idea of [7] to plan the via location and the routing path for the same purposes.

### B. The Impact of Finger/Pad Locations on Wire Congestion

If too many wires pass through a narrow range in a routing result, design rule violations may occur. Because the vias are evenly distributed on the substrate in our package, we compute the wire count between two continuous vias, and the wire count is called the density. If the density is higher, we should spend more package areas to solve the routing problem at detailed routing step. Therefore, developing a good method to improve the density is essential. The relation between the density, via location and routing method is detailed in [7]. We focus on the relation between the density and the finger/pad location in this work.

A good finger/pad assignment can help to reduce the density of the package routing. We use an example to explain the relation between the density and the finger/pad assignment. To display the importance of the finger/pad assignment, the via location and the routing method is fixed in the example. In Fig. 3(A), we use random method to generate the finger order, $10, 1, 2, 3, 11, 6, 9, 4, 5, 8, 7, 0$. Fig. 3(B) uses a congestion-driven assignment method to generate the new finger order, $10, 11, 1, 2, 6, 3, 4, 9, 5, 7, 8, 0$. Compare Fig. 3(B) with (A), the maximum density can be reduced 50% when we merely change the finger order.

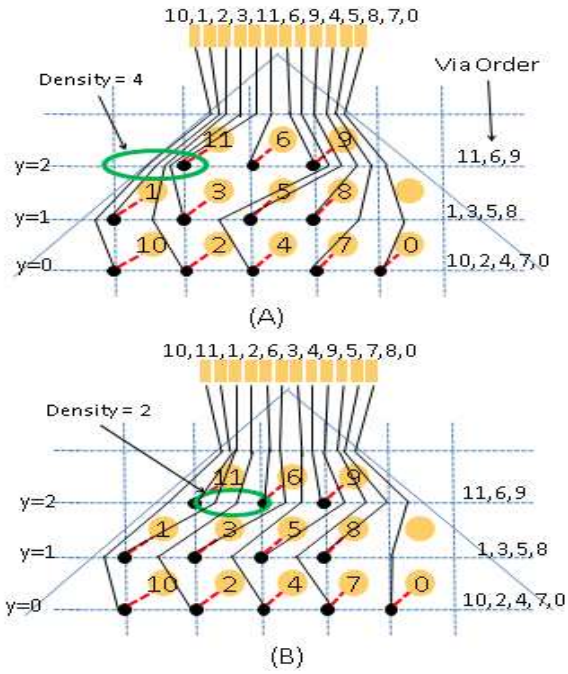


Fig. 3. The relation between the density and the finger/pad location. (A) uses a random method to generate a finger order and the maximum density is 4. (B) uses a congestion-driven assignment method to obtain another finger order and the maximum density is 2.

$$\frac{V_{IR}(x,y)-V_{IR}(x-\triangle x,y)}{R_{sx}\frac{\triangle x}{\triangle y}}+ \frac{V_{IR}(x,y)-V_{IR}(x,y-\triangle y)}{R_{sy}\frac{\triangle y}{\triangle x}} = -J_0\cdot\triangle x\cdot\triangle y \quad (1)$$

where $V_{IR}(x,y)$ is voltage of a point $(x,y)$, $J_0$ is current current density, and $R_{sx}$ and $R_{sy}$ are the resistances in $x$ and $y$ directions. According to EQ(1), we can exchange power pad locations to minimize $\triangle x$ and $\triangle y$ to improve IR-drop.

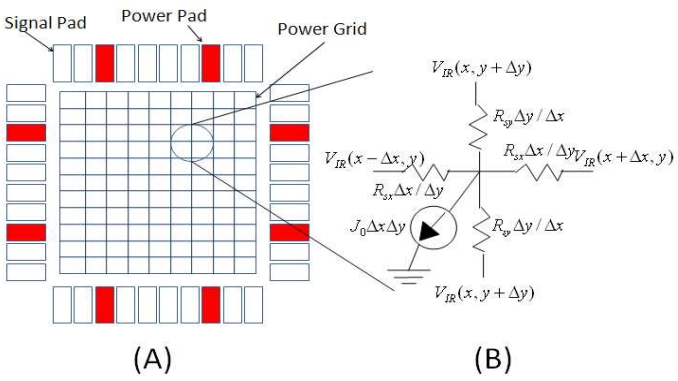


Fig. 4. The analysis model of IR-drop. (A) I/O Pad locations and the power distribution grid of the chip. (B) A node model in the grid. Using this model and EQ(1), we can compute the voltage drop in the chip.

### C. The Impact of Finger/Pad Locations on IR-Drop Violation

IR-drop is the unavoidable waste of electric charge when the circuit obtains energy from power pads. Compare wire-bond package with flip-chip package, the IR-drop problem of the wire-bond package is worse than the flip-chip package. The main reason is that the distance from the power pad to the module in the flip-chip package is short than the wire-bond package. However, as we move into nanometer regime, the resistance of the connection wire would consume the supply energy. If the power pad cannot supply enough energy, the voltage drop might exceed the lower boundary constraint. In this paper, we would modify the location of each power pad to improve the resistance of the connection wire. Further, IR-drop can be improved.

To improve IR-drop of the core, we need a good and efficient model for IR-drop analysis. It is usually used after floorplanning and placement [18][17], and the results are shown to be close to the results from SPICE simulation. On the other hand, [12] proposed an analytical model before floorplanning. Since finger/pad assignment problem is resolved before floorplanning, we adopt the model in [12] to obtain the IR-drop map. Since this model should be used before the planning of the core, it is not very accurate. The power grid model in [12] is shown in Fig. 4. The authors assume that the power consumption of all grids are the same, and propose the following equation to calculate IR-drop of each point.

$$\frac{V_{IR}(x,y)-V_{IR}(x+\triangle x,y)}{R_{sx}\frac{\triangle x}{\triangle y}}+ \frac{V_{IR}(x,y)-V_{IR}(x,y+\triangle y)}{R_{sy}\frac{\triangle y}{\triangle x}}+$$

### D. Problem Formulation

We have detailed the relations between the wire congestion, IR-drop and the finger/pad location. In modern chips, finger/pad counts are continuously increased and supply voltages are continuously decreased. Issues of the wire congestion and IR-drop are becoming more and more serious. The goal of this work is to plan nets on regular finger/pad locations to improve the density and IR-drop. In other words, we decrease the density and voltage drop of the core by relocating finger/pads. The problem can be formulated as follows:

**Input:** The locations of fingers/pads, $F_1, F_2, ..., F_x$, the set of the net name, $N_1, N_2, ..., N_x$ and the type of each net, the locations of bump ball, $B_{1,1,1}, B_{2,1,2}, ..., B_{y,i,j}$, where $i, j$ denotes the coordinate of the bump ball, and $y$ denotes the net name.

**Output:** The assignment of net $N_i$ to finger/pad locations $F_j, 1 \leq i, j \leq x$.

**Objective:** Minimize the maximum density and the voltage drop of the core based on pre-floorplan model.

## III. Congestion-driven Finger/Pad Assignment with Minimal IR-Drop

To solve the density and IR-drop problems, we propose a two-step methodology at the finger/pad planning level, as Fig. 1(C) illustrates. We first propose two congestion-driven finger/pad assignment methods to optimize the package density; the idea is to calculate the optimal density and compute the optimal finger/pad order and locations. We then present a finger/pad exchanging approach to reducing the IR-drop. The exchange approach will simultaneously consider the density and IR-drop.

### A. Congestion-driven Finger/Pad Assignment

The monotonic routing is a method in the package design which guarantees the high-quality routing result. This paper adopts this routing principle to verify the effect of the assignment method. According to the monotonic characteristic, [7] proposed a via assignment rule. For each finger $F_n$, the target bump ball is $B_{n,x,y}$, the net name is $N_n$, and the connected via is $V_n$. The coordinate of $V_n$ is $(V_{n,x}, V_{n,y})$. We randomly choose two nets $N_i$ and $N_j$, finger/pad locations are $F_i$ and $F_j$ and via location are $(V_{i,x}, V_{i,y})$ and $(V_{j,x}, V_{j,y})$. If $V_{i,x} < V_{j,x}$ and $V_{i,y} = V_{j,y}$, $i$ is certainly smaller than $j$. In other words, the via order and the displayed sequence in finger order are the same. An example can help to explain the rule. In Fig. 3(A), the finger locations from the left to the right are $F_1, F_2, ...F_{12}$, the finger order is $\_, 11, \_, \_, 6, \_, \_, 9, \_, \_, \_, \_$. The via order in $y = 2$ is $11, 6, 9$. If the via order conforms this rule, a legal monotonic routing certainly exists in this package. In this paper, we assume that the connected via is fixed at the left-down corner of the bump ball and use [7] method to be the package routing show the effectiveness of the finger/pad assignment. To minimize the maximum density, a better finger/pad assignment method is needed. Here we propose two congestion-driven finger/pad assignment approaches: Intuitive-Insertion-Based Finger/Pad Assignment and Minimal-Density-Based Finger/Pad Assignment.

*1) Intuitive-Insertion-Based Finger/Pad Assignment (IFA):* This method utilizes an inserted method to avoid the illegal monotonic rule. In the IFA method, we first decide a processing priority according to the coordinate of all horizontal lines. For each horizontal line, we must calculate the number of bump balls. For the first horizontal line (y=n, n is the highest horizontal line), the net name $N_x$ of each bump ball $B_x$ directly assigns to $F_x$. For other horizontal lines (y=n-1 to 0), the net name of the first bump ball $B_{i,1,y}$ assigns into $F_1$ and the net name of bump balls ($x = 2$ to $m - 1$) is assigned at $F_{b-1}$, where $F_b$ denotes the $(x-1)_{th}$ bump ball location in the $(y-1)_{th}$ horizontal line. The net name of the final bump ball in this horizontal line is directly inserted into the final finger location. We repeat this step until the priority order are executed to the end. The time complexity for IFA is $O(n^2)$.

Fig. 5 shows the illustration of an example and also the effectiveness of IFA. Bump balls and nets in this example are the same with Fig. 3. The illustration of IFA is shown in Fig. 5(A) and the routing result is shown in Fig. 5(B). In Fig. 5(A), because nets 11, 6 and 9 are set at the highest horizontal line(y=2), step 1 is to assign these three nets into finger locations $F_1, F_2$ and $F_3$. Step 2 is to insert nets 1, 3, 5 and 8(y=1) into suitable locations. Net 1 is set at $B_{i,\mathbf{1},y}$, we assign net 1 into $F_1$ and original locations $F_n$ of $N_n$ are moving to $F_{n+1}$. For net 3, the bump ball location is $B_{3,2,1}$. The net name on $B_{i,2,1+1}$ is "Net 6". Therefore, net 3 is inserted before net 6. Net 5 uses the same method to obtain the suitable location. Net 8 is inserted into the last location because it is the last net on this line. Step 3 is to repeat step 2 to insert remainder nets. The final finger order is $10, 1, 11, 2, 3, 6, 4, 5, 9, 7, 8, 0$. The routing result is shown in Fig. 5(B) and the density is 2.

*2) Minimal-Density-Based Finger/Pad Assignment (MFA):* If IFA is applied on the two-level BGA package, the routing result is very good. If IFA is applied on the three- or more-level BGA package, the result is imperfect because the insertion method of IFA only considered two horizontal lines. We propose another method, Minimal-density-based Finger/pad Assignment (MFA), to solve this problem. This method would considers the whole bump ball locations when the nets seek the optimal finger/pad location. The pseudo code is shown in Fig. 6. We first decide a processing priority according to the coordinate of all horizontal lines(line 1). For each horizontal line, we calculate the number of bump balls (line 2). Then, the optimal interval(OI) is computed (line 3), where

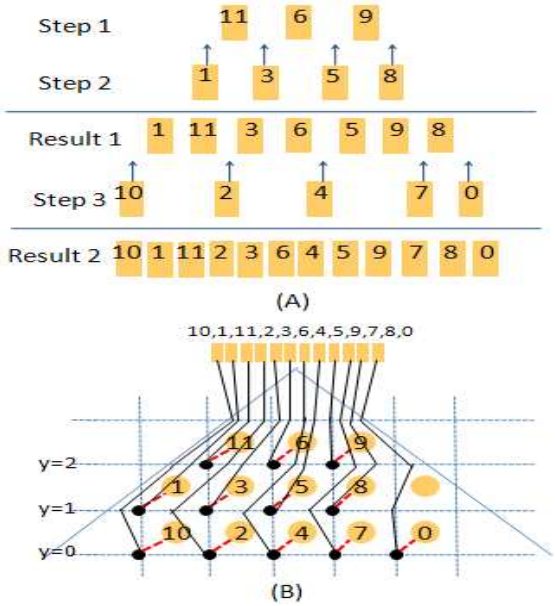


Fig. 5. The IFA assignment result is shown in (A), the routing result is shown in (B). The maximum density in the routing result is 2. Compare this result with Fig. 3(A), the maximum density decreases 50%.

"Total Non-assign Net" denotes the number of nets not connecting to the via, "Total Via Number" denotes the number of the via on the horizontal line, "Used Via Number" denotes the used via on the horizontal line. "(Total Via Number + 1)" denotes the segment in this horizontal line. For each bump ball ($B_{i,x,y}, 1 \le x \le m$), we calculate the empty number (EN) and insert net name into the (EN + 1)$_{th}$ location(lines 4-7), where EN denotes the empty slot in the finger location. The time complexity for MFA is $O(n)$.

Minimal-Density-Based Finger/Pad Assignment

1. **For** each horizontal line (y=n , y-- )
2. m = bump ball number in this horizontal line
3. compute the optimal interval :

$$OI = \frac{\text{Total Non-allocated Net} - \text{Used Via Number}}{\text{Total Via Number} + 1}$$

4. **For** (x=1 to m)
5. compute the empty number : EN = $\lfloor x * OI \rfloor$
6. net name on $B_{i,x,y}$ assigns into the (EN+1)th space
7. **End For**
8. **End For**

Fig. 6. The pseudo code of the Minimal-Density-Base Finger/Pad Assignment(MFA) method. This method can be applied on the multi-layer BGA package and the time complexity is $O(n)$.

We use the same example to show the effectiveness of MFA. The illustration of IFA is shown in Fig. 7. Because nets 11, 6 and 9 are set at the highest horizontal line(y=2), the finger location of these three net should be decided. According to the input information, the bump ball of these three nets are $B_{11,1,2}$, $B_{6,2,2}$ and $B_{9,3,2}$, Total Non-assign Net is 12, Total Via Number is 4 and Used Via Number is 3. $OI = (12-3)/(4+1) = 1.8$. For net 11, $EN = \lfloor 1*1.8 \rfloor = 1$. Therefore, net 11 is inserted into $F_2$ because $F_1$ is a empty slot. For net 6, $EN = \lfloor 2 * 1.8 \rfloor = 3$. Because $F_2$ is occupied, $F_1, F_3, F_4$

are empty space, net 6 is inserted into $F_5$. Using the same method, all nets can be inserted into the suitable location. The final order of fingers is $10, 11, 1, 2, 6, 3, 4, 9, 5, 7, 8, 0$, as shown in Fig. 7(C) and the routing result is shown in Fig. 3(B).

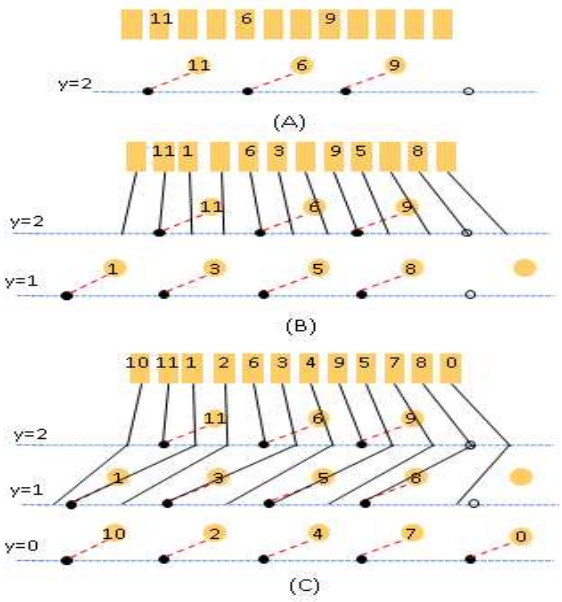


Fig. 7. The illustration of the Minimal-Density-Based Finger/Pad Assignment method. For each horizontal line, the net names are averagely assigned into the finger/pad location, the routing path of all nets can be averagely planed into the whole substrate.

### B. Finger/Pad Exchange for IR-Drop Improvement

After obtaining one initial net order for finger/pad locations, this order can be further exchanged to improve IR-drop of the core because IR-drop is ignored at the previous step. In this paper, we use EQ(1) to calculate IR-drop. If the location of the power pad is exchanged, IR-drop would be changed because $\triangle x$ and $\triangle y$ are changed. If we purely utilize EQ(1) to exchange finger/pad locations, the IR-drop issue can be solved. This method would cause the high-density routing in package design because the package problem is ignored in EQ(1). Here we propose a method to improve IR-drop and suppress the density simultaneously.

In Section III.A, the monotonic order has been introduced. If this principle is ignored in our exchange method, the monotonic routing not exist in the chip package. Therefore, we specify a range constraint when the finger/pads are exchanged. For each finger $F_n$, the target bump ball is $B_{n,x,y}$ and the net name is $N_n$. We randomly choose two nets $N_i$ and $N_j$, the connected bump balls are $B_{i,xi,yi}$, $B_{j,xj,yj}$ and finger/pad locations are $F_i$ and $F_j$. If $xi < xj$ and $yi = yj$, $F_i$ is certainly showed on $F_j$ left. We use an example to explain how we formulate the constraint. In Fig. 3(B), net 6 is assigned at $F_5$, the exchange range of net 6 is between $F_3$ and $F_7$. If the exchange range is without the limit, we must spend higher cost to find a suitable connected via to build the monotonic routing. When nets are exchange, an estimative method of package density is needed. A simple and effective method to estimate the density when the finger/pad are exchanging is proposed. Because the monotonic routing is used in the chip package, the density of the high horizontal line is higher than the density of the low horizontal line. Therefore, we only oversee the density in the highest horizontal line. In IFA and MFA methods, the initial order of $N_n$ on finger/pad location, $F_n$ is decided. If $B_{i,x,y}$ is planned at the highest horizontal line, the connected finger/pad $F_i$, should be recorded. If the recorded number is $x$, the net order could be divided into $x+1$ sections. For each section, we should record the interval number $I_j^{ini}, 1 \leq j \leq x+1$. When nets are exchanged, the interval number would be changed. These numbers are called $I_j^{new}, 1 \leq j \leq x+1$. Therefore, the increased density ($ID$) can be computed as following:

$$ID = max(I_j^{new} - I_j^{ini}), 1 \leq j \leq x+1 \quad (2)$$

The cost function in our exchange method is shown as follow :

$$Cost = \alpha \cdot V_{IR} + \beta \cdot ID \quad (3)$$

where $V_{IR}$ denotes the voltage drop of the core, $\alpha$ and $\beta$ denote the weight in our cost function. We use EQ(1) to compute $V_{IR}$. According to the cost function and exchange constraint, we integrate these constraints into the SA (Simulated Annealing) [5] algorithm to minimize IR-drop and the maximum density. In the SA algorithm, we randomly choose one power net to exchanging and use EQ(3) to compute the exchange cost. If the new cost is small than the previous cost, the exchange result is accepted. If the new cost is larger than the previous cost, we randomly decide that the original net order must be replaced by the new net order.

TABLE I
THIS SHOWS THE MAXIMUM DENSITY IN OUT TEST CIRCUITS. THE MFA METHOD SHOWS THE BEST RESULT. COMPARE MFA WITH THE RANDOM METHOD, THE MAXIMUM DENSITY DECREASES 68%.

| Input | Finger/Pad Counts | Level | Max Density | | |
|---|---|---|---|---|---|
| | | | Random | IFA | MFA |
| Circuit1 | 96 | 4 | 11 | 8 | 6 |
| Circuit2 | 160 | 4 | 12 | 8 | 5 |
| Circuit3 | 208 | 4 | 13 | 8 | 4 |
| Circuit4 | 348 | 3 | 11 | 4 | 3 |
| Circuit5 | 352 | 4 | 15 | 8 | 4 |
| Circuit6 | 380 | 5 | 17 | 12 | 5 |
| Circuit7 | 448 | 4 | 17 | 8 | 4 |
| Average Ratio of Maximum Density | | | 1 | 0.58 | 0.32 |

## IV. EXPERIMENTAL RESULTS

This paper implements IFA, MFA, and the IR-drop driven finger/pad exchanging with minimal density approach using C++ language on an AMD 3200 computer with 1G memory. Seven simplified industrial circuits are used to test the performance of proposed methodology.

Table I shows the maximum density after the package routing. In the third column, Level denote the number of the horizontal(vertical) line in the bottom(left) and top(right) part in of package architecture. The random method denotes that the assignment order conforms the monotonic rule and other factors are ignored. In the last row, we compare the average ratio of the maximum density. We set the average density of the random method is 100%. The average density of IFA is 58% and MFA is 32%. Compare the random method with MFA, the average density improves 68%. The extended area of substrate and the total wire length can be greatly improved when we use a detailed routing method to finish the package design.

After MFA, initial finger/pad locations can be obtained. We then use the proposed finger/pad exchange method to improve IR-drop. The result is shown in Table II. Though the density is increased,

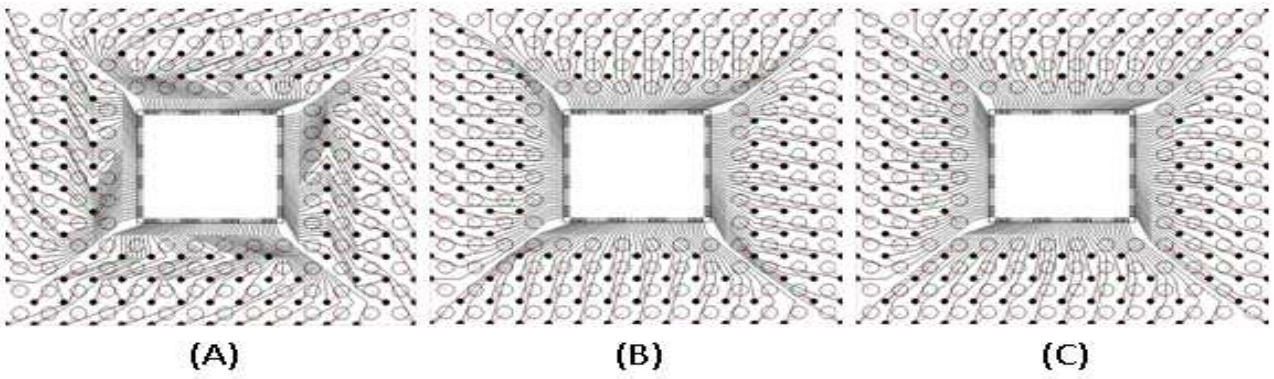


Fig. 8. The routing results of Circuit 2. We use the same routing algorithm to realize the package routing. (A)The random assignment result. (B)The IFA result. (C)The MFA result. The maximum density of MFA is smaller than others.

TABLE II
THIS TABLE SHOWS THAT THE IMPROVED RATIO OF IR-DROP. WE COMPARE FIVE TEST CIRCUITS. THE LEVEL NUMBERS IN THESE TEST CIRCUITS ARE 4. OUR METHOD IMPROVE 10.61% OF IR-DROP IN AVERAGE FOR TEST CIRCUITS.

| Input | Max Density | | IR-Drop Improved Ratio(%) |
|---|---|---|---|
| | After MFA | After Exchanging | |
| Circuit1 | 6 | 8 | 27.36 |
| Circuit2 | 5 | 8 | 9.43 |
| Circuit3 | 4 | 7 | 5.89 |
| Circuit5 | 4 | 7 | 6.92 |
| Circuit7 | 4 | 7 | 3.45 |
| Average Improvement of IR-Drop | | | 10.61 |

the maximum density is better than IFA and the IR-drop improves 10.61% in average for test circuits.

## V. CONCLUSION AND FUTURE WORK

Chip-package codesign is very important due to the demand of the increasing complexity of the designs. In this work we have proposed techniques to allocate finger/pads for package routability and core signal integrity concerns, which are primary key metrics in system design. Experimental results have shown the effectiveness of our approaches.

In the modern chip design, stacking ICs are frequently used to increased performances and functions. In [9], the authors proposed an I/O planning method to plan the tier location for all I/O Pad. Therefore, a parallel process of stacking IC and package problems will be explored to further improve the cycle time of the chip design and increase the yield of stacking ICs.

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