

Contactless Testing: Possibility or Pipe-Dream?

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Abstract

The traditionally wired interfaces of many electronic systems are in many applications being replaced by wireless interfaces. Testing of electronic systems (both integrated circuits and printed circuit boards) still requires physical electrical contact through probe needles and/or sockets. This paper addresses the state-of-the-art, options, and hurdles-still-to-take of contactless testing, which would resolve many test challenges due to shrinking size and pitch of pads and pins and inaccessibility of advanced assembly techniques as System-in-Package (SiP) and 3D stacked ICs.

1 Wireless Testing of Integrated Circuits

Dae Young Lee and John P. Hayes – University of Michigan

Direct-contact probing is the standard way to test integrated circuit (IC) wafers via automatic test equipment (ATE). However, it entails high cost due to contact-point deformation and the need for repeated cleaning of probe needles. Wireless testing aims to replace probe needles with contactless circuits that link the wafer and ATE. The potential technologies for wireless testing include radio-frequency (RF), near-field, and optical communication. We review these technologies and present the results of some simulation experiments to assess their efficiency and practicality.

1.1 Introduction

IC technology roughly doubles transistor density every two years, causing a steady increase in testing difficulty [1]. Wafer probing reduces overall testing costs by identifying known good dies prior to packaging. However, the frequent physical contacts (by means of touch-downs) between the ATE's probe needles and the wafer-under-test have some serious drawbacks. The probe needles and contact points suffer deformation, and debris accumulates that can affect test results. The debris can be removed by abrasive cleaning, but that can damage the probe needles [2]. In addition, the increasing use of components with multiple chips, such as 3D IC stacks employing through silicon via (TSV) technology, makes direct-contact probing extremely difficult. TSV tips are too fragile to be probed and conventional probe cards do not support variable contact-point locations.

The limitations of direct-contact testing mainly derive from physical contact between the wafer and the ATE's probe needles. If we could replace this by wireless communication, the foregoing problems could be largely eliminated, and testing of TSV-based 3D ICs could be simplified. Wireless testing has some basic requirements of its own, however, including low power and small circuit size. To completely eliminate physical contact between a probe card and the device under test,

power should be delivered by wireless technology or be generated on the wafer. The antennas and two-way communication circuits should not consume too much chip area nor affect the functionality of the original device. Therefore the power and size of the added components are severely restricted. The corresponding items on the ATE are much less restricted.

Wireless testing has been proposed before [3, 4], but little data has been published concerning the foregoing technology issues. However, useful insights can be gained from other communication problems that are similar to wireless testing in terms of range, power consumption, and circuit size constraints. One of these is wireless chip-to-chip communication for 3D wafer integration [5–9].

1.2 Wireless Technologies

We briefly consider three communication methods as potentially suitable for wireless wafer-level testing of ICs: radio frequency (RF), near field, and optical.

RF is found today in many forms of wireless communication. Since it requires placing large numbers of RF transmitters and receivers on the individual dies of a wafer, the size of these circuits and their antennas is of utmost importance. Modulation is needed to avoid interchannel interference. RF can provide long communication range, but the associated size overhead, including antenna and circuits, is considerable [10].

Unlike RF, near-field communication does not use wave propagation. Instead, it transfers energy through a quasi-static electromagnetic field. This enables the communication circuits to consume very low power, and eliminates wave propagation effects like fading, reflection and phase shifting. If the distance between the transceivers is very short, near-field may be more efficient than RF communication.

Optical signals consist of high-frequency electro-magnetic fields and are relatively immune to interference. They can therefore be detected without complex modulation and amplifier circuits. However, owing to difficulty and high cost of integrating them with conventional CMOS processes, optical communication seems unsuitable for wireless wafer-level testing [11].

1.3 Near-Field vs. RF

RF and near-field communication may seem to be distinct technologies, but both stem from the same fundamental electromagnetic effects. Whether to use near-field analysis or not depends on the distance from the radiation source and the carrier frequency used. At a fixed frequency f , most of the energy radiates through a quasi-static field near the source. Wave propagation is the major means of energy transfer in the far-field zone.

The general solutions of Maxwell's equations for a field at distance (range) R from the source contain terms of the form $1/R$, $1/R^2$ and $1/R^3$. Among these, $1/R$ corresponds to electromagnetic wave propagation, and $1/R^3$ is related to the quasi-static condition. Which term is dominant depends on R and f . When R is small, the quasi-static terms dominate, and we have the so-called *near-field* case where the coupling between the source and destination antennas is defined by mutual inductance or capacitance according to standard circuit theory. Further from the source, the propagation term becomes dominant and we have the *far-field* case associated with the propagating waves of RF theory; see Figure 1.

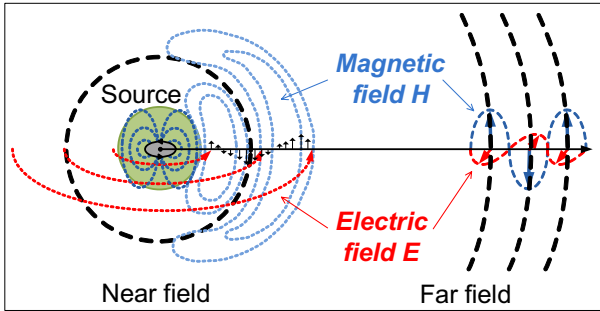


Figure 1: Near and far fields around an RF source.

The two wireless communication technologies require quite different antenna designs. Generally, RF antennas are linear in shape with a length proportional to the wavelength of the RF carrier. Capacitors and inductors are used as near-field antennas and are often called sensors or transducers.

Conventional ATE performs touch-downs on the target wafer with an accuracy measured in micrometers. Hence the range R needed for wireless testing is necessarily very small, implying that near-field communication is more suitable than RF, and the antenna should be some kind of inductive or capacitive transducer rather than a conventional RF antenna.

RF communication may be considered for longer communication range, which provides more freedom in designing wireless probe cards. However, for efficient RF communication, even a carrier frequency of tens of gigahertz necessitates millimeter-sized antennas which are too large to be used for wireless wafer-level testing. On the other hand, RF

can be used for characterizing an entire wafer, operations which require longer range but are less area-constrained than wafer-level testing.

1.4 Inductive vs. Capacitive

As noted above, two main near-field phenomena are available for testing purposes: inductive and capacitive coupling. Inductive coupling has several advantages, even though the design and characterization of on-chip inductors is complicated [8]. First, it is driven by current change, which is not limited by supply voltage and is easily provided by current-generating circuits. Second, almost no high permeability material is used in conventional CMOS processes, so only relatively insignificant eddy currents generated by high-conductivity material affect the coupling magnetic field. Third, inductive coupling provides more options for design. Since in both cases, gain is proportional to the area of the transducers, dimensional miniaturization may not provide sufficient coupling. But inductive coupling has one more option, the number of turns, which can be increased without additional area consumption.

To compare inductive and capacitive coupling, on-chip capacitive and inductive transducers of the same size ($25 \mu\text{m} \times 25 \mu\text{m}$) were simulated using Ansoft's HFSS v10 simulation tool. The inductors have three turns per layer and two metal layers, while the capacitive transducer consists of two single-layer metal plates. Figure 2 demonstrates that the gain S_{21} (the ratio of output to input voltage with a 50Ω load) of inductive coupling at 4 GHz is much higher than that of capacitive coupling at the same range R . Hence, we conclude that inductive coupling can provide more efficient communication for wireless testing than capacitive coupling, mainly because of its larger number of design options.

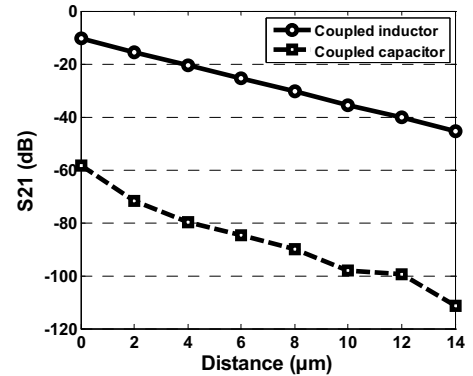


Figure 2: Simulated gain S_{21} as a function of distance R .

1.5 Performance Comparison

RF has been investigated for inter-chip communication and for wireless global clock distribution. The required antenna size tends to be much larger than the corresponding near-field antenna. Optical communication is not considered here due to its incompatibility with conventional CMOS processes.

Table 1 lists several implementations of near-field and RF communication for chip-to-chip communication and clock distribution. Far-field communication requires large and complex circuits and a large antenna [10]. Most capacitively-coupled chip-to-chip links consume less power, but the communication distance is much shorter than in

the inductive case [5, 6]. Taking into account the rapid drop of signal strength over the near field, the low power consumption achieved by capacitive coupling seems to result from the short communication distance. If we use the same range R with inductive coupling, the overall power consumption will be significantly lower than that of capacitive coupling. In addition, for flexibility in locating transceivers on probe cards, very short-range capacitive coupling seems unsuitable for wireless testing. One can form longer range communication channels via inductive coupling, while maintaining the same data rate and area overhead [7–9]. There are very few actual implementations of wireless

testing so far. We include [3] in Table 1 for comparison purposes.

1.6 Conclusion

We have sketched the main wireless technologies for chip testing, and analyzed their efficiency and practicality. Our simulation experiments, although limited in scope, support the theoretical analysis. Near-field communication via inductive coupling appears to be a promising technology for wireless testing. Besides low area and power consumption, it offers immunity to interference and good signal gain.

	Fazzi et al. [5]	Gu et al. [6]	Miura et al. [7]	Floyd et al. [10]	Sellathamby et al. [3]
Basic technology	Capacitive	Capacitive	Inductive	Far-field RF	Unknown
Modulation method	Pulse	Pulse	Pulse	15 GHz RF	916 MHz AM
Energy/bit	0.15 pJ/b	0.27 pJ/b	0.33 pJ/b	None	1 μ W (total)
Data rate	2.46 Gb/s/ch	10 Gb/s/ch	1 Gb/s/ch	None	1 Mb/s
Bit error rate	$<10^{12}$	$<10^{12}$	$<10^{12}$	None	Unknown
Process	0.13 μ m CMOS	0.18 μ m CMOS	0.18 μ m CMOS	0.18 μ m CMOS	CMOS
Range R	$<1 \mu$ m	3 μ m	15 μ m	5.6 μ m	200 μ m
Channel size	15 $\times$ 15 μ m ²	2 $\times$ 48 $\times$ 18 μ m ²	30 $\times$ 30 μ m ²	600 $\times$ 600 μ m ²	$>100 \mu$ m long

Table 1: Performance comparison of prior chip-level wireless communication systems.

2 A Complete Solution for Wireless IC Testing

Chris Sellathamby, Brian Moore, Steven Slupsky – Scanimetrics

The ever-increasing demand for smaller microchips and improved performance has led to a crisis in interconnectivity between chips, and has shifted the design, cost, performance and reliability focus to address chip-to-chip interconnect limitations. The International Technology Roadmap for Semiconductors (ITRS) predicts the interconnect crisis could emerge as soon as 2009 [1]. This is due to further chip miniaturization, which requires shrinking the interconnects in chip designs. However, simply decreasing the size of chip interconnects causes many problems related to testability, signal timing, and power consumption. This section describes unique solutions to major chip interconnect problems experienced by semiconductor manufacturers, including non-contact (touchless) chip-scale communications solutions. The work involves the creation of a complete solution that includes non-contact testing of semiconductor devices, which is a key part of any interconnect solution.

2.1 Background

As designs move to smaller nanometer processes, test development is becoming more difficult. Today’s nanometer-scale microchips call for extensive changes in all facets of the design flow. The need for advanced interconnects (the bond pads, wires, and protocols used to connect chips electronically) and packages (the carrier or container for a microchip) has become more critical. Chip designs are shrinking because of size and cost benefits, but the interconnects and probing requirements are causing chip interface bottlenecks.

The testing of semiconductors is a significant and growing problem in the very large scale integration (VLSI) circuit manufacturing industry. With growing complexity and density of devices per wafer area, the cost of testing a microchip is growing faster than the cost of manufacturing one [1]; and in some cases, the testing cost exceeds the manufacturing cost. Semiconductor testing has become a multi-billion dollar industry, leading to opportunities for the introduction of new test-

ing technologies, such as non-contact testing methodologies [12]. Issues such as testing with smaller pad size and increased pad density, increased signal input/output (I/O) frequencies, longer test times, mechanical reliability of low- k dielectric materials, and probe card contact and alignment are restricting the progress towards smaller, faster, and more economical integrated circuits [13]. All present state-of-the-art wafer probing techniques utilize probes which physically contact the device being tested and have limitations, such as the number of contacts, size of contacts, operating frequency, parallel testing capability, and risk of damage to the devices being tested [2].

In addition, many new technologies have emerged to address the high-speed, fine-pitch interconnect issues. These technologies include Through-Silicon Vias (TSVs), proximity interconnect based on capacitive coupling, and redistributed chip-scale packaging (RCP), but testing devices which use these technologies remains a challenge.

2.2 Non-Contact Testing – A Reality

Non-contact testing is neither a possibility nor a pipe dream – it is a reality. Non-contact testing alleviates many of the constraints of contact probing, allowing for significant improvements in the economics of integrated circuit manufacturing of the devices. In addition to the traditional testing performed after packaging, non-contact testing can also be implemented earlier in the manufacturing value chain, providing important feedback during the production process [14]. Non-contact testing, being a much faster process and capable of highly parallel testing, allows for increased test coverage on a larger population of devices, while maintaining throughput.

Data and test signals can be sent in a non-contact manner by having antennas and transceivers in both the DUT and the probe card. In order to achieve fully non-contact testing, power must also be transferred to the device under test (DUT) from the probe card by non-contact means. This is accomplished by transmitting radio frequency (RF) power from

the probe card through microfabricated antennas, receiving the power on the DUT through corresponding antennas, and converting the received RF energy to DC power. The amount of power that can be transferred from the probe to the DUT is limited by the size of the antenna and the number of antennas available for power transfer. For high-power devices, a hybrid approach is used in which power is connected using contact probes while data is transferred wirelessly.

Scanimetrics' patented interconnect and non-contact probing technology can be used to improve many aspects of chip design and fabrication, including fabrication process monitoring, chip testing, and chip cost. Higher integration is achieved through the use of the technology both to enable 3D packaging and to improve performance of smaller chips.

2.3 A Real Application

One example of a cost benefit on non-contact testing is to utilize Scanimetrics' solution to enable complex system-in-package (SiP) designs, which combine more than one chip in a single package. In order to improve yields and decrease time to market, Scanimetrics' Wireless Test Access Port (WiTAP) enables the SiP module to be tested during the assembly process. Each chip or DUT and the entire module can be tested cost-effectively using Scanimetrics' products during the manufacturing process. This same technology has been demonstrated for use in non-contact wafer probing as well. After testing, the chips within the SiP module are able to interconnect and communicate during normal operation using the same low power, high-speed wireless interconnect technology.

Scanimetrics' solution has been qualified on the production line of one of the top-ten semiconductor companies in the world. Figure 3 depicts the top view of a multi-site production hybrid probe card which uses cantilever contact probes for power and ground while all signal I/O is wireless. The probe card is designed for a production Electroglas 4090u prober and a Verigy 93000 tester. The probe card tests four SiP sites simultaneously (' $\times 4$ configuration'). Figure 4 illustrates the bottom view of the probing area, consisting of cantilever contact probes for power and the probe transceivers for signal I/O. Figure 5 shows the SiP wafer being probed.

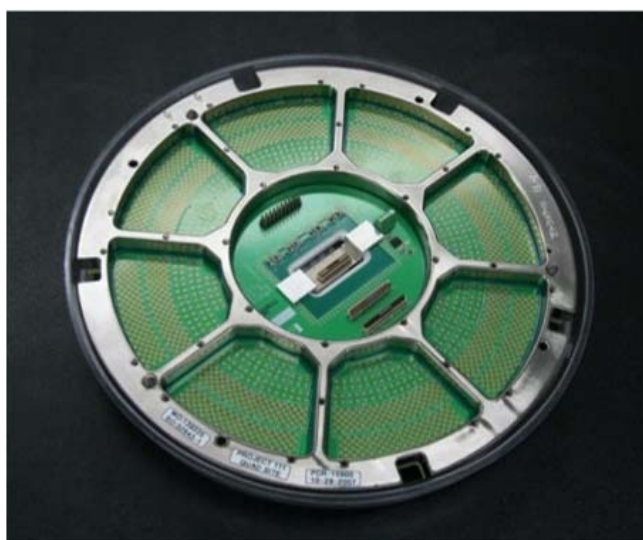


Figure 3: Top view of a Scanimetrics production probe card.

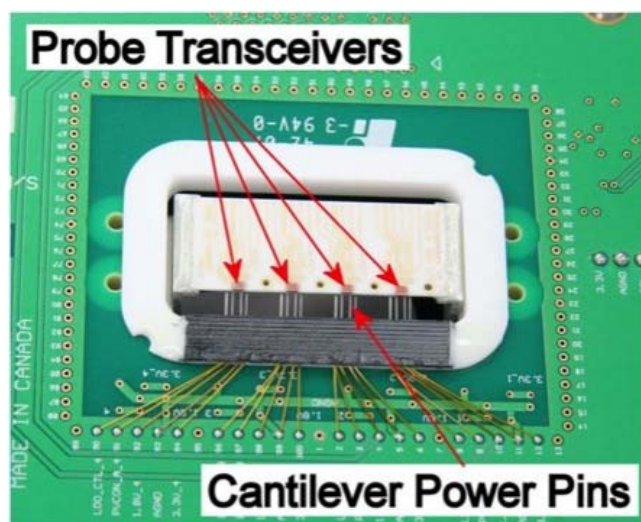


Figure 4: Bottom view of the probing area of the card.

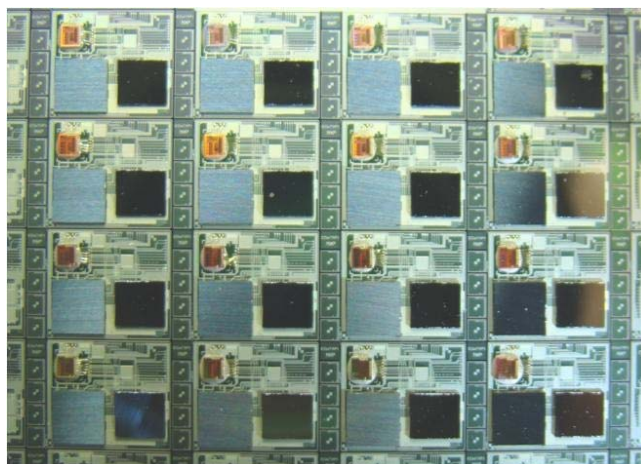


Figure 5: WiTAP chips on SiP modules.

2.4 Conclusion

Non-contact wafer-level probing of integrated circuits has been demonstrated in a production environment. While this technique has the potential to significantly improve test performance and reduce test costs, it requires that antennas and transceiver circuits be designed into the device being tested. This requirement places stringent restrictions on the design of these components in order to minimize impact on chip real estate and circuit performance. In addition, the wafer probing application requires high data rates and good signal integrity. Antennas and transceiver circuits have been designed that address these issues and permit non-contact testing of semiconductor wafers using wireless probes.

The same non-contact testing interface can be used for chip-to-chip interconnect, enabling higher speed communication with lower power consumption. In a complete implementation of this technology, I/O cell size can be reduced, resulting in an overall reduction of chip size.

3 Laser-Direct Testing of IC Package Substrates

Laurence Pujol – Beamind

In the field of PCB, the evolution in packaging technologies generated the development of new test methods able to deal with new technologies and respond to new needs: (1) very fine pitch, down to 20 μm pads, (2) high flexibility, i.e., no fixturing or specific tools any more, (3) full test coverage, and (4) no marking on the tested device.

3.1 Laser-Direct Technology

In 1905, Albert Einstein was awarded a Nobel prize for the theory of the photoelectric effect by which electrons can be extracted from a metal by photons provided their energy is high enough. Using today's technologies such as ultra-violet (UV) solid-state lasers (e.g., used for laser drilling) and ultra-sensitive analog electronics, it is possible to use the photoelectric effect to run electrical currents through the traces of an IC package substrate and thus measure opens and shorts in a non-contact way.

This technology has been developed by Beamind, a VC-funded company, in collaboration with the CEA/LETI, Grenoble, France, on the MINATEC site, one of the most advanced semiconductor technological platforms in Europe.

Measurement Configuration

In order to generate and collect photo-electrons coming from the trace, the LDT system includes the following.

- A deep-UV laser with a wavelength low enough to overcome the pad finishing material work function (surface finishings are mainly gold, tin-lead and lead-free alloys), focussed on a spot smaller than the pad. Two beams are generated from the laser in order to address both sides of the substrate.
- Two pairs of deflective mirrors, mounted onto galvanometers, allow the beams to point to the pad of the trace.
- A pair of semi-transparent collecting plates can be set to a potential V^+ attracting photoelectrons emitted by the trace.
- A proprietary electronic board to process the photo-electric signal coming from the collecting plates.
- A dedicated set of algorithms and software interpreting the measurement signal and delivering the final test diagnostic.

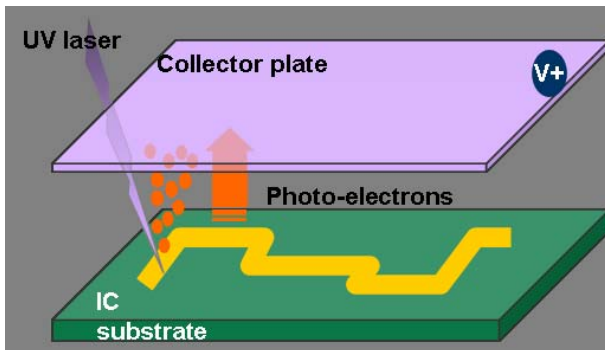


Figure 6: LDT measurement configuration.

LDT Measurement Basic Principles

As the collector plate is set to a voltage higher than the trace, an electri-

cal field is created between the substrate and the collector. This field is used to attract electrons removed from the trace by the photo-electrical effect. Photoelectrons trapped on the plate generate a charge converted to a signal by the electronic board connected to the plate. This signal indicates the charge collected $\sum Q$. As electrons (negative charges) are removed from the traces by the photoelectric effect, the potential of the trace increases to reach the potential collector inhibiting the electrical field between the trace and the collector plate. More laser shots on the trace will no longer extract photoelectrons from it and therefore generate a charge collected signal close to zero.

The number of shots required to cancel the electrical field depends upon the trace capacitance according to following equation: $\sum Q = C \cdot V$ with Q the electrical charge removed from the trace (linked to the number of laser shots), C the capacitance of the trace versus collector plate, and V the starting potential difference between trace and collector.

Measuring the electrical charge extracted from the trace and the voltage gap is similar to checking the capacitance of the trace. Each substrate has thousands of traces with their own capacitance with respect to the collector plate. A learning phase is then used to log the capacitance signatures of all the traces into a software database ($\sum Q_{\text{ref}}$). This learning phase is done at the very beginning of a test campaign of a new batch of substrates. It uses the first units to fill the reference database. The capacitance signature from each substrate tested is then compared to this reference database.

Measurement of Short Defects

Two traces are shorted if they are electrically connected while they should be isolated from each other (see Figure 7). Trace #1 is charged through one of its test points ($tp1$), up to the potential V^+ of the collector plate. If traces #1 and #2 are connected to each other, then the collected charges value $\sum Q$ is higher than $\sum Q_{\text{ref}}$, as the charged capacitance is the sum of the capacitance of traces #1 and #2. $\sum Q$ measured during the charge of trace #1 exceeds a pre-determined short threshold for trace #1.

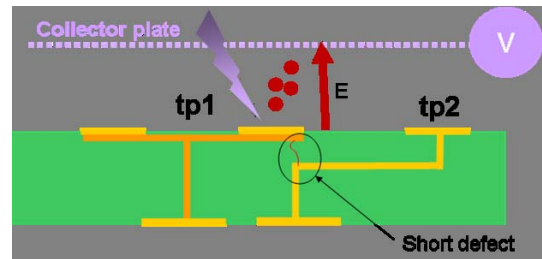


Figure 7: Short detection principle.

Measurement of Open Defects

A trace is open if no electrical connection exists between two pads of a same trace. There is no electrical continuity between $tp1$ and $tp2$ as shown in Figure 8(a). In Phase 1, test point $tp1$ is charged up to the potential V of the collector plate. Then the laser beam is moved to test point $tp2$ and shoots on the pad (see Figure 8(b)). If photoelectrons are extracted generating a charge collected signal, it means that an electric field remains between $tp2$ and the collector. The pad has therefore not

been charged to the potential V during Phase 1. A non-zero signal denotes that there is no electrical connection between $tp1$ and $tp2$: the trace is open.

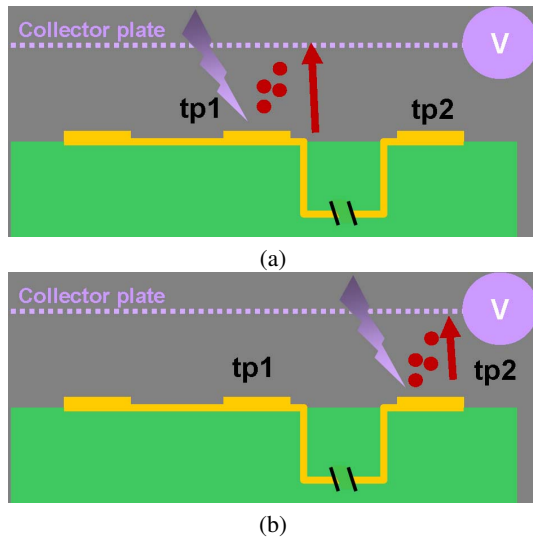


Figure 8: Open detection principle.

3.2 Key Benefits of LDT Technology

The LDT is a disruptive technology for electrical testing on many points. The measurement is entirely contactless: UV laser energy is optimized to perform electron extraction with no ablation, leaving no mark onto the test pad.

LDT can focus on very small spots, leading to a very good ability to test very fine pitch patterns. Today, the UV laser beam size is smaller than $60\text{ }\mu\text{m}$ and could be reduced further down to a few microns.

Laser movements are controlled by scanning mirrors that are ten times faster than the mechanical probes used by flying prober technology.

The testing speed and test *productivity* can then be increased up to 150 TPS (Test Points per Second).

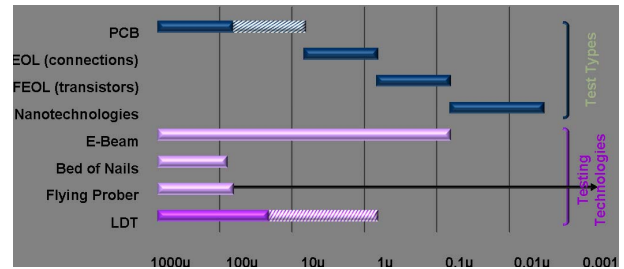


Figure 9: Required pattern sizes.

The position of the laser beam is fully programmable; no fixtures are required as in the beds of nails technology. That *flexibility* greatly reduces the total cost of ownership and line-setup time and is very useful for testing small to medium series.

The benefit of this contactless technology is not limited to the field of PCBs. Due to LDT's technological advantages, it can be very useful in the silicon field. The fine pitch capacitance measurement can be used to test TSVs (Through-Silicon Vias) or redistribution interconnection layers, for instance.

Foreseeing the evolution of 3D stacking of IC components and challenges expected to test complex packages, LDT technology will become an inevitable key technology in advanced IC manufacturing.

3.3 Conclusion

Like laser drilling and Laser-Direct Imaging, electrical test of IC package substrates are now benefiting from laser-based technology. Laser-Direct Testing spreads laser properties in electrical test, providing contactless, fine-pitch testability and improving productivity. Suitable for the last generation of high-density PCB substrates, it is slowly merging into the 3D stacked IC packaging market place.

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