

Imperfection-Immune VLSI Logic Circuits using Carbon Nanotube Field Effect Transistors

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Abstract

Carbon Nanotube Field-Effect Transistors (CNFETs) show big promise as extensions to silicon-CMOS because: 1) Ideal CNFETs can provide significant energy and performance benefits over silicon-CMOS, and 2) CNFET processing is compatible with existing silicon-CMOS processing. However, future gigascale systems cannot rely solely on existing chemical synthesis for guaranteed ideal devices. VLSI-scale logic circuits using CNFETs must overcome major challenges posed by: 1) Misaligned and mispositioned Carbon Nanotubes (CNTs); 2) Metallic CNTs; and, 3) CNT density variations. This paper performs detailed analysis of the impact of these challenges on CNFET circuit performance. A combination of design and processing techniques, presented in this paper, can enable VLSI-scale CNFET logic circuits that are immune to high rates of inherent imperfections. These techniques are inexpensive compared to traditional defect- and fault-tolerance, do not impose major changes in VLSI design flows, and are compatible with VLSI processing because they do not require special customization on chip-by-chip basis.

1. Introduction

Carbon Nanotube Field Effect Transistors (CNFETs) are promising candidates as extensions to silicon-CMOS due to fine pitch and excellent device characteristics. Figure 1.1 shows the side view of a CNFET. Parallel semiconducting Carbon Nanotubes (CNTs) are grown on or transferred to a substrate. The regions of CNTs under the gate are undoped. The conductivity of these undoped regions is controlled by the gate. The source and drain regions of the CNTs are heavily doped. The gate, source and drain contacts, and interconnects are defined by conventional lithography. With this structure, a large portion of existing design and manufacturing infrastructure for FET-based VLSI systems can be utilized.

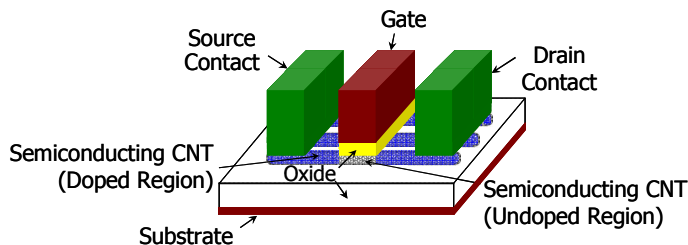
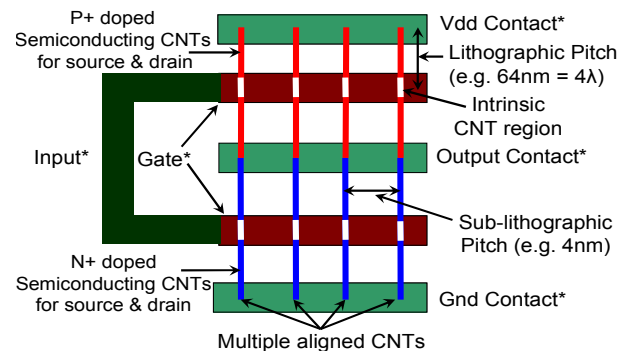


Figure 1.1. Carbon-Nanotube Field-Effect-Transistor (CNFET).

Figure 1.2 shows the schematic of a CNFET inverter. The inverter consists of contacts, p+ doped source and drain regions of semiconducting CNTs for the pull-up PFET network, n+ doped source and drain regions of semiconducting CNTs for the pull-down NFET network, two gates for the pull-up and pull-down networks, undoped or intrinsic regions of CNTs under the gates, and local interconnects connecting the gates. The distances between gates and contacts are limited by the lithographic feature size (lithographic pitch in Fig. 1.2, e.g., 64 nm for the 32 nm

technology node). Since CNTs are grown on the substrate, the inter-CNT distance (sub-lithographic pitch in Fig. 1.2) is not limited by lithography.

Simulation results show that an “ideal” CNFET inverter using a perfect CNFET technology can be 5.1 times faster, and can consume 2.6 times lower energy per cycle (i.e., 13X Energy-Delay-Product benefit) compared to a 32 nm silicon-CMOS inverter [Deng 07, Patil 09]. These improvements over silicon-CMOS are due to near ballistic electrical transport in CNTs. Furthermore, several new applications including large-area electronics may be enabled by such devices [Cao 08].



* Lithographically defined gate, contacts and interconnect

Figure 1.2. CNFET inverter.

There has been significant progress in recent years at the single-CNFET-device level. However, a major gap exists between such single-device-level results, and the transformation of these materials revolutions into practical design technologies for gigascale digital integrated circuits (ICs) that are competitive with silicon-CMOS at the end of device scaling. For practical VLSI designs using CNFETs, the following fundamental barriers must be overcome:

1) Misaligned and mis-positioned CNTs: It is nearly impossible to guarantee perfect alignment and accurate positioning of all CNTs at VLSI scale. Mis-positioned and misaligned CNTs can result in incorrect digital logic functionality.

2) Metallic CNTs in CNFETs: CNTs can be either metallic (m-CNT) or semiconducting (s-CNT) depending on their chiralities [Saito 98]. m-CNTs have zero bandgap and, hence, their conductivity cannot be controlled by the gate. The existence of m-CNTs inside CNFET transistors creates source-to-drain shorts. For random CNT growth, about 1/3 of the CNTs are metallic [Saito 98]. There are no known CNT synthesis techniques that grow exclusively s-CNTs.

3) Complementary Device integration with high CNT density: High CNT density (e.g., 250 CNTs/μm) is needed for CNFET current densities to be comparable to CMOS [Deng 07, Patil 09]. Current state-of-the-art CNT density is 10 CNTs/μm [Kang 07]. Chemical doping of CNTs to achieve high performance MOSFET-like CNFETs, along with the integration of n-type and p-type CNFETs on the same substrate, is also an important processing challenge.

In spite of several unanswered questions about CNFETs, three major trends are clear:

1) Future gigascale systems cannot rely solely on current chemical synthesis for guaranteed perfect devices. As discussed before, misaligned and mis-positioned CNTs can result in incorrect logic functionality. Similarly, no known CNT growth technique guarantees 0% m-CNTs. m-CNTs create source-drain shorts resulting in excessive leakage, severely degraded noise margins, and delay variations.

2) Expensive defect- and fault-tolerance techniques will not enable wide adoption of CNFET-based circuits. In fact, expensive techniques will create major roadblocks to the adoption of CNFET technologies.

3) New design techniques must be compatible with VLSI processing and have minimal impact on existing VLSI design flows. Investments made in VLSI design infrastructure are too large to be ignored. For example, techniques that rely on separate customization of every chip can be prohibitively expensive if not designed carefully.

An **imperfection-immune design paradigm** is required to overcome these barriers. In this paper, we present an overview of such techniques that we recently developed. In Sec. 2, we present a technique for designing CNFET logic circuits that implement correct logic functions even in the presence of a large number of mis-positioned and misaligned CNTs [Patil 07, 08b]. In Sec. 3, we present design and processing guidelines for metallic-CNT-tolerant CNFET circuits, based on practical constraints on leakage, noise margin and delay variations [Zhang 08]. Section 4 presents a simple model to characterize CNT density variations. Using this model, the impact of CNT density variations on performance variations of CNFET circuits is analyzed. Section 5 concludes this paper.

2. Misaligned- and Mis-Positioned CNT-Immune Design

In an ideal CNFET, all CNTs should grow on the substrate in one direction from one contact to another, passing under the gate region. However, in reality, not all CNTs are perfectly aligned and positioned. Figure 2.1 shows an SEM image of CNTs on quartz that we have grown in our laboratory. Even though a large fraction (~99%) of CNTs grow aligned to the crystal orientation of the single crystal quartz substrate (Fig. 2.1), a non-negligible (~1%) fraction of CNTs are misaligned [Kang 07, Patil 08a]. Even if all the CNTs are aligned, some CNTs may be mis-positioned and may lie outside the gate region. It is nearly impossible to guarantee perfect alignment and positioning of all CNTs at VLSI scale. This can result in incorrect logic behaviors of fabricated logic structures (Fig. 2.2). Figure 2.1 shows a possible CNFET NAND cell layout overlaid on an SEM image of directional CNTs grown on quartz. The mis-positioned CNT in Fig. 2.1 causes a Vdd to Output short in this NAND cell. This is because the portion of this CNT between Vdd and Output is entirely p-doped. Figure 2.2 shows a complex logic circuit in which misaligned and mis-positioned CNTs cause incorrect logic functionality.

Unlike Fig. 2.1, any misaligned or mis-positioned CNT in the NAND gate of Fig. 2.3b will not cause any malfunction. This is because any CNT in the pullup network of Fig. 2.3b either passes under the gates corresponding to inputs A or B,

or passes through the etched region between the two gates (in which case it will not conduct). Given sufficient CNT density (e.g., 250 CNTs/ μm), the chance that no CNT passes under a given gate (e.g., gate A or gate B) is very remote. One can create the etched region between the two gates in the NAND pull-up by first creating an extended gate region (Fig. 2.3a) and then etching the gate and CNTs in a single self-aligned lithographic step (Fig. 2.3b).

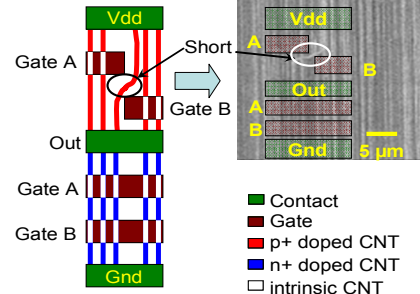


Figure 2.1 Misaligned CNT causing short in NAND logic

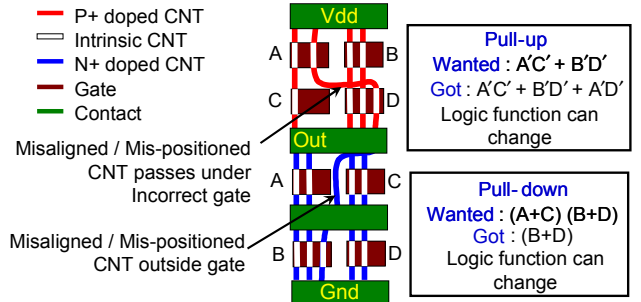


Figure 2.2. Incorrect Logic Functionality caused by misaligned and mis-positioned CNTs.

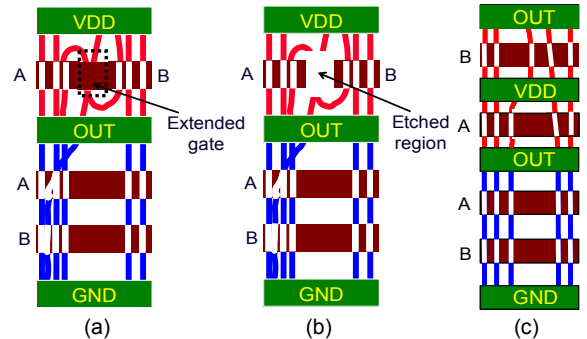


Figure 2.3. (a) Misaligned-and-mis-positioned-CNT-immune NAND with extended gate. (b) Misaligned-and-mis-positioned-CNT-immune NAND with etched region. (c) Misaligned-and-mis-positioned-CNT-immune NAND [Bobba 09].

Two algorithms for misaligned-and-mis-positioned-CNT-immune designs are presented in [Patil 07, 08b]:

1) Given the layout of a circuit implementing a logic function, we can determine whether one or more misaligned or mis-positioned CNTs can result in incorrect logic function implementation using a graph-theoretic abstraction.

2) Given an arbitrary logic function, we can generate a misaligned-and-mis-positioned-CNT-immune layout. Figure 2.4 implements a layout corresponding to the expression $A + (B + C)(D + E)$. It can be proved that this layout is immune to misaligned and mis-positioned CNTs. A modification of this design technique (Fig. 2.3c) is described in [Bobba 09].

The worst case energy, delay and area costs of our approach are 18%, 13%, and 21%, respectively [Patil 07],

which is significantly lower than traditional defect- and fault-tolerance techniques. This approach is also compatible with VLSI since it does not require special customization on individual die basis. Only standard cell layouts need to be modified to make them immune to misaligned and mis-positioned CNTs.

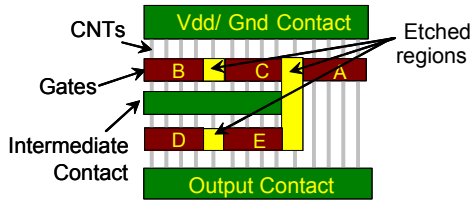


Figure 2.4. Misaligned-and-mis-positioned-CNT-immune layout for network represented by the function $A+(B+C)(D+E)$.

The effectiveness of our misaligned-and-mis-positioned-CNT-immune design techniques [Patil 07, 08b] is demonstrated experimentally in [Patil 08a]. Figure 2.5 shows SEM images of logic structures with the etched CNT regions. Results of electrical measurements performed on these structures are shown in Fig. 2.6. Details of the fabrication process can be found in [Patil 08a].

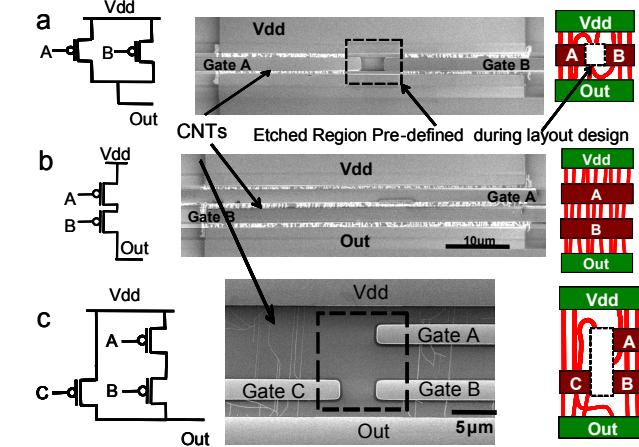


Figure 2.5. SEM images of logic structures corresponding to (a) NAND pull-up (b) NOR pull-up (c) OR-AND-INVERT pull-up.

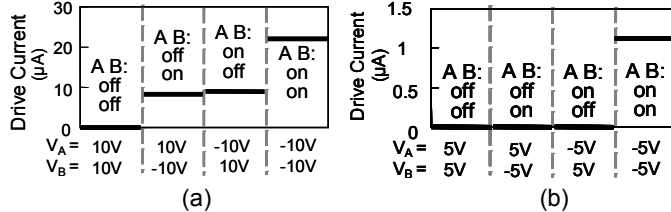


Figure 2.6. Experimental demonstration of correct logic behavior of misaligned-and-mis-positioned-CNT-immune (a) NAND and (b) NOR pull-up logic structures.

3. Metallic-CNT-Tolerant Circuits

An m-CNT in a CNFET acts as a conductive channel whose resistance cannot be controlled by the transistor gate. This behavior is undesirable in CNFET-based logic circuits. As discussed in [Zhang 08], an ensemble of m- and s-CNTs poses major challenges to CNFET-based digital VLSI due to:

1) Excessive leakage: Since m-CNTs cannot be turned off, CNFETs with a typical fraction of 1/3 m-CNTs [Saito 98] can have more than 2,000 times worse I_{on}/I_{off} compared to state-of-the-art CMOS technology.

2) Noise margin degradation: The presence of m-CNTs can result in conducting paths through both pull-up and pull-down networks of logic gates. Hence, even a small number of m-CNTs in a logic gate can severely degrade its noise margin.

3) Variability in circuit performance: The respective numbers of m-CNTs and s-CNTs in a CNFET are unpredictable. This leads to unpredictable performance (e.g. delay) variations in CNFET based logic circuits. We denote the total number of CNTs in a CNFET by N . For fixed inter-CNT spacing (impact of CNT spacing variations is analyzed in Sec. 4), N is directly proportional to the width of the gate of a CNFET. Generally speaking, designing CNFETs with larger N reduces variation. However, larger N imposes penalties (increased circuit area and power consumption).

No existing CNT growth technique grows s-CNTs exclusively. We denote by p_m and $p_s (=1-p_m)$ the average fraction of m-CNTs and s-CNTs, respectively, for a given CNT growth technique. Typical CNT growth processes produce CNTs with $p_m = 1/3$ and $p_s = 2/3$ [Saito 98].

The most natural processing option to tackle the m-CNT problem is to have predominantly s-CNTs on the wafer to start with. A preferential CNT growth technique is used by [Li 04] which yields 90% s-CNTs (i.e., p_m is reduced from 33% to 10%). More recently, a growth technique by [Qu 08] reported an even lower p_m of 4%. Reduction in p_m has also been demonstrated by self-sorting when CNTs are deposited onto the wafer ([LeMieux 08]). While such improvement in p_m (i.e., lower p_m) is necessary, it alone is not enough for VLSI-scale digital circuits.

The other processing option is to remove m-CNTs after CNT growth from an ensemble of m-CNTs and s-CNTs. [Collins 01] introduces a current-induced electrical breakdown technique to achieve m-CNT removal. In this technique, s-CNTs are switched off using gate voltage so that current only flows through m-CNTs. At high current levels, oxidation is induced by self-heating of m-CNTs causing them to break down. This approach has the advantage of high removal rate of m-CNTs. However, a major drawback is that it is not scalable for large-scale VLSI systems since it involves individually contacting and breaking down m-CNTs in each CNFET. Compared to electrical breakdown, gas phase chemical reaction-based removal techniques ([Hassanien 05, Yang 06, Zhang 06]) can be more easily applied at wafer scale. Although high removal rates may be achieved by m-CNT removal techniques, all these techniques also inadvertently remove some (useful) s-CNTs.

Without considering processing details of these removal techniques, we model a general m-CNT removal process using two parameters: p_{Rm} defined as the conditional probability of a CNT being removed given it is an m-CNT, and p_{Rs} defined as the conditional probability of a CNT being removed given it is an s-CNT. An *ideal removal* technique is one for which $p_{Rm} = 1$ and $p_{Rs} = 0$ (i.e., all m-CNTs are removed and all s-CNTs are intact).

3.1 Design and Processing Guidelines for Metallic-CNT-Tolerant circuits

In order for metallic-CNT-tolerant digital logic circuits to be practical at VLSI scale, synergy between processing and

design is necessary. Specifically, the following two questions must be answered:

1. Processing question: What p_m , p_{Rm} and p_{Rs} values must be satisfied for designing CNFET circuits with practical constraints on circuit performance metrics such as leakage, noise margin, and delay variations?

2. Design question: Determine N_{min} , the minimum number of CNTs per CNFET prior to removal (for specified values of processing parameters p_m , p_{Rm} and p_{Rs}), such that the aforementioned constraints are satisfied.

In order to answer these questions, we performed detailed probabilistic analysis in [Zhang 08] and provided design and processing guidelines for practical circuit performance targets. Here, the key results from such analysis are presented.

Figure 3.1 shows how the parameter p_{Rm} can affect the average I_{on}/I_{off} ratio of CNFET circuits. We can determine guidelines for p_{Rm} by applying practical leakage constraints. The target I_{on}/I_{off} value of 10^4 is obtained from [ITRS 07]. It is shown that this target value can be achieved with $p_{Rm} \sim 1 \cdot 10^{-4} = 99.99\%$ for $p_m = 1/3$. The parameter p_{Rs} can be helpful in improving the I_{on}/I_{off} ratio – however, the sensitivity of I_{on}/I_{off} to p_{Rs} is much smaller compared to sensitivity of I_{on}/I_{off} to p_{Rm} , until the p_{Rm} is high enough when the off-current of s-CNTs starts to dominate the total leakage current (corresponding to the flat parts of the curves).

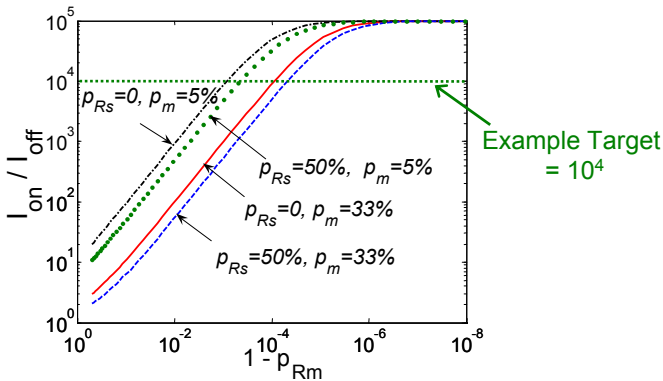


Figure 3.1. $\mu(I_{on})/\mu(I_{off})$ vs. survival probability ($1-p_{Rm}$) (assuming s-CNT alone has $I_{on}/I_{off} = 10^5$).

Similar analysis can be performed to quantify the impact of m-CNTs on gate robustness and delay variations of CNFET circuits. For gate robustness, we use *Probability of Noise Margin Violation (PNMV)* as a metric, which is defined as the probability of a pair of cross-coupled inverters violating a given noise margin requirement (set at $V_{dd}/4$ in the following discussion). For delay variations, “standard deviation (abbreviated as SD) / mean” of single-stage inverter delay driving a fixed load is used as a metric [Cao 05]. The detailed analysis of how m-CNT removal affects these quantities can be found in [Zhang 08]. Figures 3.2 and 3.3 present key results from such analysis by showing how PNMV and delay variations can be affected by different processing and design parameters (p_{Rs} , p_m , and N). It is shown in [Zhang 08] that p_{Rm} no longer plays a very critical role in deciding gate robustness and delay variations once the leakage guideline (i.e., $p_{Rm} > 99.99\%$) is met.

With practical constraints on gate robustness and delay variations (shown as example targets in the Figs. 3.2 and 3.3),

and with the above guideline on p_{Rm} , our recommendation is to use $N_{min} = 28$ and $p_{Rs} = 20\%$ for $p_m = 1/3$. Significant reduction of p_m can improve all the above guidelines for p_{Rm} , p_{Rs} , and N_{min} , as shown in Figs. 3.1-3.3.

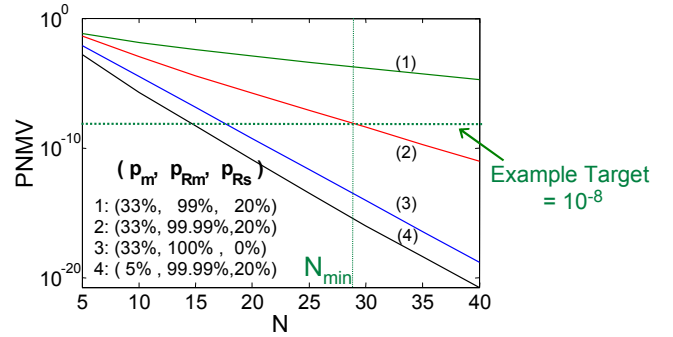


Figure 3.2. PNMV vs. N (details in [Zhang 08]).

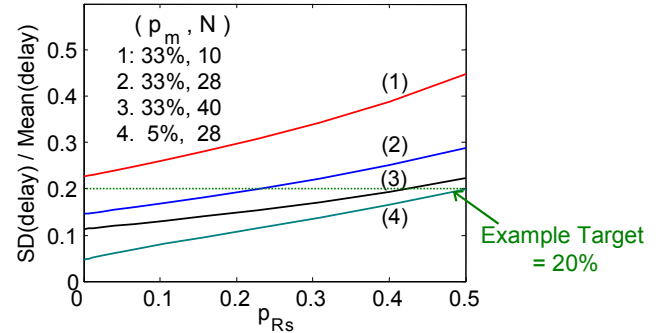


Figure 3.3. SD(delay) / Mean(delay) vs. p_{Rs} using delay model described in [Zhang 08].

3.2 Design for Leakage Reduction in the Presence of Metallic CNTs

Design techniques can also help tackle the m-CNT problem. We show in this section that conventional logic gate layouts can be modified to achieve orders of magnitude reduction in average leakage current.

Figure 3.4 shows how a conventional inverter layout (Fig. 3.4a) can be transformed into a modified layout (Fig. 3.4b) where the n-type (p-type) CNFET is replaced by a stack of two n-type (p-type) CNFETs in series. In the layout of Fig. 3.4b, CNFETs N1 and N2 (P1 and P2) are uncorrelated in a sense that the probability of any CNT in N1 (P1) being m- or s-CNT is independent of the probability of any CNT in N2 (P2) being m- or s-CNT. Therefore, when the removal rate of m-CNTs is high (i.e., p_{Rm} is high), the probability of m-CNTs surviving in both N1 and N2 (P1 and P2) becomes very small. This technique is similar to that of [Moore 56] where it was applied to circuits using relays.

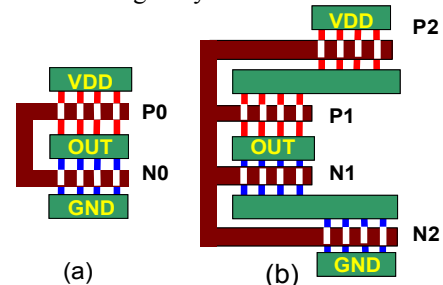


Figure 3.4. Layouts of (a) a conventional inverter (b) an inverter with forced stacking of uncorrelated CNFETs.

Monte Carlo simulation (10^7 samples using CNFETs with $N = 20$) is performed to compare average off-currents of both layout styles in Fig. 3.4, and the results are shown in Fig. 3.5. As shown in Fig. 3.5, the peak off-current reduction happens when p_{Rm} is about 99.9% and the maximum reduction is more than two orders of magnitude. In the cases of very high or very low p_{Rm} values, the amount of leakage reduction is significantly reduced. This is because, for low p_{Rm} (i.e., high $1 - p_{Rm}$) values, the probability of m-CNTs surviving in both N1 and N2 (P1 and P2) is high. On the other hand, for high p_{Rm} values (i.e., low $1 - p_{Rm}$ values), the majority of m-CNTs are removed and the off-currents of both layout styles in Fig. 3.4 are dominated by off-state leakage currents of s-CNTs.

Note that, the layout in Fig. 3.4b introduces significant penalties in gate delays. Similar tradeoffs arise with transistor stacking for leakage reduction in silicon CMOS circuits as well [Narendra 01]. Therefore, layout techniques as in Fig. 3.4b should be carefully applied mainly in non-critical sections of logic circuits.

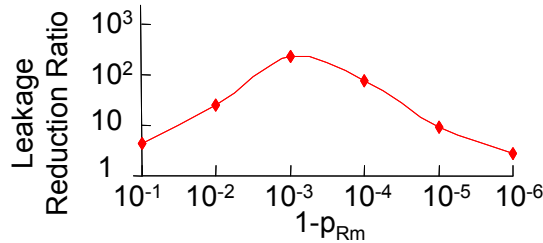


Figure 3.5. Reduction in off-current by forcing CNFET stacking ($p_{Rs} = 20\%$, $p_m = 1/3$, $N = 20$).

4. CNT Density Variations

CNT density is of pivotal importance for CNFET-based VLSI circuits. [Deng 07] shows that, for optimal energy-delay tradeoffs, we need CNFETs with CNT density of about 250 CNTs/ μm . In contrast, state-of-the-art CNT growth techniques yield typical densities of only 10-50 CNTs/ μm [Kang 07]. To increase average CNT density, technology advances are essential.

In addition to the need for high CNT density, another major challenge is the existence of large CNT density variations. Since the exact locations of CNTs cannot be determined during layout design, CNT density variations can result in large delay variations, and a significant probability of complete failure in cases where there may be CNFETs with no CNTs.

For quantitative analysis of such effects, the quantity N (i.e., the number of CNTs in a CNFET prior to m-CNT removal) in Sec. 3 must be treated as a random variable. Instead of directly controlling N , designers can only determine the width of a CNFET, denoted by W , which covers a random number of CNTs. To emphasize the dependency of N as a function of CNFET width W , we write N as $N(W)$ in this section and define $N(W)$ as *CNT count distribution* for a CNFET with width W .

CNT spacing, denoted by S , is defined as the distance between two neighboring CNTs in a CNFET (Fig. 4.1a). Figure 4.1b shows an example of CNT spacing distribution extracted from Scanning Electron Microscopy (SEM) images of $\sim 1,500$ CNTs from an experimental growth.

Extracting distributions of $N(W)$ experimentally can be time-consuming since it is a function of W . Spacing distribution (e.g., Fig. 4.1b), on the other hand, is width independent and easy to extract experimentally. Therefore, simple methods to derive CNT count distribution from CNT spacing distribution are desirable.

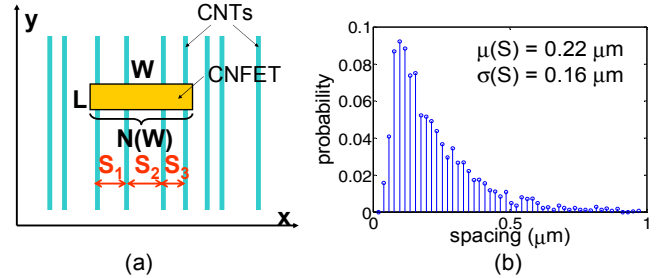


Figure 4.1. (a) CNT count model. (b) CNT spacing distribution extracted from an experimental CNT growth.

[Zhang 09] shows that the probability distribution of $N(W)$ can be characterized using the probability distribution of S . Moreover, using results from renewal theory [Cox 62], it can be shown that when W is large, the distribution of $N(W)$ asymptotically approaches Gaussian with the mean and variance shown below:

$$\lim_{W \rightarrow \infty} N(W) \sim \text{Gauss}\left(\frac{W}{\mu_S}, \frac{W \cdot \sigma_S^2}{\mu_S^3}\right) \quad (4.1)$$

where μ_S and σ_S represent the mean and standard deviation of CNT spacing distribution S . In practice, we find that W does not have to be very large to reach this asymptotic limit. Figure 4.2 compares the approximate Gaussian distribution with experimentally extracted count distribution under two-micron-wide (i.e., $W = 2 \mu\text{m}$) CNFETs, showing good fit with each other. In this case, the mean value of $N(W)$ is only 9 (less than N_{min} shown in Sec. 3.1 and below). Hence, the Gaussian approximation of $N(W)$ is appropriate for most practical CNFET widths.

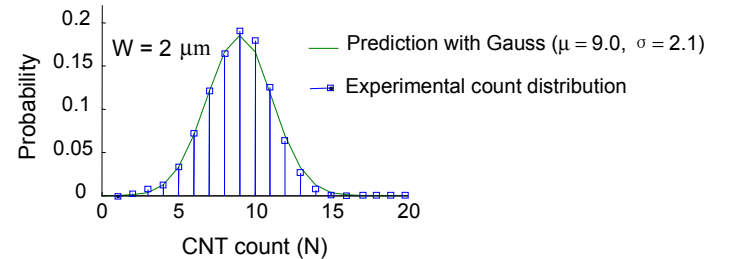


Figure 4.2. Experimentally extracted CNT count distribution compared to predicted distribution with Gaussian approximation.

CNT density variations can further degrade gate robustness and delay variations of CNFET-based logic gates. Figure 4.3 compares the PNMV metric in the cases of both with and without CNT density variations. As shown in the figure, density variations increase PNMV. If the example target of PNMV is again set at 10^{-8} , the corresponding guideline for N_{min} will increase from 28 to 33 when CNT density variations are considered. Figure 4.4 compares the delay variations of a single stage inverter with and without considering CNT density variations. Similar to Fig. 3.3, the results are calculated using the model presented in [Zhang 08]. As shown in the figure, CNT density variations further increase the amount of delay variations.

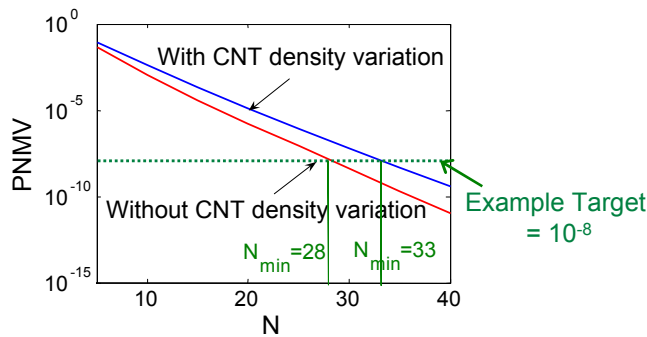


Figure 4.3. PNMV vs. N with and without considering CNT density variations. In both cases, $p_m = 33\%$, $p_{Rm} = 99.99\%$ and $p_{Rs} = 20\%$.

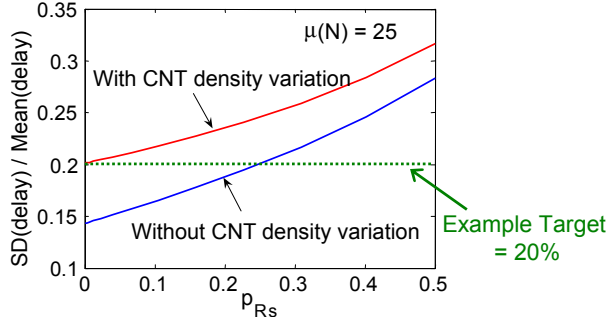


Figure 4.4. Delay variation of an inverter driving a fixed load with and without considering CNT density variations. The mean value of $N = 25$, $p_m = 33\%$ and $p_{Rm} = 99.99\%$, in both cases.

5. Conclusions

We have the following messages for researchers interested in digital system design in emerging nanotechnologies such as CNFETs:

1. Imperfection-immune design is required.
2. It is extremely important to optimize across processing and design. Otherwise, we will end up with solutions that are either impractical or highly inefficient.
3. Traditional defect- and fault-tolerance techniques must be applied very carefully. Otherwise, the benefits of such emerging nanotechnologies can significantly reduce.
4. Design techniques must be compatible with VLSI processing and design flows.

Imperfection-immune design techniques and experimental results, presented in this paper, are based on these principles, and may pave the way for VLSI-scale CNFET technologies.

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