MTJ-Based Nonvolatile Logic-in-Memory Circuit, Future Prospects and Issues

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***Abstract*—Nonvolatile logic-in-memory architecture, where nonvolatile memory elements are distributed over a logic-circuit plane, is expected to realize both ultra-low-power and reduced interconnection delay. This paper presents novel nonvolatile logic circuits based on logic-in-memory architecture using magnetic tunnel junctions (MTJs) in combination with MOS transistors. Since the MTJ with a spin-injection write capability is only one device that has all the following superior features as large resistance ratio, virtually unlimited endurance, fast read/write accessibility, scalability, complementary MOS (CMOS)-process compatibility, and nonvolatility, it is very suited to implement the MOS/MTJ-hybrid logic circuit with logic-in-memory architecture. A concrete nonvolatile logic-in-memory circuit is designed and fabricated using a 0.18 μm CMOS/MTJ process, and its future prospects and issues are discussed.**

Keywords-nonvolatile; logic-in-memory; MTJ; standby-power-free; quick sleep/wake-up

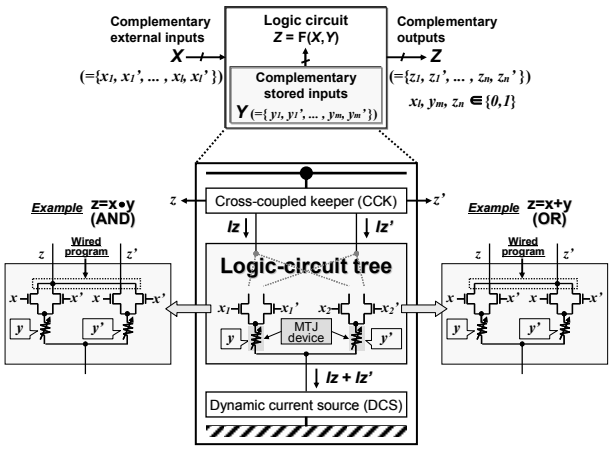

Figure 1. General structure of an MTJ-based logic-in-memory circuit.

I. INTRODUCTION

Reduction of power consumption and interconnection delay are the two major targets for the next generation very large scale integrated circuits (VLSIs). Drastic increase of static power dissipation is being anticipated due to leakage current in beyond 45 nm complementary metal oxide semiconductor (CMOS) technology [1]. In addition, increase in the length of global-interconnection in advanced VLSIs results in further increase of both power and delay. Logic-in-memory architecture [2], where memory elements are distributed over a logic-circuit plane, combined with nonvolatile memory is expected to realize both ultra-low-power and shorten interconnection delay [3]-[7]. However, in order to fully take advantage of the logic-in-memory architecture, it is important to implement a nonvolatile memory that has a capability of shorter access time below 10 ns, unlimited endurance, scalable write, and small dimension comparable to the employed CMOS technology. The only available candidate of a nonvolatile memory that could satisfy all the above requirements at this stage is the one using magnetic tunnel junction (MTJ) with spin-injection write [8]-[10].

In this paper, a concrete nonvolatile login-in-memory circuit, a nonvolatile full adder [11], is designed and fabricated using a 0.18 μm CMOS/MTJ process.

Since stored data has been already memorized into MTJ devices in the proposed circuits, the supply voltage can be immediately cut off without data transmission into external nonvolatile storage devices when the circuit changes to a standby mode. This property achieves great reduction of power dissipation.

II. LOGIC-IN-MEMORY CIRCUIT USING MTJ DEVICES

Fig. 1 shows an MTJ-based logic-in-memory circuit model. It consists of three basic components; a cross-coupled keeper (CCK), a logic-circuit tree and a dynamic current source (DCS). The CCK generates complementary binary outputs, z and z', in accordance with a magnitude-comparison result between two current signals, Iz and Iz', where precise current difference can be immediately detected by using the feedback circuit structure. The use of the DCS makes it possible to cut off steady current

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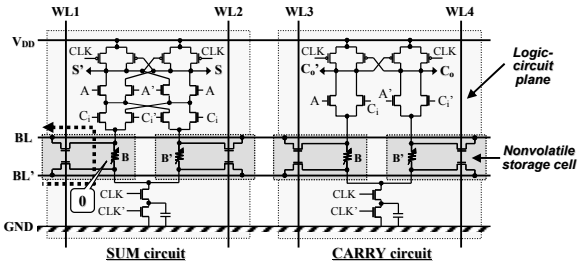


(a)

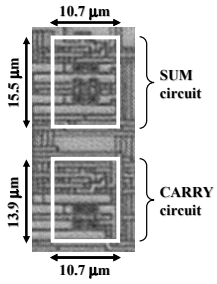
B	A	C_i	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

SUM CARRY

*1) *2)

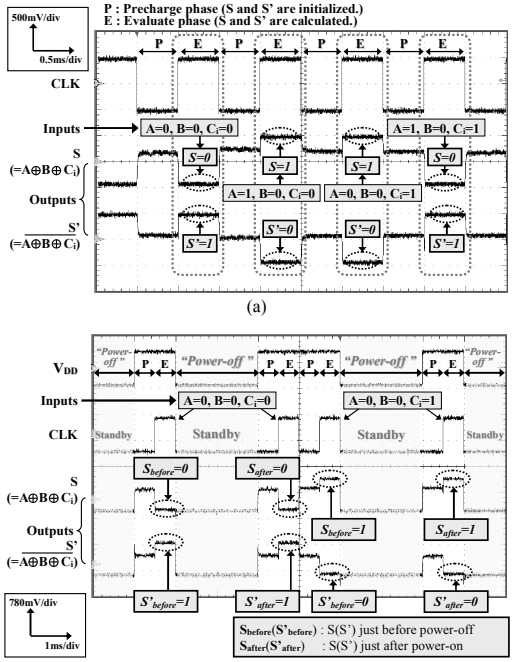
*1) The four input-patterns are demonstrated in Fig.3(a).
*2) The two input-patterns are demonstrated in Fig.3(b).

(b)



(c)

Figure 2. Nonvolatile full adder based on logic-in-memory architecture: (a) Overall circuit structure of the full adder with nonvolatile stored inputs. MTJs are merged into logic-circuit planes (surrounded by dotted lines). (b) Truth table of the full adder. (c) Chip photomicrograph of the CMOS-circuit part.



(a)

(b)

Figure 3. Measured waveforms of the SUM circuit in the fabricated nonvolatile full adder chip: (a) SUM operation in an active mode. (b) Sleep/wake-up behavior due to transition between active and standby mode.

from V_{DD} to GND, which results in low-power dissipation. Arbitrary logic circuits are realized by programming the configuration of the logic-circuit tree. For example, two-input AND and two-input OR gates are realized by using 4 NMOS transistors and two MTJ devices as shown in Fig. 1. By changing the wired-connection points of the logic-circuit tree, two different gates are simply realized.

III. MTJ-Based Nonvolatile Full Adder For a Fully-Parallel Image Processor

The proposed MTJ-based nonvolatile logic-in-memory circuit is suitable for realizing a fully-parallel VLSI, because nonvolatile storage elements are merged into a fine-grain processing element (PE). In this section, we discuss about a nonvolatile full adder for an operation unit of sum of absolute differences (SAD) which is used for a motion-vector detection of an MPEG encoding [6]-[7].

A. MTJ-Based Nonvolatile Logic-in-Memory Full Adder

We have employed a nonvolatile full adder circuit to demonstrate a circuit based on logic-in-memory architecture. Fig. 2(a) shows the circuit diagram of the full adder, whose logic function is represented by the table in Fig. 2(b). It consists of SUM-circuit and CARRY-circuit parts, where the symbols A (A'; the complement of A) and C_i (C_i') are the external inputs and the symbol B (B') is a stored input. The use of a dynamic logic style [13] controlled by clock signals, CLK and CLK', cuts off the steady current flow from the supply voltage V_{DD} to GND, which reduces the dynamic power dissipation of the circuit.

The stored data is programmed by controlling external signals. Complementary stored inputs, B and B', are programmed by using individual current-flow path, which is selectable by the word lines, WL1, WL2, WL3, and WL4, and the bit lines, BL and BL'. For example, in the case of storing B = 0 into the corresponding MTJ in the SUM circuit, the word line WL1 is set to the supply voltage V_{DD}, and BL and BL' are set to GND and V_{DD}, respectively, which makes the current-flow path through the MTJ set up as shown in Fig. 2(a). All the external inputs and the complementary clock signals are turned off during the above write operation.

B. Chip Fabrication

Fig. 2(c) shows a test-chip photomicrograph of MOS-transistor-circuit parts with a 0.18 μm CMOS process. The effective areas of SUM and CARRY parts are about 166 μm^2 and 149 μm^2, respectively.

Fig. 3 shows the measured waveforms of the SUM-circuit chip combined with the fabricated MTJs. Since the dynamic logic style is used in the proposed circuit, the output results, S and S', appear at evaluate phase "E", while S and S' are initialized to intermediate state at precharge phase "P" as shown in Fig. 3(a). When four kinds of input patterns (ABC_i) = (000), (100), (001), (101) are applied to the SUM-circuit chip, it is confirmed that the expected complementary outputs are observed as (SS') = (01), (10), (10), and (01), respectively, in the measured waveforms. Because the inputs, B and B', are stored in nonvolatile storage elements (MTJs), the supply voltage can be cut off with maintaining stored data in a standby state. This eliminates the static power dissipation of the logic

TABLE I. COMPARISON OF FULL ADDERS.

	CMOS	**Proposed**
Delay	224 ps	**219 ps**
Dynamic power (@500MHz)	71.1 μW	**16.3 μW**
Write time	2 ns/bit	**10 ns/bit (2 ns/bit)** *1)
Write energy	4 pJ/bit	**20.9 pJ/bit (6.8 pJ/bit)** *1)
Static power *2)	0.9 nW	**0.0 nW**
Area (Device counts) *3)	333 μm² (42 MOSs)	**315 μm²** (34 MOSs + 4 MTJs)

*1) High-speed write is expected at 2ns in precessional mode, while the write current becomes 1.28 times larger than that at 10ns write.[13]
As the result, the write energy at 2ns write is reduced to 33(=100*1.28*1.28/5) percent.
*2) Power must be supplied in order to maintain stored data in CMOS-based storage circuit at any time. On the other hand, power supply can be cut off in the proposed nonvolatile logic-in-memory circuit.
*3) The proposed full adder is compactly implemented compared to CMOS implementation, because storage elements are stacked over a logic-circuit plane.

circuit with stored inputs. Moreover, since nonvolatile storage elements are merged into a logic-circuit plane in this circuit, only a short time lag to read the stored data is expected, which results in a quick sleep/wake-up VLSI system.

Fig. 3(b) shows the measured waveforms of the SUM-circuit chip, where the stored inputs, B and B', are fixed to '0' and '1', respectively and periodic 1.0-V-peak-to-peak voltage signals are applied to CLK, CLK', A, A', C_i, and C_i', respectively, under periodic turn on and off of V_{DD} = 1.0 V. It can be clearly seen in the traces of Fig. 3(b) that the output S_{after} (S right after power-on) is the same as S_{before} (S just before power-off), which means that stored data remain intact even if V_{DD} is shutdown and is turned on again. It should be noted that nonvolatile storage function of the present circuit is realized without employing complex reload/write-back from/into an off-chip nonvolatile storage device.

C. Evaluation

In order to confirm the advantages of the present circuit, we have employed a circuit simulator HSPICE under a 0.18 μm CMOS process and evaluated the performance.

Table I summarizes the results: Dynamic power dissipation is reduced to 23 % of that of the conventional circuit under the normalized delay, because the present circuit structure makes it possible to reduce the number of current paths from V_{DD} to GND, compared to CMOS-only implementation. The proposed nonvolatile logic-in-memory circuit makes it possible not only to eliminate the static power consumption but also to reduce the chip area. In the nonvolatile logic-in-memory circuit, write time of an MTJ is one of the most important elements, because it also dominates the write energy when updating stored inputs in the nonvolatile logic-in-memory circuit. With progress in the performance of MTJ, we expect that a high-speed, ultra-low-power, and compact VLSI can be realized.

IV. CONCLUSION

A new circuit structure, called an MTJ-based logic-in-memory circuit, has been presented and its basic behavior has been demonstrated by the chip fabrication. By using HSPICE simulation, it is also demonstrated that the power dissipation and effective area of the proposed circuits are greatly reduced in comparison with those of the corresponding CMOS-only implementation.

As a future prospect, it is also important to establish design and verification tools of the CMOS/MTJ-hybrid circuit. Since the supply voltage can be immediately cut off and turned on again in the proposed circuitry, the dedicated power control technique such as fine-grain power management technique should be considered for realizing an ultra-low-power VLSI system.

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