Nano-electronics Challenge

Chip Designers meet Real Nano-electronics in 2010s?

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I. Past and Future of Silicon-based CMOS Technolgies and Applications

During 1990s, silicon-based CMOS made steady advancement with miniaturization and with lower power consumption by incorporating the scaling effect and expanded its share by invading the region of bipolar transistors and compound semiconductors market. On the other hand, new semiconductor application technologies grew rapidly one after the other in conjunction with the development of silicone CMOS technologies. Such developments included the microprocessor for PC, server and router chipsets for internet application, RF for cellular phones, analogue circuitry, base band processors, and wireless LAN technologies. Also in memory areas, the flash memory technology was introduced into the market and FeRAM, MRAM, and PRAM technologies with new principles were introduced into the market.

From year 2000 around, CMOS scaling began to lose its effectiveness and could not improve chip performance much when compared with that of 90's. Figure 1 shows the trend of micro-processor performance, which indicates a typical trend of semiconductor chip performance. The performance is contributed by 3 major factors. The contributing factors are MOS transistor (MOSFET) speed, clock frequency improvement, and the architecture improvement (mainly the improvement of parallel speed; see figure captions.). Around 2000, the chip temperature increased drastically due to huge CMOS leakage current and this resulted in no further clock frequency increase. Also at about the same time, the simple miniaturization of silicon-based MOSFET did not result in the speed improvement from physical reasons of nano-scale devices. Some improvement was accomplished with increased electron/hole mobility by applying the strain to silicon, but it was so much less than what was achieved by scaling during 90's.

It may not be an exaggeration to say that the chip performance improvement can be achieved almost by working on the architecture in very near future. The key for it is the multi-core approach supported by low power consumption circuit designs. But continued significant improvement of the chip performance can not be achieved only with the architecture improvement.

This was something predicted from 90's and during those days, there was a strong expectation toward nano-technology and more attention was on nano-electronics and post-Si technology.

II. Nessecity of Nanoelectronics and Co-design

But when we look back, this uncertain era started with the collapse of IT bubble in 2001 together with September 11 terrorist attacks and this induced rather conservative trends in

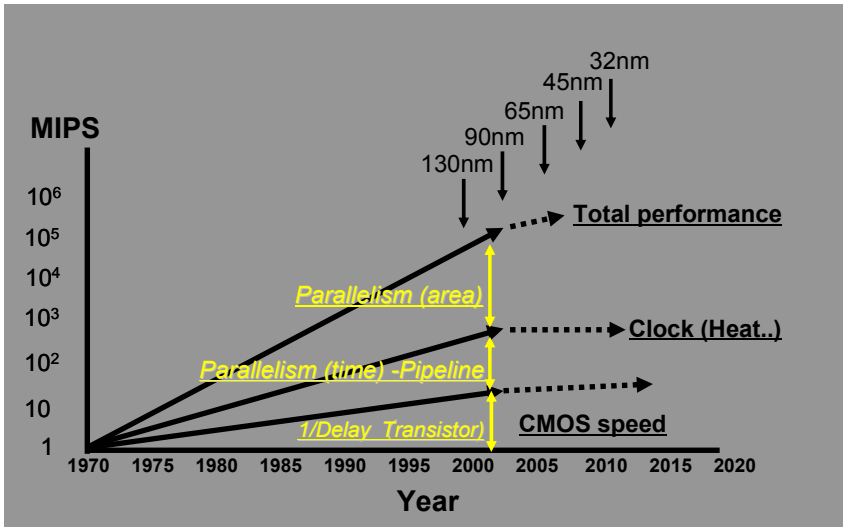

Figure 1. Trend of micor-processor performance and contribution by 3 major factors: MOS transistor (MOSFET) speed, clock frequency increase, and the architecture improvement. Clock frequency increase contributed to increase in time-domain-parallelism (linked with pipeline) and architecture mainly contributed to area-domain-parallelism. Since around 2000, clock frequency has not been increased due to chip heating. Also at about the same time, the simple miniaturization of silicone MOSFET did not result in the speed improvement due to nano-scale device limitation. Some improvement was accomplished by applying the strain to silicon, but it was not as much as what was achieved by scaling during 90's. Currently, it is not an exaggeration to say that the chip performance improvement can only be possible by working on the architecture. The key technology is the multi-core approach supported by low power consumption technology. But continued significant improvement of the chip performance can not be achieved only with the architecture improvement.

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semiconductor industries. This can be called as "*Neo-conservative*" semiconductor age. Due to this trend, further investment toward nano electronics became rather limited and semiconductor studies in the academic almost followed the same pattern.

From 2001 till now, nano electronics are confronting severe winter stage and very little progress was achieved. Thus nano electronics stagnated for 10 years. What this means is that the majority of the resource from year 2000 on, was spent on further improvement and optimization of 90's technologies. There is a strong possibility that this will cause negative impacts on future semiconductor business. Also, the manufacturing and design costs of the semiconductor are increasing exponentially as time goes on and there will be a high risk of the semiconductor business if the current situation continues.

When we look at the application side, unfortunately innovative applications were very limited and most of them were improvements of existing technologies with less expensive or with easier interface, which seemed best way to make profit in these 10 years.

Thus, in another words, there was little significant development of neither "More Moore" nor "More than Moore" in these 10 years, as shown in Fig.2.

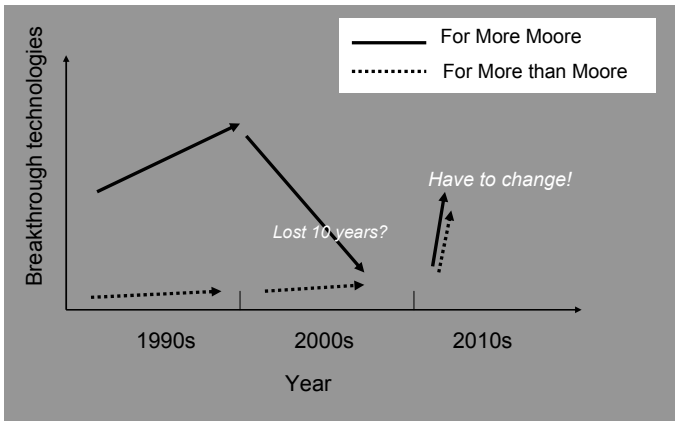

Figure 2. Trends of breakthrough technologies developed in every 10 years in the field of semiconductor technologies for SoC.

Considering all these situations, it is vital for nano electronics to undertake an immediate action in order to catch up with what was lost in past 10 years. For that purpose, ***co-design*** by designers and technologists is essential. This is because very short term development of these nano-electronics is needed for this situation. If conventional ways are taken, only devices are firstly developed. Then, after their development is completed in around 10-20 years, designers start to build circuits and systems, and in most cases it is found that the devices have to be largely improved. On the basis of co-design for nano-electronics, designers have to have plural candidates of devices for their new applications and clarify the requirements for the devices even in early stages. Technologists have to improve the devices to meet the requirements. In late stages, the designers ought to select only one device and the technologists ought to finalize high-performance devices with higher reliability and lower cost.

Currently, there is one large difficulty in starting co-design. Although there have been various emerging devices proposed by experts in technologies, most seem to be *so cutting edge* that designers could not see the reality and could not consider if these emerging devices can meet their future requirements. As a result, there has been a very large gap between academia and industry, and there has been very limited breakthrough for post-Si-based neon-electronics.

However, in very rear cases, unique co-design-based works are tried in some academia. These examples may give a chance to change this gap. The purpose of this session is giving opportunities to learn three practical case-studies. They will be presented on how designers and technologists can collaborate to resolve the challenges of post-silicon devices.

III. CHIP DESIGNERS MEET REAL NANO-ELECTRONICS IN THIS HOT TOPIC SESSION?

The first topic is power saving. It is evident that the most serious issue is increasing power consumption of the chip. To save power, very unique approach is "non-volatile logic" using hybrid circuit of the emerging non-volatile memory devices and CMOS. Magnetic-RAM technology using multi-tunneling-junction (MTJ) devices can be used for the hybrid design. The non-volatile logic will make conventional CMOS designers clearly understand "how nano-electronics can solve the issues of conventional CMOS".

The second topic is performance vs. process variation. Industries simply need high speed devices with low power consumption after the end of silicon-based-CMOS scaling. Strong candidates for this are III-V compound semiconductors (with a high bandgap like GaAs) and CNT-FET, and they are intensively studied very recently. In general, the process variation with these emerging devices will increase more when compared with that of conventional silicon-based-MOSFET, where the process variation has already been a big problem. Therefore, even though high performance CMOS circuits using post-silicon semiconductors can be expected, a new immunity design for the process variation is essential for realizing these devices. This paper introduces a very unique design method for it.

The third topic is a new architecture using emerging nano-devices, which are called as nano-architectures. It is well known that nano-carbon based mechanical switch (NEMS) has an excellent mechanical property. New nano-electronics applications have been expected not only for memory applications or sensor applications, but also even high-speed logic applications for FPGA. This paper introduces a new nano-architecture of 3D-FPGA with new logic circuits using the NEMS based on CMOS hybrid techniques. In addition, crossbars using nano-wire transistors contribute performance and function of the 3D-FPGA on this case study.

These three case studies will make audiences see impacts of nano-electronics and understand further breakthroughs needed for the nano-electronics based on co-design.