Impact of Voltage Scaling on Nanoscale SRAM Reliability

Vikas Chandra
ARM R&D
vikas.chandra@arm.com

Robert Aitken
ARM R&D
rob.aitken@arm.com

***Abstract*—Low voltage SRAMs are critical for power constrained designs. Currently, the choice of supply voltage in SRAMs is governed by bit cell read static noise margin, writability, data retention etc. However, in the nanometer technology nodes, the choice of supply voltage impacts the reliability of SRAMs as well. Two important reliability challenges for current and future generation SRAMs are gate oxide degradation and soft error susceptibility. The current generation transistors have ultra-thin gate oxides to improve the device performance and they are prone to breakdown due to higher level of electric field stress. In addition, the soft error susceptibility of SRAMs has significantly increased in the nanometer regime. In this work, we have quantified the impact of voltage scaling on the soft error susceptibility of gate oxide degraded SRAMs. We show that when gate oxide degradation is taken into account, there exists an optimal voltage (V_{opt}) at which the bit cell $Qcrit$ is maximized. Further, we show that both V_{opt} and $Qcrit_{max}$ are a function of the level of oxide degradation. Finally, we investigate the impact of technology node scaling and analyze the trend of V_{opt} and $Qcrit_{max}$. As the technology node shrinks to sub-45nm, both V_{opt} and $Qcrit_{max}$ decrease sharply, thus significantly decreasing the reliability of SRAMs.**

I. Introduction

SRAM design is becoming increasingly challenging with each new technology node. The design challenges are introduced due to increase in leakage, decrease in static noise margin, bit cell writability and robustness concerns. Further, the supply voltage in SRAMs is also being aggressively scaled to reduce power consumption [10], [20]. Until now, voltage scaling in SRAMs has been agnostic to lifetime reliability concerns. The two important reliability challenges for current and future generation SRAMs are soft error susceptibility and gate oxide degradation. The choice of supply voltage impacts both the susceptibility of soft errors and the probability of gate oxide breakdown.

Rapidly shrinking technology nodes and aggressive voltage scaling have increased the probability of soft errors. Soft errors are radiation induced faults which happen due to a particle hit, either by an alpha particle from impurities in packaging material or a neutron from cosmic rays [1], [17]. When particles strike the silicon substrate, they create hole-electron pairs which are then collected by *pn* junctions via drift and diffusion mechanisms. This collected charge creates a transient current pulse and it, if large enough, can flip the value stored in the state saving element (latch, bit cell). These upsets are called Single Event Upsets (SEU). SRAMs are especially vulnerable to SEU due to the small size of the bit cell and small node capacitances.

Progressive gate oxide breakdown (GBD) in CMOS devices is becoming one of the most important source of time dependent degradation [15]. The gate oxide thickness (t_{ox}) of CMOS devices has been steadily decreasing with the technology node scaling. The continuous scaling in the last few decades has led to oxide thicknesses below 2 nm in state-of-the-art technologies. Thinner gate oxides and saturating supply voltage result in large electric field in the gate oxide which eventually forms traps in the oxide leading to tunneling current. Tunneling currents further degrade the oxide and more traps are formed. Once enough traps are formed, they start affecting the electrical properties of the device. With the given process scaling trend, soft oxide breakdown is more likely to happen during the product lifetime.

With the introduction of high-k gate dielectrics in 45nm technology node, the probability of having gate oxide degradation during the device lifetime increases substantially. This degradation will not lead to drastic failure but it will certainly change the design properties, namely, energy, delay, noise margin etc [11], [12], [19]. As the gate oxide degrades with aging, the susceptibility of the design to soft errors changes as well. The level of gate oxide degradation as well the susceptibility of soft error is a strong function of the supply voltage. In this work, we have quantified the impact of voltage scaling on the soft error susceptibility of gate oxide degraded SRAMs. We show that when gate oxide degradation is taken into account, there exists an optimal voltage (V_{opt}) at which the bit cell soft error robustness (denoted by critical charge, $Qcrit$) is maximized. Further, we show that both V_{opt} and the maximum value of critical charge, $Qcrit_{max}$, are functions of the level of oxide degradation. As the technology node shrinks to sub-45nm, both V_{opt} and $Qcrit_{max}$ decrease sharply, thus significantly decreasing the reliability of SRAMs.

The rest of the paper is organized as follows. Section II describes the background of soft error and gate oxide breakdown. Section III discusses the trend of soft errors in current generation SRAMs. Section IV explains the model of the gate oxide breakdown used in this work. Section V analyzes the impact of supply voltage scaling on the soft error susceptibility of SRAMs. Section VI summarizes the work and concludes.

II. Background and Related Work

The two reliability degradation mechanisms, soft error and gate oxide breakdown, are independently understood quite well. However, their interaction with each other is not as commonly investigated. Their relationship becomes very critical as the technology node scales to 45nm and smaller. This section gives an overview of the two degradation mechanisms and related work.

978-3-9810801-5-5/DATE09 © 2009 EDAA

A. Soft Error

When alpha particles or neutrons hit silicon, they generate hole-electron pairs which can then be swept to diffusion junction if an electric field exists across the device. This has the effect of causing a short duration pulse of current. The effect of the strike on the diffusion can be modeled as a current source as shown in Figure 1. A soft error will happen if the

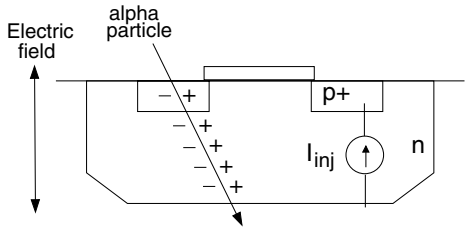


Fig. 1. An alpha particle hit on a PMOS transistor

collected charge at the junction is equal to the critical charge ($Qcrit$). $Qcrit$ is defined as the minimum charge needed to flip the bit stored in the storage cell. To estimate a circuit's sensitivity to soft error, the $Qcrit$ value is calculated. The higher the value of $Qcrit$, the more difficult will be to flip the cell and hence it will be more robust. $Qcrit$ is directly proportional to the node capacitance and supply voltage. With technology scaling, usually the node capacitance and supply voltage also scale down thus decreasing the value of $Qcrit$. For a given current pulse waveform $i(t)$, $Qcrit$ is defined as the minimum time integral on $i(t)dt$ that results in a cell flip (Equation 1).

$$Qcrit = \int_0^t i(t)dt \tag{1}$$

There has been a lot of work on choosing the right shape of the current pulse. In [18], the authors use a triangular pulse and in [4] the authors conclude that the shape of the pulse will vary but it can be represented by a piecewise linear function with a peak corresponding to the funneling charge collection and a more slowly decaying tail for the diffusion charge collection. In [9], [14], the authors describe a double exponential current pulse, as described by Equation 2.

$$i(t) = \frac{Q_{total}}{\tau_f - \tau_r} \cdot \left(e^{-t/\tau_f} - e^{-t/\tau_r}\right) \tag{2}$$

In this equation, Q_{total} denotes the total amount of charge generated by the strike, τ_r and τ_f are the rise and fall time constants respectively. The value of τ_r is much smaller than τ_f and hence most of the charge collection happens right after the steep current rise. In reality, the peak value of the current pulse and the rise/decay time constant will depend on particle type, particle energy, angle of incidence etc. The area under the current curve denotes the charge dumped on (or taken away from) a node where the strike happens. For a more robust storage cell, the area under the curve will be larger.

B. Gate Oxide Breakdown

Current generation devices are prone to progressive gate oxide degradation during their lifetime. The oxide degradation begins when the traps begin to form in the gate oxide. At first the traps are non-overlapping and thus do not conduct. As more traps are formed, they start to overlap and possibly form a resistive conduction path from gate to channel. This type of breakdown is known as soft oxide breakdown (SBD). Once the conduction channel is formed, more traps appear due to thermal damage. These new traps cause the conduction channel to become wider and hence more current flows leading to even higher temperature. This *thermal runaway* condition leads to a catastrophic failure known as hard oxide breakdown (HBD).

Figure 2 shows the three phases of gate oxide wearout [19]. The traps start to form at the end of the first phase. During the second phase (soft oxide breakdown phase), the traps move around and the leakage current fluctuates randomly. In this phase the device is still functional but drifts in energy and delay. Once the conduction path is formed in the oxide, the device enters the realm of hard breakdown (third phase). In this phase, the leakage current is exponentially higher and the fault is termed as catastrophic. The transition from the beginning of soft oxide breakdown to hard breakdown is not abrupt. The gate leakage current starts to progressively increase long before the hard breakdown occurs (Figure 2).

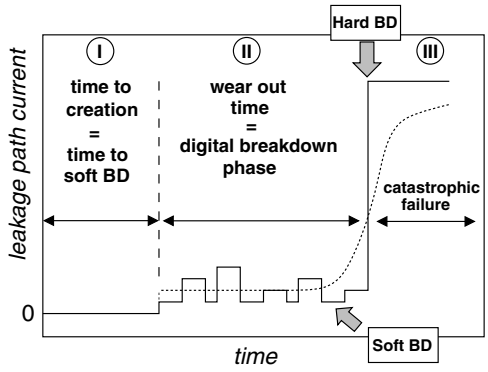


Fig. 2. Wear-out and breakdown model for thin gate oxides [19]

Gate oxide breakdown (GBD) has been investigated in the context of device functional failure. Most of the analyses have been done for the hard breakdown of oxides with associated resistances ranging in few tens of KΩ and lower. The impact of oxide breakdown on circuit functionality for simple circuits has been investigated in [7]. The observed degradation in circuit performance is due to the increase in gate leakage and the reduction in gate transconductance which can lead to functional failure. The effect of GBD on SRAM static noise margin and functionality has been discussed in [8]. In [19], the authors describe the impact of soft oxide breakdown on the energy/delay drift in SRAMs. It has been shown that SRAM bit cell noise margin is significantly affected when the GBD happens in the pull-down NMOS [11]. As GBD is most likely to happen during the device lifetime for sub-45nm designs, it is important to understand its impact on circuit reliability. The effect of aging on soft error susceptibility ($Qcrit$) has been briefly described in [2] but the analysis is not exhaustive. In this work, we have analyzed the impact of supply voltage on the soft error susceptibility of gate oxide degraded SRAM.

As the supply voltage increases, the bit cell becomes more robust against soft errors and the value of $Qcrit$ increases. However, increasing the supply voltage also increases the leakage due to gate oxide degradation which tends to reduce the value of $Qcrit$. Due to these two opposite trends, there exists an optimal supply voltage at which the bit cell $Qcrit$ is maximized in the presence of gate oxide breakdown.

III. Soft Error Trends in SRAMs

It is important to understand the trend of soft error susceptibility with technology and voltage scaling in the absence of gate oxide degradation. The value of $Qcrit$ of an SRAM without oxide degradation provides an upper-bound on the bit cell robustness. A 6 transistor (6T) bit cell is shown in Figure 3. A 6T bit cell is a dense, symmetrical storage cell consisting of two identical back-to-back inverters and is a basic building block of a high density SRAM. The bit cells used in this work are from commercial libraries in 65nm and 45nm technology nodes. Also, the analyses in the following sections are based on detailed extracted netlists which include all the parasitic capacitances. This is important as parasitics change the value of $Qcrit$ substantially.

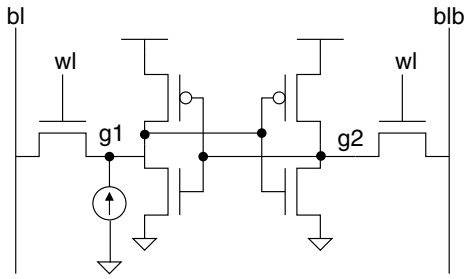
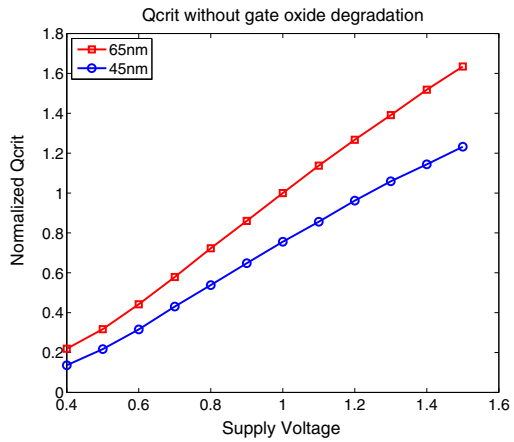


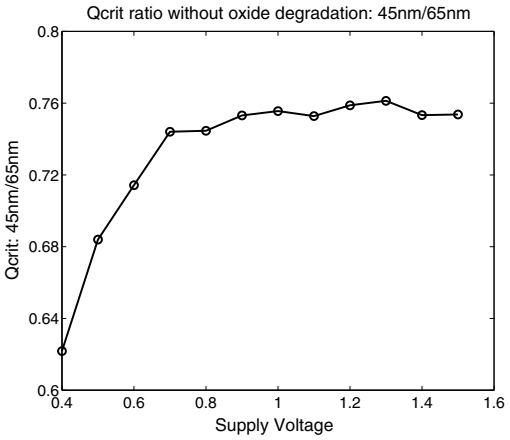
Fig. 3. Particle strike modeling in a 6T bit cell

The factors which impact the critical charge of a bit cell are described in [6]. The two critical nodes in Figure 3 are shown as nodes $g1$ and $g2$. The criticality results from the small size of the bit cells and their associated tiny capacitances (10^{-16} to 10^{-17} F). Technology scaling further decreases the node capacitances and hence increases the soft error susceptibility of SRAMs [3]. As described in Section II-A, a particle strike is modeled as a current source. The current source shown in Figure 3 represents the charge generated at node $g1$ when it gets struck by a particle. Since the bit cell is symmetrical, the analysis of particle strike on node $g2$ will be identical to that of node $g1$.

Figures 4(a) and 4(b) show the impact of technology and voltage scaling on the bit cell $Qcrit$. Specifically, Figure 4(a) plots the values of $Qcrit$ for 65nm and 45nm bit cells with respect to the supply voltage. Figure 4(b) shows the ratio of 45nm to 65nm $Qcrit$. The linear relationship of $Qcrit$ and voltage in Figure 4(a) can be explained by the charge-voltage formula, $Q = C \cdot V^{\alpha}$, where C represents the node capacitance and α represents the sensitivity of $Qcrit$ with voltage (the value of α is close to "1"). It is also interesting to compare the relative ratios of bit cell $Qcrit$ values at 45nm and 65nm nodes, as shown in Figure 4(b). As the voltage is scaled



(a)



(b)

Fig. 4. (a) $Qcrit$ scaling for a bit cell with voltage in 65nm and 45nm (b) Ratio of bit cell $Qcrit$ (45nm/65nm) with voltage

down from 1.5V, the ratio of $Qcrit$ remains fairly constant at 0.75 up until 1V. As the voltage is scaled down to 0.4V, the ratio falls to 0.62 and hence voltage scaling increases the soft error upset susceptibility by $\sim$18%. The impact of technology and voltage scaling on the soft error susceptibility of SRAMs is described in detail in [3].

IV. Gate Oxide Degradation Model

We only considered gate to diffusion (source or drain) breakdown since it represents the worst case scenario [5]. Breakdown to the channel can be modeled as a superposition of gate-drain and gate-source breakdowns. Figure 5 shows the fault model for the gate oxide breakdown defect. We have used the voltage dependent *power-law* oxide degradation model [21], [22]. Once the gate oxide degrades, the increase in gate leakage is modeled as a voltage dependent current source between the gate and the source or drain depending on the location of the breakdown. A linear ohmic oxide breakdown resistance is not sufficient to model the experimental data. The ohmic model only provides good results for hard breakdown

but the power-law leakage current model predicts progressive oxide breakdown behaviors much better prior to the final hard breakdown [12], [13]. As shown in Figure 5, the power-

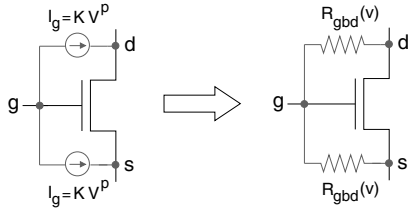


Fig. 5. Power-law gate oxide breakdown model for an NMOS transistor

law current model can be converted to a voltage dependent resistance model (Equation 3).

$$R_{gbd}(V) = \frac{V}{K \cdot V^p} = \frac{1}{K} \cdot V^{(1-p)} \quad (3)$$

In Equation 3, the exponent p refers to the level of oxide degradation and K reflects the "size" of the breakdown spot.

The exact values of K and p are difficult to predict for a new technology node as device post-breakdown behaviors are extremely complicated. Device characteristic after gate oxide breakdown relies on many parameters including breakdown location, transistor type, voltage polarity, device operation mode, oxide area and even poly-gate doping type. However, based on silicon measurements, it was found that p is in the range of $\sim$5 and K is in the range of $\sim 10^{-5}$ [13]. Figure 6 shows the values of $R_{gbd}(V)$ as a function of voltage for representative values of K and p. From Equation 3 and Figure

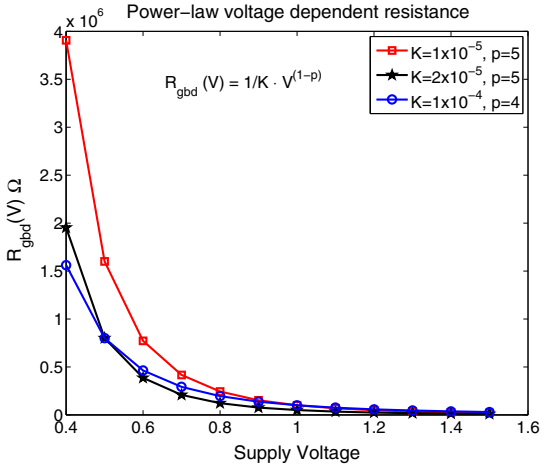


Fig. 6. Voltage dependent power-law resistance modeling oxide degradation

6, it can be observed that as the values of K and p increase, the value of $R_{gbd}(V)$ decreases. A smaller value of $R_{gbd}(V)$ signifies a larger gate oxide degradation. It can be observed from Figure 6 that as the voltage increases beyond 1V, the value of $R_{gbd}(V)$ falls sharply and becomes less than 100 KΩ which takes it into the realm of hard breakdown [5], [8], [12].

It has been shown in [7], [13] that the time to oxide breakdown in PMOS is an order of magnitude higher than in NMOS. Hence, in this work, we have focused on the oxide degradation in NMOS only. Since the probability of having more than one breakdown in an NMOS transistor is low [16], we consider either a gate-source breakdown or a gate-drain breakdown but not both. Figure 7 shows the possible GBD locations in the bit cell. The three categories of transistors in a bit cell are pull-down NMOS (PD), pull-up PMOS (PU) and pass-gate NMOS (PG). In Figure 7, the four resistances

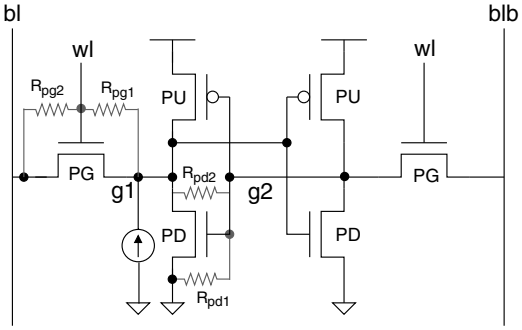


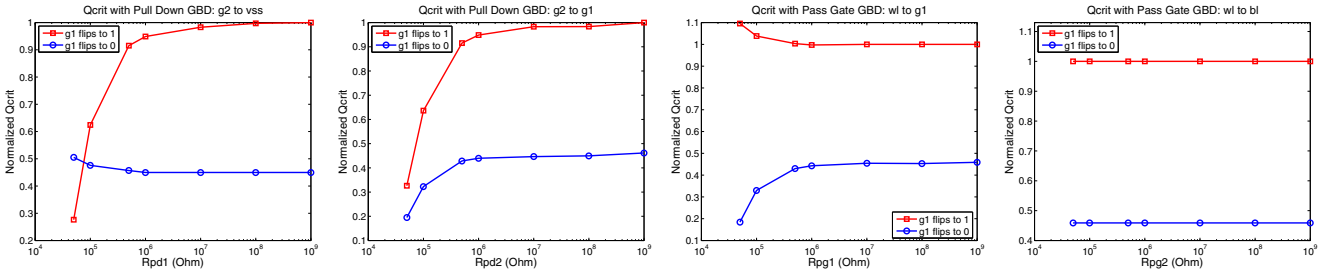
Fig. 7. Gate oxide breakdown locations in a bit cell and particle strike modeling by a current source

(R_{pd1} and R_{pd2}, R_{pg1} and R_{pg2}) denote the GBD locations in the PD and PG transistors respectively. However, the effect of each of these resistances on $Qcrit$ varies quite widely. For the case where a particle strikes at the node $g1$, Figure 8 shows the value of a 45nm bit cell $Qcrit$ as a function of each of the four resistances (two cases are considered - $g1$ flips to "1" and $g1$ flips to "0"). The idea is to understand the sensitivity of bit cell $Qcrit$ to various breakdown resistances at a fixed voltage. It can be noted from Figure 8 that the oxide degradation in the PG transistor does not alter the value of $Qcrit$ significantly. The oxide degradation in the PD transistor, however, drastically reduces the value of $Qcrit$ when $R_{gbd}(V)$ is in KΩs range. It is also interesting to note that $Qcrit$ shows a similar trend for both R_{pd1} and R_{pd2}. Hence, in this work, we analyzed the bit cell assuming that the gate oxide defect only exists in the gate-source of the PD transistor (R_{pd1}). Our observations from the analysis of R_{pd1} can be extended to oxide degradation in other transistors as well.

V. Soft Error Trend in Oxide Degraded SRAMs

Section III analyzes the trend of $Qcrit$ scaling with voltage. However, the analysis assumes that there is no degradation in the gate oxide. Section IV discusses the model of gate oxide degradation in nanoscale transistors. In this section, we analyze the impact of voltage scaling on the bit cell $Qcrit$ in the presence of gate oxide degradation. As shown in Figure 6, the value of gate breakdown resistance ($R_{gbd}(V)$) is a function of voltage and so is the bit cell $Qcrit$. Figure 9 plots $Qcrit$ against voltage for representative values of K and p for a 45nm bit cell. The data is normalized with respect to the value of 45nm $Qcrit$ at 1V for the bit cell with no oxide degradation.

The dotted line in Figure 9 is an asymptotic line depicting the case when there is no gate oxide degradation. As the oxide



(a) (b) (c) (d)

Fig. 8. Impact of gate oxide breakdown resistance on 45nm bit cell $Qcrit$ at 1V supply voltage (a) R_{pd1} (b) R_{pd2} (c) R_{pg1} (d) R_{pg2}

degrades, the value of $Qcrit$ becomes a non-linear function of the supply voltage. Even with oxide degradation, the value of $Qcrit$ scales similar to the asymptotic case for lower supply voltage. However, $Qcrit$ rolls-off at higher voltage and the

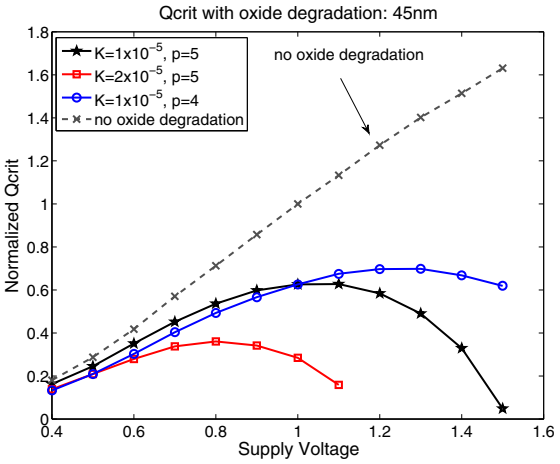


Fig. 9. $Qcrit$ scaling with supply voltage for 45nm bit cell

voltage at which the roll-off happens is a function of the level of degradation. Equation 4 shows the factor impacting the non-linear behavior of $Qcrit$ with respect to supply voltage.

$$Qcrit(V) = Qcrit_0 \cdot \left(\frac{V}{V_{nom}}\right)^{\alpha} \cdot A_{gbd}(V) \qquad (4)$$

The first term, $Qcrit_0$ is the $Qcrit$ of the bit cell at V_{nom} in the absence of oxide degradation. The second term, $\left(\frac{V}{V_{nom}}\right)^{\alpha}$, denotes the increase in $Qcrit$ with increasing supply voltage, where α is the sensitivity of $Qcrit$ to the supply voltage. The third term, $A_{gbd}(V)$, denotes the attenuation due to decrease in the gate breakdown resistance, $R_{gbd}(V)$ and is a function of the voltage. The trend due to the second and third terms can be observed in Figures 4(a) and 8(a) respectively. As the supply voltage increases initially, the second term dominates and the value of $Qcrit$ increases. However, as the voltage is further increased, the attenuation factor starts to dominate due to substantial increase in the gate leakage. Hence, there exists an optimal voltage (V_{opt}) at which the value of $Qcrit$ is maximized.

As explained above, there is an optimal supply voltage (V_{opt}) for each of the three representative levels of oxide degradation at which $Qcrit$ is maximized (Figure 9). The value of V_{opt} decreases, as the level of degradation increases. For the three cases shown in Figure 6, the values of V_{opt} are 1.25V (K = 1x10^{-5}, p = 4), 1.05V (K = 1x10^{-5}, p = 5) and 0.8V (K = 2x10^{-5}, p = 5). The value of $Qcrit$ at V_{opt} (called $Qcrit_{max}$) also changes with the level of oxide degradation. The normalized values of $Qcrit_{max}$ for the three cases mentioned above are 0.7, 0.62 and 0.35 respectively. To summarize, increasing levels of gate oxide degradation decreases both V_{opt} as well as $Qcrit_{max}$.

It is also crucial to understand the impact of technology node scaling on $Qcrit$ for a given level of gate oxide degradation. Figure 10 shows the impact of technology scaling on the trend of V_{opt}. The data in Figure 10 have been normalized with respect to the value of 65nm $Qcrit$ at 1V for the bit cell with no oxide degradation. The 45nm data (from Figure 9) have also been normalized to the 65nm data in Figure 10 to have an accurate comparison for understanding the technology trend. The level of gate oxide degradations shown in Figures 10(a), 10(b) and 10(c) are in increasing order of magnitude. The values of V_{opt} are shown by dashed lines. As the degradation increases, the $Qcrit$ curve decreases in magnitude and shifts to the left. Table I compares the values of V_{opt} and $Qcrit_{max}$ for 65nm and 45nm technology nodes. It is interesting to note how

Degradation level (low to high)	V_{opt} (V)			$Qcrit_{max}$		
	45nm	65nm	ratio	45nm	65nm	ratio
K=1x10^{-5}, p=4	1.25	1.35	0.92	0.525	0.75	0.70
K=1x10^{-5}, p=5	1.05	1.1	0.95	0.475	0.65	0.73
K=2x10^{-5}, p=5	0.8	0.8	1.0	0.275	0.375	0.73

TABLE I
IMPACT OF TECHNOLOGY SCALING ON V_{opt} AND $Qcrit_{max}$

the value of V_{opt} changes with technology node scaling. As the degradation increases, the absolute value of V_{opt} decreases (curves shift to the left in Figure 10) for both 65nm and 45nm processes. If the oxide degradation is substantial, the value of V_{opt} becomes independent of the technology node (as can be seen in Figure 10(c) where the V_{opt} becomes same for both 45nm and 65nm technology nodes).

The values of $Qcrit_{max}$ also change with technology node scaling, as can be observed in Figures 10(a), 10(b) and 10(c).

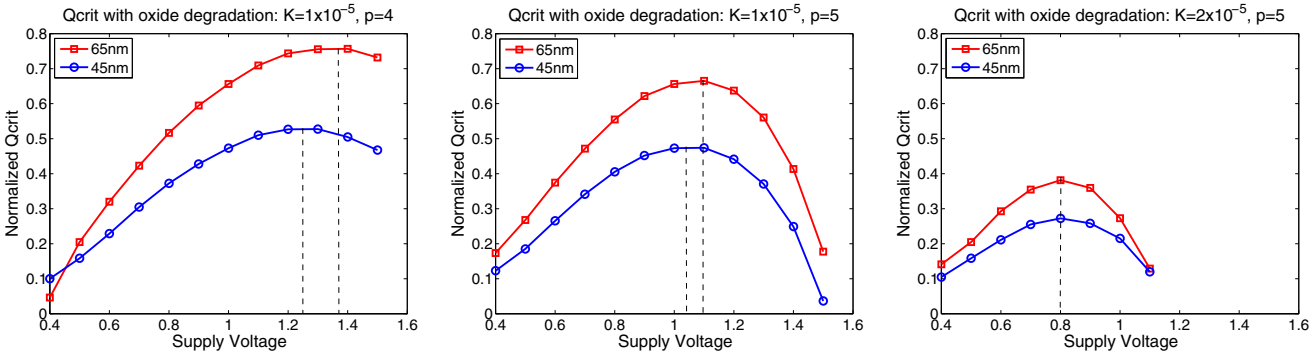


Fig. 10. Impact of technology scaling on $Qcrit$ in oxide degraded SRAMs (a) K = 1x10^{-5}, p = 4 (b) K = 1x10^{-5}, p = 5 (c) K = 2x10^{-5}, p = 5

The absolute value of $Qcrit_{max}$ decreases for both 65nm and 45nm nodes as the level of degradation increases (curves shift lower in Figure 10). However, the ratio of 45nm $Qcrit_{max}$ to 65nm $Qcrit_{max}$ remains fairly constant (Table I). It is also useful to note that the 45nm to 65nm ratio of $Qcrit_{max}$ is very close to the $Qcrit$ ratio shown in Figure 4(b) for a non oxide degraded SRAM. Both the ratios are $\sim$0.7, which is the technology scaling ratio between 45nm and 65nm nodes.

VI. Conclusions

As the technology node scales to sub-45nm, the effect of various reliability concerns become very crucial. Specifically, soft error susceptibility and gate oxide degradation are the two important reliability challenges for current and future generation SRAMs. In this work, we analyze the impact of supply voltage scaling on the soft error susceptibility of gate oxide degraded SRAMs. We show that, for a given oxide degradation level, there exists an optimal supply voltage (V_{opt}) at which the bit cell $Qcrit$ is maximized. In 45nm bulk CMOS SRAM, the value of V_{opt} is between 0.8V and 1.25V for representative levels of oxide degradation. We observed that the value of V_{opt} decreases with technology node scaling. Also, as the gate oxide degradation increases, the ratio of $Qcrit_{max}$ to $Qcrit$ decreases by up-to 65%. This ratio also becomes smaller as the technology node scales down. In a nutshell, gate oxide degradation significantly increases the susceptibility of soft error in voltage scaled nanoscale SRAMs. The values of V_{opt} and $Qcrit_{max}$ are a function of gate oxide properties and other technology parameters. Our future work will focus on developing an analytical model to predict the value of $Qcrit_{max}$ for a given supply voltage and oxide degradation parameters.

References

[1] R. C. Baumann, "Soft errors in advanced semiconductor devices - Part I: The three radiation sources," *IEEE Transactions Device and Materials Reliability*, vol. 1, no. 1 pp. 17-22, Mar 2001.

[2] E. H. Cannon *et al*, "The impact of aging effects and manufacturing variation on SRAM soft-error rate," *IEEE Transactions on Device and Materials Reliability*, Vol. 8, No. 1, pp. 145-152, Mar 2008.

[3] V. Chandra and R. Aitken, "Impact of Technology and Voltage Scaling on the Soft Error Susceptibility of Nanoscale CMOS," *IEEE Intl. Symposium on Defect and Fault Tolerance of VLSI Systems*, 2008.

[4] C. Dai *et al*, "Alpha-SER Modeling and Simulation for Sub-0.25μm CMOS Technology," *IEEE Symposium on VLSI Technology*, June 1999.

[5] R. Degraeve *et al*, "Relation between breakdown mode and breakdown location in short channel NMOSFETs and its impact on reliability specifications," *IRPS*, 2001.

[6] T. Heijmen, "Factors that Impact the Critical Charge of Memory Elements," *IEEE Intl. On-Line Testing Symposium (IOLTS)*, 2006.

[7] B. Kaczer *et al*, "Impact of MOSFET gate oxide breakdown on digital circuit operation and Reliability," *IEEE Transactions on Electron Devices*, Vol. 49, No. 3, pp. 500-506, Mar 2002.

[8] B. Kaczer *et al*, "Experimental verification of SRAM cell functionality after hard and soft gate oxide breakdowns," *ESSDERC*, 2003.

[9] A. J. KleinOsowski *et al*, "Modeling Single-Event Upsets in 65-nm Silicon-on-Insulator Semiconductor Devices," *IEEE Transactions on Nuclear Science*, Vol. 53. No. 6, pp. 3321-3328, Dec. 2006.

[10] H. Qin, Y. Cao, D. Markovic, A. Vladimirescu and J. Rabaey, "SRAM leakage suppression by minimizing standby supply voltage," *Intl. Symp. on Quality Electronic Design (ISQED)*, 2004.

[11] R. Rodriguez *et al*, "Oxide breakdown model and its impact on SRAM cell functionality," *Simulation of semiconductor processes and devices*, 2003.

[12] R. Rodriguez *et al*, "The impact of gate oxide breakdown on SRAM stability," *IEEE Electron Device Letters*, pp. 559-561, Sep. 2002.

[13] R. Rodriguez, J. H. Stathis, and B. P. Linder, "Model for Gate-Oxide Breakdown in CMOS Inverters," *IEEE Electron Device Letters*, Vol.24, No.2, pp.114-116, Feb. 2003.

[14] G. R. Srinivasan *et al*, "Accurate, Predictive Modeling of Soft Error Rate Due to Cosmic Rays and Chip Alpha Radiation," *IRPS*, 1994.

[15] J. H. Stathis, "Physical and predictive models of ultra thin oxide reliability in CMOS devices and circuits," *IRPS*, 2001.

[16] J. Sune and E. Y. Wu, "Statistics of successive breakdown events in gate oxides," *IEEE Electron Device Letters*, pp. 272-274, 2003.

[17] Y. Tosaka *et al*, "Impact of cosmic ray neutron induced soft errors on advanced CMOS circuits," *IEEE Symposium on VLSI Technology*, 1996.

[18] S. Walstra and C. Dai, "Circuit-Level Modeling of Soft Errors in Integrated Circuits," *IEEE Transactions on Device and Materials Reliability*, Vol. 5, No. 3, pp. 358-364, Sep. 2005.

[19] H. Wang, M. Miranda, F. Catthoor and W. Dehaene, "Impact of random soft oxide breakdown on SRAM energy/delay drift," *IEEE Transactions on Device and Materials Reliability*, pp. 581-591, Dec. 2007.

[20] J. Wang and B. Calhoun, "Canary replica feedback for near-DRV standby VDD scaling in a 90 nm SRAM", *CICC*, 2007.

[21] E. Wu *et al*, "Interplay of voltage and temperature acceleration of oxide breakdown for ultra-thin gate oxides," *Solid-State Electronics*, Vol.46, pp.1787-1798, 2002.

[22] E. Wu, and J. Sune, "Power-law voltage acceleration: A key element for ultra-thin gate oxide reliability," *Special issue of Microelectronics Reliability*, 2005.