On Linewidth-based Yield Analysis for Nanometer Lithography

Aswin Sreedhar and Sandip Kundu
Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, MA
Email: {asreedha, kundu} @ ecs.umass.edu

***Abstract*— Lithographic variability and its impact on printability is a major concern in today's semiconductor manufacturing process. To address sub-wavelength printability, a number of resolution enhancement techniques (RET) have been used. While RET techniques allow printing of sub-wavelength features, the feature width itself becomes highly sensitive to process parameters, which in turn detracts from yield due to small perturbations in manufacturing parameters. Yield loss is a function of random variables such as depth-of-focus and exposure dose. In this paper, we present a first order canonical dose/focus model that takes into account both the correlated and independent randomness of the effects of lithographic variation. A novel tile-based yield estimation technique for a given layout, based on a statistical model for process variability is presented. Another novel contribution of this paper is the computation of global and local line-yield probabilities. The key issues addressed in this paper are (i) layout error modeling, (ii) avoidance of mask simulation for chip layouts, (iii) avoidance of full Monte-Carlo simulation for variational lithography modeling, (iv) building a methodology for yield estimation based on existing commercial tools. Numerical results based on our approach are shown for 45nm ISCAS85 layouts.**

***Keywords*-Photolithography, depth-of-focus, exposure dose, focus-exposure matrix (FEM), chemical mechanical polishing, stratified sampling, linewidth-based yield.**

I. INTRODUCTION

Photolithography is the heart of the semiconductor manufacturing process. Sub-wavelength lithography is facing several critical challenges due to manufacturing limitations as the industry moves towards manufacturing end-of-the-roadmap CMOS devices. These challenges include printability issues, topographic changes due to metal planarization, overlay errors, random particle defects to name a few [4][10]. Although techniques such as Resolution Enhancement Techniques (RET) which involve optical proximity correction (OPC), phase shift masking (PSM), off-axis illumination (OAI) have been used to greatly improve the printability and the manufacturing process window, they cannot perfectly compensate for these lithographic deficiencies [1][2][4][5][12]. Process variations in sub-wavelength lithography such as optical defocus, and exposure dose variations can be spatial and random. Wafer tilting and metal planarization can lead to changes in depth-of-focus (DOF) and exposure dose.

The International Technology Roadmap for Semiconductors (ITRS) projects that variations in the lithographic process present an important challenge for both functional and parametric yield on current integrated circuit designs [3]. Across Chip Line width Variation (ACLV) is a direct impact of both layout topology and process variations. Figure 1. shows ACLV with change in exposure dose and focus. ACLV includes interconnect line width and poly gate length variation leading to both functional and parametric yield losses. Since profitability of a particular manufacturing process is directly related to its yield, estimating acceptable yield due to sensitivities in the lithographic process is of utmost importance for today's nanometer designs.

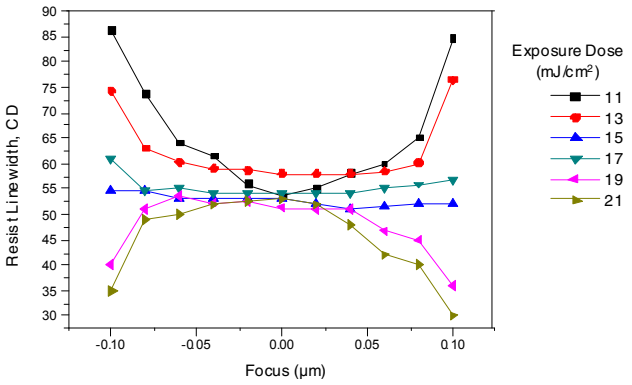

Figure 1. ACLV with defocus and exposure dose variation for Metal-1 lines in 45nm technology

Statistical approaches to yield prediction and yield modeling have been developed over a number of years [11][13][14]. These methods estimated functional and parametric yield of a design based on random particulate defect densities in the manufacturing process. For many generations, yield loss due to random defects has been well understood and thoroughly researched. But as technology scales, the influence of random defects from particulates has been in the decline compared to lithography and design related defects. Hence estimation of die yield based on lithographic sensitivities is a must for the current and future technology generations. A recent approach that models the impact of lithographic sensitivities on die yield was proposed by Sreedhar *et.al.* [17]. But the use of a half-width based linewidth estimation model considers a smaller optical diameter where the impact of a line is limited to its immediate neighbor and also it does not take correlations in manufacturing parameters between neighboring lines into account.

In this paper, we attempt to model the variations of sub-wavelength lithographic exposure process and estimate the acceptable yield. Our lithographic analysis shows good

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correlation with PROLITH yield results for different sample layout regions. The contributions of this paper include,

- A first order canonical model to estimate focus and dose variation. The model takes both global and local correlations of die focus and dose into account.
- Provide a novel linewidth-limited yield estimation technique to estimate linewidth yield. The model uses a zone or stratified sampling based approach to estimate the line printability distribution.
- Layout specific estimation of yield for each metal layer and hence the design yield.

The rest of the paper is arranged as follows. Section II provides some preliminaries and the canonical model for dose and focus variation. Our post-OPC yield estimation methodology is discussed in Section III. Test designs used and experimental results using our framework are presented in section IV followed by conclusion and future improvements in section V.

II. MODELING LITHOGRAPHIC VARIATION

Across Chip Linewidth Variation (ACLV) is the most significant contributor towards chip leakage and timing variability. ACLV is dependent both on process and layout topology. Sources of ACLV include optical defocus, exposure dose variations, pitch variations, resist thickness, lens aberration etc.

Focus and exposure dose variation are the two most important sources which are random in nature and are hard to control. All other source of errors can be lumped into these two sources equivalently [4]. Based on the above discussion, it is observed that linewidth variation due to lithographic sensitivities is a significant concern. Such variations affect performance and power of a design and hence have to be estimated.

A. Canonical Model

Focus and Dose variation are expressed in the canonical form shown below. The coefficients of the different sources of global and local variations are obtained as a part of the lithographic technology characterization process.

$$F = f_0 + \sum_{i=1}^{n} s_{fi}\Delta Z_i \quad (1)$$

$$D = d_0 + \sum_{i=1}^{n} s_{di}\Delta Z_i \quad (2)$$

Where, f_0 and d_0 are the random nominal values for dose and focus obtained for a particular simulation setting. Whereas ΔZ_i i=0….,n. represents different sources of lithographic variation. Coefficients S_{fi} and S_{di} represent the sensitivities of each source of variation. Such sensitivities can be modeled based on foundry data. The two sources of variation that are discussed in this paper and used in our methodology are resist thickness variation due to CMP polishing and wafer tilt.

B. Impact of Pattern density and Wafer Tilt

Chemical Mechanical Polishing (CMP) is a method used for planarization of the wafer surface. It involves the use of polishing pad and an abrasive material. Erosion of material over the entire wafer and dishing at low pattern density regions are common problems caused by improper planarization [6]. As reported in previous research works and also by a simple visual inspection, the pattern density in the underlying metal layer is a key factor affecting CMP metal planarization. Hence the final resist thickness after planarization can be approximated as a function of underlying metal pattern density. Stine et. al. [7] showed that there exists a relationship between the interaction distance and inter-layer dielectric (ILD) thickness. Interaction distance was defined as the region over which the pattern density is estimated. We follow the same methodology in this paper.

In this paper we take the interaction distance to be 3 times that optical diameter (~3μm). There have been various methods investigated for layout density calculation [6][8][9]. We follow a floating window based density estimation technique. The density analysis window is slid over the layout to find the pattern density over different regions. The regions are made to overlap so that the density effects on each metal interconnect is estimated correctly (Figure 2.). The density value in region is compared with an appropriate resist thickness value from a pre-computed table. This table has been created after multiple simulation runs with different density values across different metal layers. Change in resist thickness corresponds to change in focus and dose in that region.

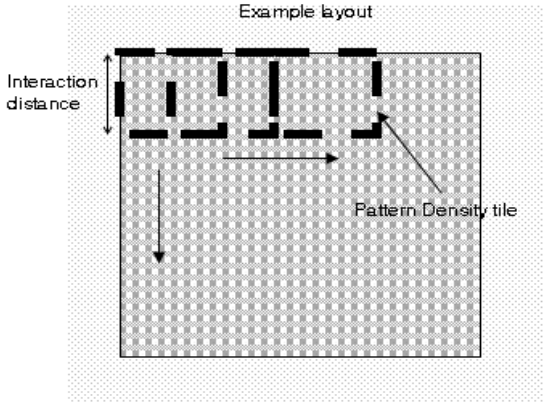

Figure 2. Example layout for pattern density measurement

Wafer tilt is defined as a possible unparallel position of the wafer during the resist coat, bake and exposure process. Similarly, this leads to variation in resist thickness for the exposure process. We model this impact on dose and focus as a random gradient that extends across the wafer. The tilt is a simple linear function of die position over the wafer plane. The above two variations are multiplied with their sensitivities and added to the nominal value to obtain the focus and dose of the line segment under consideration (Eq (1) and (2)).

C. Process parameter variation using Stratified sampling

In order to better understand the effect of random manufacturing process variations on metal linewidth, a joint

analysis is required. However, line width is not a linear function of control variables and a multivariate analysis of variation of process parameters is required to obtain line width distribution. One way to perform this analysis is Monte Carlo simulation.

Monte Carlo based analysis can be used to deduce the effect of such variations by performing repeated aerial imaging simulation [14]. It is also well known that aerial imaging simulations of layout features is compute intensive and slow [1]. To address this problem we have adopted a stratified sampling strategy. Stratified sampling has been used in varied number of applications in statistical analysis domain [15]. It has been proven that this technique does a simple, reasonably accurate and efficient sampling of the data such that entire distribution is represented by the samples from different regions. This technique reduces the number of simulations to obtain linewidth distribution, thus reducing the computational needs.

In our approach, we aim at dividing the input parameter distribution space into different strata/zones [16]. The strata are regions over which the parameter variation is not more than 0.25σ. To form the look-up table, certain number of points is chosen from each zone and lithography simulation is performed at those parametric values. In order to see the impact of changes in both exposure dose and focus, the resist profile value is obtained at each simulation point. A look-up table is created with all the sampled value and their respective linewidth value at each metal layer. This table is used to predict the yield for each metal line and hence the metal layer.

III. LINEWIDTH-BASED YIELD PREDICTION METHODOLOGY

In this section we present our linewidth variation-limited yield prediction methodology with an overview of the experimental approach & analysis.

A. *Methodology*

Figure 3. shows our experimental methodology to estimate the yield due to different sources of variations in today's lithographic manufacturing process. The analysis involves estimating the probability if a metal line will not result in an open or a short. This probability can hence be used to predict the yield of that metal layer for the die. The following sections give a detailed description of our methodology.

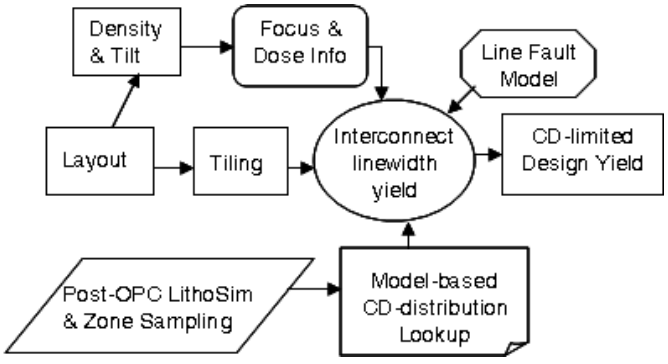

Figure 3. Post-litho linewidth-limited Yield estimation mathodology

B. *Layout Tiling and TileMminimization*

Layout tiling process can be explained as follows. Each metal interconnect is divided into segments of fixed size (~6λ). Around each segment a region of width equal to the optical diameter is considered to be a tile. The tile symbolizes the region of impact of other structures due to lithographic variation on the segment under consideration.

Yield analysis is performed on each tile and the segment yield is obtained using the scheme described in the following sections. Since today's designs have high metal density, the number of such segment tile will exponentially increase with the design size. Hence in order to minimize the number of tile simulated for yield estimation, tile comparison is performed.

Segment tiles are converted into two dimensional matrices as shown in Figure 4. (a). Each segment tile as and when created is compared to the already present set of tiles. Comparisons are done with flipped, rotated and reflected versions of the current tile. Figure 4. (b) shows en example of this minimization method. This method of tile matching is the key to minimization of the total number of tiles needed to simulate. The set of tiles that are to be simulated are called distinct tiles.

Based on our simulation, the total number of tiles reduced by 95% when the tile size used was around the optical diameter. The reduction is more if the tile size goes down. For 45nm ISCAS85 c432 circuit, the total tile number is 49141 and the total distinct tiles are 2569 (TABLE I.). Key point to note is only tiles of similar metal layers are used for comparison. Segment yield estimation is performed on distinct tiles as explained in the following section.

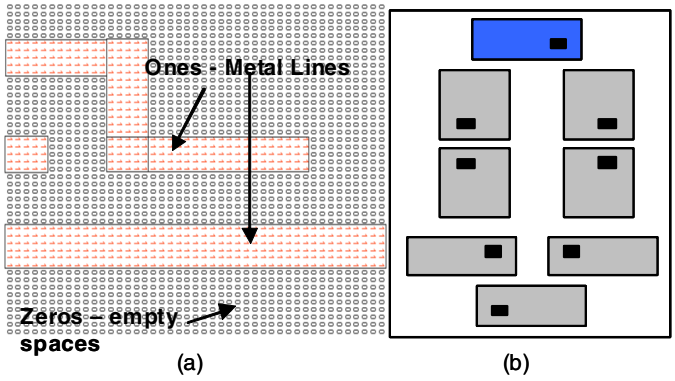

Figure 4. (a) Segment tile represented in matrix format. (b) Original blue tile and its rotated and reflected forms represent by grey tiles.

C. *Variation-Aware Linewidth limited yield*

Metal line yield depends on three different factors as listed below,

- Post-etch linewidth distribution
- Averaged LER amplitude & period

Linewidth-limited yield is estimated in two parts. The first part is to find the probability of not having an open or short; where we take post-etch line edge roughness into account. The

second part is to include the effect of line-edge roughness (LER) variability on final line yield. LER is defined as the perturbation of pattern line edge caused by photolithography and etching process. To find the metal linewidth probability, the layout fault is modeled as follows.

1) Line Fault Modeling

Consider the metal lines shown in Figure 5. The post-litho linewidth ($LW_{post\text{-}etch}$) is either smaller or larger than the expected linewidth (LW_{ideal}) due to proximity effects. The line edge roughness effects on both sides of the metal line have to be included while defining the fault model. LER in this case is averaged and is assumed to be constant, irrespective of the length of the line. This assumption is just for defining line OPEN and SHORT conditions. The periodicity of LER will be used later to compute the metal line segment yield.

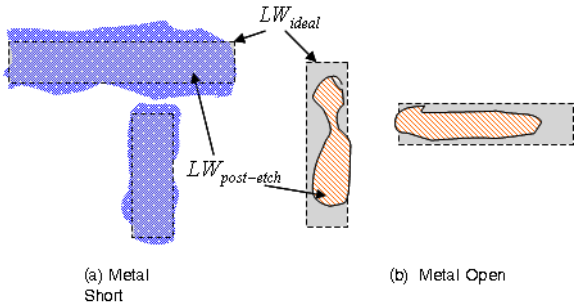

Figure 5. Line fault Modeling (a) Metal Line SHORT, (b) Metal Line OPEN

The condition required for constriction in linewidth leading to an open is given as follows,

$$LW_{ideal} - LW_{post-etch} - W_{LERTot} \le 0.3 * LW_{ideal} \quad (3)$$

$$LW_{jut\,S_1,S_2} = LW_{post-etch} - LW_{ideal} \ldots \forall M_{layer} \quad (4)$$

$$LW_{jut_{S_1,S_2}} - W_{LERTot} \le Spacing \quad (5)$$

Similarly, the condition when the lithographic process can lead to a bridge between two adjacent lines at nominal spacing is described. LW_{ideal} is the ideal/expected linewidth for the current lithography process, otherwise termed as mask CD. $LW_{post\text{-}etch}$ is the obtained linewidth after etch process with variations. M_{layer} is the metal layer ranging from 1 to 10 or 12 depending on the process. LW_{jutS1} and LW_{jutS2} denote the protrusions on either side of a metal line. W_{LERTot} is the total constant LER width and Spacing is the edge to edge distance between two adjacent metal lines. In this case spacing is the limit to which two adjacent lines can expand and not bridge.

2) Line Edge Roughness (LER) variability

LER was assumed to be constant in the above line fault model. In reality, LER is not constant and it varies with different periods along the length of the line. To estimate the effect of LER on line yield, we use the results obtained by Shibata *et.al.* [10]. Figure 6. shows the probability $P_{\lambda i}$ of LER at different periods λ_i. This data shown was obtained through measurement with a top-down scanning electron microscope (SEM).

In presence of LER, the yield of an infinitely long line will be 0. Hence, for a short line, the probability of having an open or bridging is less compared to a long line. Thus we can deduce that the line failure probability is an exponential function dependant on line length l. This is given by,

$$Line Failure\ \Pr obability\ P_f(l) = \exp\left(-a\sum {l_i}/{\lambda_i}\right) \quad (6)$$

Where, a is a manufacturing process parameter to be obtained from correlating with observed data. LER has both amplitude and frequency. Since this is not fixed amplitude, the likelihood of open or shorts will depend on the number of crests and troughs of the LER [17]. If a line is infinitely long and the worst case LER amplitude can cause a line failure, the probability of failure of the line will be 1. However, for a shorter line, this probability will be less than 1.

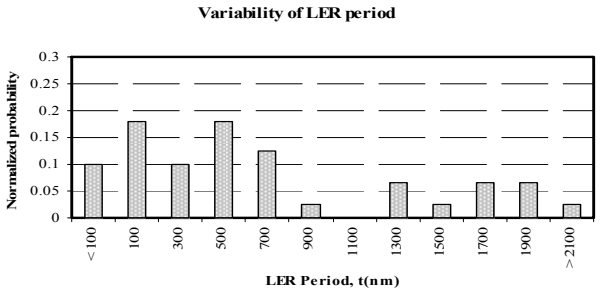

Figure 6. Distribution of LER periods obtained from autocorrelation function for various LER conditions [7]

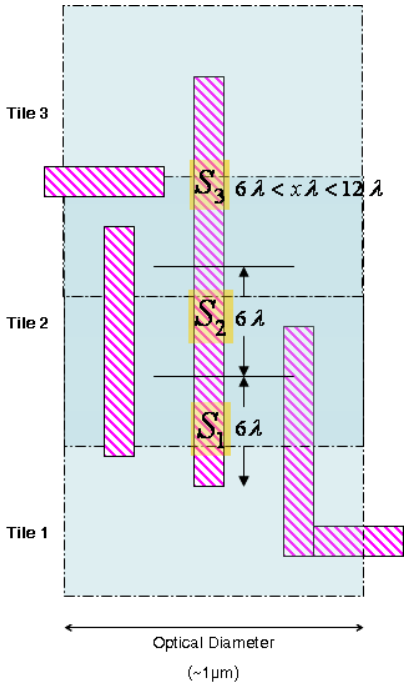

Figure 7. Metal line of length l with different segments

3) Linewidth Yield

Consider the line shown in Figure 7. consisting of different segments S_i. If the line segments are each of length 6λ or little longer, then the sum of all the segment lengths must be the total length of the line $l = \sum l_i$ .The probability of line *l* being

printable can be given as the product of the probabilities of each segment. The probability of each metal layer depends on the line probability and the length of the line and LER period. Since longer lines have more probability of having a fault, it is modeled as an exponential function shown below.

$$P_{line} = \prod_{n} P_{seg}$$

$$Þ_{MLayer} = \sum_{i} Þ_{\lambda_i}\left(1 - e^{-al/\lambda_i}\right)$$

Once the probability of failure for an individual metal layer is obtained, it can be used in turn to compute design yield.

$$\ddot{Y}(Design\ ) = \prod_{i} Þ(MLayer\ _i)$$

$$\log \ddot{Y}(Design\ ) = \sum_{i} \log\left[Þ(MLayer\ _i)\right]$$

Hence it can be seen that to obtain a very high yield, the probability of having an open or short should be very low.

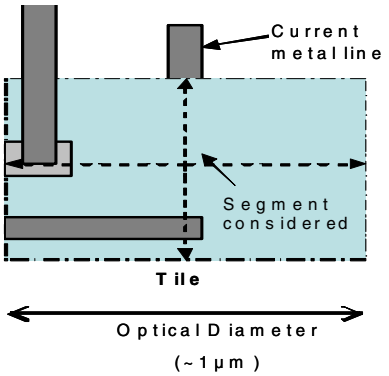

Figure 8. Segment tile for a region of interconnect metal line.

IV. EXPERIMENTATION & RESULTS

In this section, we test our approach for various designs using leading-edge industry tools, and estimate the linewidth-limited yield.

The results reported here are based on 45nm cell library available freely from NCSU. Layout of ISCAS85 circuits in 45nm technology were obtained using Cadence Encounter tool. Then the layouts were converted into a simplified netlist format using Capo from University of Michigan. The yield estimation tool reported here was coded in C++ to run directly off of Capo generated netlist. The steps in the yield estimation procedure are described next.

Pattern density calculation - As shown in section II.B, the design is divided into multiple overlapping cells to estimate the change in resist thickness due to pattern density and hence the dose & focus. At the end of this density calculation Stine model is used to translate density to topographical change to compute change in focus in a given region.

Segmentation, Tile creation & Minimization - Each metal line in the netlist is divided into contiguous segments. A tile is created around each segment as shown in Figure 8. The dimensions of the tile is based on the optical diameter defined as the region within which optical diffraction patterns of neighboring features will have an impact on this segment. Since we use a 193nm wavelength for light source, a square tile was used where each side is ~1µm. Tiles are minimized as explained in section II.B and listed in TABLE I.

Wafer tilt calculation - Since wafer tilt is a random component, its effect on the focus and dose of each tile is calculated during run time. Change in focus due to tilt are correlated. Thus, tilt is a single statistical parameter for the entire wafer.

Computation of Segment yield - In the next step yield of each segment is computed using a statistical simulation. The mean value of the focus is based on topography calculation defined in the first step of yield estimation above using canonical formula defined in section II.A and wafer tilt. The statistical litho simulation, results in line widths which are converted into yield based on formulae defined in section III.C where we elaborated how the line fault model that takes LER into account. The litho simulation was performed using Prolith™, a commercial tool from KLA-Tencor Corp. The LER information was based on results reported in [10].

Algorithm: Design Yield Estimation

1: **forall** metal lines n,
2: **foreach** segment k of length l
3: create tiles for segment k
4: f = Focus(density,tilt);
5: d= Dose(density,tilt);
5: $LW_{post\text{-}etch}$ = CD from model based lookup table
6: Segment yield $\ddot{Y}_{seg}$ = f($LW_{post\text{-}etch}$,LW_{ideal})
7: Line probability $Þ_{line} \leftarrow \ddot{Y}_{sg1} * \ddot{Y}_{sg2}$……
8: **foreach** metal layer $m_i \in$ design
9: Metal Yield = $Þ_{L1} * Þ_{L2} * Þ_{L3}$……. $* Þ_{Ln}$
10: ***Design Yield*** = $\ddot{Y}_{M1} * \ddot{Y}_{M2}$….. $* \ddot{Y}_{M6}$

A pseudo-code used in the design yield estimation methodology is given above. The assumptions on process parameters were based on ITRS specification that the acceptable variation of both dose and focus is ±10%. This is the case when the process is within the FEM window. ITRS reports that the line edge roughness of a line is approximately 5nm [3]. Then, for a reasonably long line of nominal width 10nm or below an open fault is very likely to occur (corresponding to erosion from both edges of 5nm each).

TABLE I. TILE MINIMIZATION RESULTS

ISCAS85 Design	Total Tiles	Distinct Tiles
c432	49141	2569
c1908	69750	4696
c1355	60073	4003
c6288	185488	8839

TABLE II. shows the linewidth-limited yield for different ISCAS85 circuits. The yield is a joint function of the line spacing and variations. It is observed that the yield for

comparable metal layers goes down as the circuit size increases. This follows an intuitive pattern.

TABLE II. TILE MINIMIZATION RESULTS

ISCAS85 Design	Yield
c432	0.99901
c880	0.99926
c1355	0.99393
c1908	0.99355
c6288	0.98941

V. CONCLUSION

We proposed a novel linewidth-based yield estimation technique for a given layout, based on a statistical model for process variability. A commercial lithography simulation tool was used to estimate the linewidth distribution for multi-dimensional input parameter variations. The impact of pattern density and wafer tilt were considered. Stratified sampling was used to reduce the number of samples to be simulated to obtain tail of the distribution. Linewidth distribution and LER periodicity was used to compute probability of failure of a line, which then was used to compute yield of a metal layer and finally the chip. The results based on the proposed yield model shows that when layouts are scaled in geometric proportion and when process parameters vary, the yield decreases drastically.

ACKNOWLEDGMENT

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