Sizing Rules for Bipolar Analog Circuit Design

Tobias Massier Helmut Graeb Ulf Schlichtmann
Institute for Electronic Design Automation
Technische Universitaet Muenchen

Abstract

This paper presents sizing rules for basic building blocks in analog bipolar circuit design. Sizing rules efficiently capture design knowledge on the technology-specific level of transistor-pair groups. This reduces the effort for and improves the resulting quality of analog circuit synthesis. We present a hierarchical library of transistor-pair groups as basic building blocks for analog bipolar circuits. Sizing rules are constraints associated to these building blocks that must be satisfied to guarantee the function and robustness of each block. Results of applications like circuit sizing or design centering show that the use of sizing rules leads to improved and robust results.

1. Introduction

Analog components are essential in modern integrated systems: certainly in mixed-signal systems, but also as vital parts in digital systems, for instance power-on reset, pad driving, or clock generation. But since design automation for analog circuits is still much less developed than for digital circuits, they often are the bottleneck in the design flow.

Analog synthesis is complicated because it incorporates topology and layout synthesis, component sizing, and in addition, physical effects like variation of process parameters or operating conditions, matching constraints, or noise. It is important not to just specify circuit performance bounds, like for DC gain, power supply rejection ratio, or phase margin, but also ranges for transistor geometry or voltages at transistors (e.g., to ensure a certain operating region for transistors). These additional constraints are called sizing rules. A circuit in which sizing rules are violated might perform fine in the nominal case, but is more sensitive to process and operating variations as well as to noise [1].

Sizing rules are well-known and used in many analog sizing methods for CMOS [1–4]. A first approach that presented a detailed construction of such sizing rules for CMOS transistors and an algorithm for the detection of CMOS building blocks based on transistor pairs was presented in [5]. In the following, sizing rules for bipolar transistor circuits are presented. Bipolar transistors are of importance in analog design, e.g., for high speed or high power design [6, 7]. Applications to circuit sizing and design centering presented in Section 4 show that sizing rules for CMOS and bipolar transistors lead to robust designs.

Sizing rules are formulated as equality or inequality constraints for transistor geometry parameters (transistor width, length, area) and for electrical transistor quantities (e.g., transistor collector-emitter voltage). They can be checked during simulation-based analog synthesis without simulation overhead. Sizing rules represent an optimal compromise between design performance (e.g., gain) and process yield. In particular, sizing rules guarantee the proper function of a building block and its robustness, e.g., towards mismatch or Early effect.

The rest of this paper is organized as follows: Section 2 develops a hierarchical library of basic building blocks on transistor-pair level for bipolar technology. In Section 3, sizing rules for bipolar transistor building blocks according to functional and robustness constraints are presented. In Section 4, results and applications are shown. Section 5 concludes the paper.

2. Hierarchical Bipolar Building Block Library

In [5], a hierarchical library for CMOS transistor building blocks, as well as an algorithm for the recognition of building blocks in a circuit was presented. Fig. 2 presents a hierarchical library of basic building blocks for bipolar transistor technology. A hierarchical library is a strictly ordered set which can be divided into subsets that represent a hierarchical level each. The elements on each hierarchy level from 1 upwards consist of elements from lower hierarchy levels. For example, a cascode current mirror on level 2 consists of two building blocks from hierarchy level 1, i.e., a level shifter and a simple current mirror. A Wilson current mirror on level 2 consists of one building block from hierarchy level 1 (a simple current mirror) and a single transistor from level 0. The numbers in parentheses next to the building blocks on hierarchy level 1 are referred to in Section 3 when transistor 1 or 2 of a building block is mentioned.

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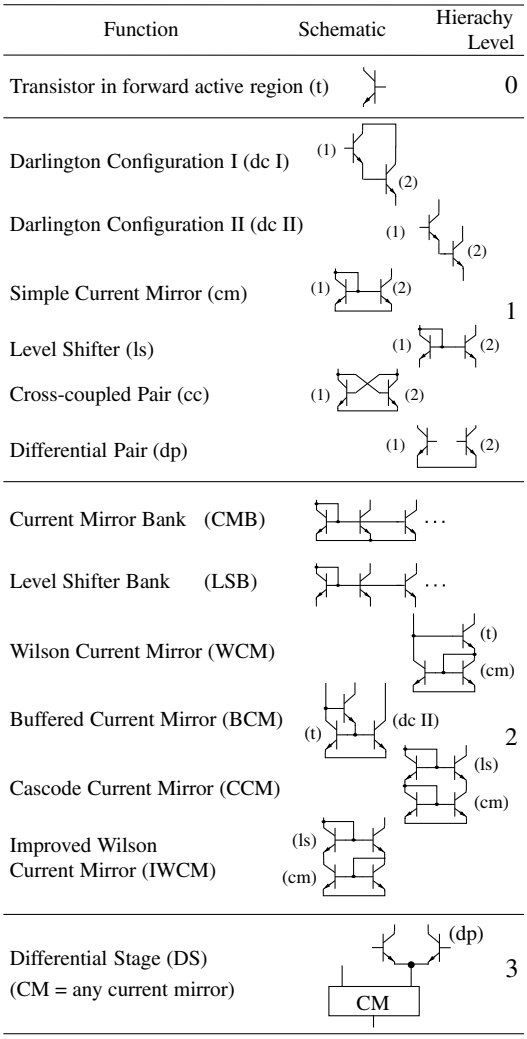

Figure 1. Hierarchical library of basic bipolar building blocks (npn)

Resistors are often added to the emitter terminals of transistors, e.g., a simple current mirror with a resistor added to the right transistor is called a Widlar current mirror. These building blocks are not shown and a transistor with a resistor connected to its emitter is treated as a single circuit element, since the basic structure is still the same.
In this sense, the list of transistor pairs on level 1 is complete. Of course, a range of further building blocks above level 1 could be included.

Block schematics and sizing rules are given for the npn-part and hold analogously for the pnp-part. Due to the hierarchical structure of the library, building blocks on higher hierarchy levels inherit the sizing rules of the blocks they consist of. In addition, they bring about additional rules. In Section 3, sizing rules for bipolar transistor building blocks will be introduced.

Various methods for subcircuit recognition were developed in the past years. For instance, Subislands [8] is an optimization-based method. It combines a graph labeling algorithm and the so-called graduated assignment technique to calculate match probabilities. In FROSTY [9], gate structures are recognized first. Afterwards, graphs incorporating this information are constructed, before a pattern matching algorithm is applied. In [10], a graph coding algorithm based on a technology file is used. The Sizing Rules Method [5] includes a library of CMOS building blocks based on transistor pairs and pairs of pairs. A given circuit is then searched for the given library elements. Finally, a list of all sizing rules for a circuit is set up, based on the recognition result. By extending the library with the bipolar building blocks given in Fig. 2, this algorithm can be used without further adjustments.

3. Bipolar Sizing Rules

In this section, sizing rules for bipolar transistor building blocks will be derived. All sizing rules will be presented for npn-transistors but hold analogously for pnp-transistors. Each sizing rule will be labeled as follows: Label *F* refers to function, *R* to robustness, *E* to an electrical property, and *G* to a geometric property. For instance, *FE* refers to an electrical sizing rule concerning function.

In [11], the collector current of a bipolar transistor is given by

$$i_c \;=\; I_S e^{\frac{v_{be}}{V_T}} \left(1 + \frac{v_{ce}}{V_A}\right). \tag{1}$$

Here, $V_T = \frac{k_B T}{q_0}$ is the thermal voltage with k_B being the Boltzmann constant, T the room temperature and q_0 the electron charge, and V_A is the Early Voltage. The saturation current is denoted by I_S. It depends on the transistor area A. The transistor area is the design parameter in bipolar transistor technology. Instead of scaling transistors, it is recommended to use identical transistors for each building block and to connect transistors in parallel, e.g., to produce a certain current ratio. The number of transistors connected in parallel will be denoted by N in the following. The values of all constants are technology-specific.

In contrast to CMOS transistors whose gate current usually can be neglected, the base current of a bipolar transistor has to be considered. The forward current gain β is given by

$$\beta \;=\; \frac{i_c}{i_b}. \tag{2}$$

The value of β depends on v_{be} [12]. Fig. 2 illustrates this. For all presented building blocks, $\beta = \beta_{max}$ has to be fulfilled. This is only the case if v_{be} stays in a range bounded by the constants $V_{be_{min}}$ and $V_{be_{max}}$ where the slope of i_c is equal to that of i_b. This leads to the following additional sizing rule for all presented bipolar transistor building blocks:

$$RE: \quad V_{be_{min}} \;\leq\; v_{be} \;\leq\; V_{be_{max}} \tag{3}$$

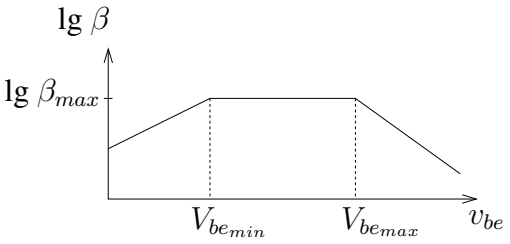

Figure 2. lg β over v_{be} for a bipolar transistor [12]

3.1 Building Blocks on Hierarchy Level 0

Transistor in forward active region

All transistors contained in the library in Fig. 2 have to operate in the forward active region. Hence, the following sizing rules have to be fulfilled:

$$FE1: \quad v_{be} \geq V_{be_0} \tag{4}$$

$$FE2: \quad v_{ce} - v_{be} \geq V_{ce_{sat}} \tag{5}$$

Usually, V_{be_0} is larger than $V_{be_{min}}$ in (3), so that the left inequality in (3) can be omitted.

3.2 Building Blocks on Hierarchy Level 1

3.2.1 Simple Current Mirror

A simple current mirror produces a constant ratio between the collector currents which depends on the ratio of the transistor areas which can be adjusted by the ratio between the number of transistors connected in parallel, which is denoted by N_2/N_1:

$$\frac{i_{c_2}}{i_{c_1}} = \frac{A_2}{A_1} = \frac{N_2}{N_1}. \tag{6}$$

Since the current through the base terminals is not zero, the collector currents are smaller than the overall current I_0 flowing into the left branch of the current mirror. Applying Kirchhoff's current law at the common base and assuming that $i_{c_1} = i_{c_2}$ with $A_1 = A_2$, we obtain that i_{c_2}/I_0 diminishes with decreasing β.

$$\frac{i_{c_2}}{I_0} = \frac{1}{1 + \frac{2}{\beta}} \tag{7}$$

To keep this error small, β has to be maximal, hence (3) has to be fulfilled. The assumption $i_{c_1} = i_{c_2}$ only holds if both transistors are identical and their collector-emitter voltages do not differ too much. Therefore, the following additional sizing rule has to be fulfilled.

$$FE: \quad |v_{ce_2} - v_{ce_1}| \leq \Delta V_{ce_{max_{cm}}} \tag{8}$$

Adding a resistor at one or both of the transistors' emitter terminals changes i_{c_2}/I_0, but the sizing rules are unchanged. It is only necessary to replace v_{ce_i} with $(v_{ce_i} + v_{R_i})$ in (8).

3.2.2 Level Shifter

The function of this presented building block is to provide a constant differential voltage between – or equal voltages at – the two transistors' emitter terminals. Both transistors have to operate in forward active region and the β of both transistors has to be maximal, thus (3) has to be fulfilled. The difference of the collector-emitter voltages has little effect on the function of this building block, as long as both transistors do not leave the forward active region. Additional rules apply, when a level shifter is part of a larger current mirror.

3.2.3 Differential Pair

The function of a differential pair is to produce a constant difference $\Delta i_c = |i_{c_1} - i_{c_2}|$ in the collector currents dependent on the base-emitter voltages of the two identical transistors:

$$\Delta i_c = I_S \left| e^{\frac{v_{be_1}}{V_T}} (1 + \frac{v_{ce_1}}{V_A}) - e^{\frac{v_{be_2}}{V_T}} (1 + \frac{v_{ce_2}}{V_A}) \right| \tag{9}$$

To keep the base currents low, both transistors have to operate in forward active region and their β has to be maximal, thus (3) has to be fulfilled. For symmetry reasons, the number of transistors in parallel on both sides has to be the same. From (9), it can be seen that the difference of the collector-emitter voltages must be small to reduce the impact of the Early effect. To ensure linearity, the difference of the base-emitter-voltages has to be small as well. This leads to the following additional sizing rules for a bipolar differential pair:

$$FG: \quad N_1 = N_2 \tag{10}$$

$$FE: \quad |v_{ce_2} - v_{ce_1}| \leq \Delta V_{ce_{max_{dp}}} \tag{11}$$

$$RE: \quad |v_{be_2} - v_{be_1}| \leq \Delta V_{be_{max_{dp}}} \tag{12}$$

However, the region where Δi_c changes linearly with Δv_{be} is very small. Indeed, it's much smaller than in a CMOS differential pair. Thus, even a relatively small difference between the base-emitter-voltages can cause one of the transistors to switch off. To remedy this, resistors can be added at the transistors' emitter terminals. Fig. 3.2.3 shows the normalized difference between the collector currents against the difference of the base-emitter voltages for different values of $R_e \cdot I_0$, based on simulation results, whereas R_e is the value of the resistors connected to the emitter terminals and I_0 the value of the current flowing into the common-emitter.
The value of $V_{be_{max_{dp}}}$ in (12) depends on the value of R_e (see Fig. 3.2.3).

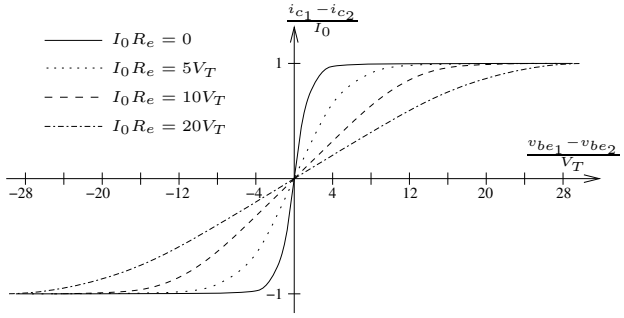

Figure 3. Normalized difference of collector currents over the difference of base-emitter voltages in a bipolar differential pair

3.2.4 Darlington Configuration I / II

In these configurations, which are also called Darlington pair, both transistors have to operate in forward active region and for both, β has to be maximal.

3.2.5 Cross-Coupled Pair

This building block is often used in VCOs as a negative resistance. Due to symmetry reasons, the number of transistors connected in parallel on both sides has to be the same and all transistors have to be identical.

$$FG: \quad N_1 = N_2 \tag{13}$$

3.3 Building Blocks on Hierarchy Level 2

3.3.1 Buffered Current Mirror

A Buffered current mirror is a modification of a single current mirror to reduce the i_{c_2}/I_0-error caused by the base current. In a buffered current mirror, this error is proportional to only $1/\beta^2$. We modeled this building block as a combination of a Darlington configuration II and a single transistor. For the lower two transistors, the sizing rules for a simple current mirror apply. The third transistor has to operate in forward active region and (3) has to be fulfilled.

3.3.2 Cascode Current Mirror

A cascode current mirror, which consists of a simple current mirror and a level shifter, has a higher output impedance than a simple current mirror. The level shifter provides equal voltages at its emitter terminals to produce equal collector-emitter voltages at the simple current mirror's transistors. Thus, in addition to the sizing rules of this building block's sub-blocks, the number of transistors in parallel in the level shifter has to be the same as in the simple current mirror, which leads to the following additional sizing rules:

$$FG1: \quad N_{ls(1)} = N_{cm(1)} \tag{14}$$
$$FG2: \quad N_{ls(2)} = N_{cm(2)} \tag{15}$$

3.3.3 Wilson Current Mirror

Like the cascode current mirror, this building block has a higher output impedance than a simple current mirror. For the lower two transistors, the rules for a simple current mirror apply, but the roles of driving and driven transistor are reversed. The third transistor has to operate in forward active region, (3) has to be fulfilled and the number of devices connected in parallel has to be the same as for transistor 1 of the simple current mirror.

$$FG: \quad N_{cm(1)} = N_3 \tag{16}$$

3.3.4 Improved Wilson Current Mirror

To reduce the v_{ce}-mismatch in a Wilson current mirror, a fourth transistor can be added. Since this building block consists of the same building blocks as a cascode current mirror, the sizing rules are exactly the same. The current ratio is the same as for the Wilson current mirror.

3.4 Building Blocks on Hierarchy Level 3

Differential Stage

A differential stage consists of an arbitrary current mirror and a differential pair. It does not produce any new sizing rules, but it assures that the two transistors connected solely via their emitter terminals are intended to operate as a differential pair, so that the corresponding sizing rules apply.

4. Results and Applications

4.1 Sizing Rules

We examined two BiCMOS and two bipolar operational amplifiers. A simple BiCMOS operational amplifier (see Fig. 4) will be used to illustrate the importance of sizing rules for bipolar and CMOS building blocks for automatic circuit sizing. To identify all building blocks in the given circuits, the recognition algorithm in [5] was used. All detected building blocks of the OpAmp have been shaded. Table 1 summarizes the number of detected building blocks on the different levels of hierarchy for this OpAmp, as well as for the other circuits examined. Table 2 shows the total number of sizing rules for each of the circuits. Although the list of generic sizing rules is rather small, the overall number of sizing rules for each examined circuit is quite large.

The inequality part of sizing rules has to be satisfied during the design process. The equality part of sizing rules

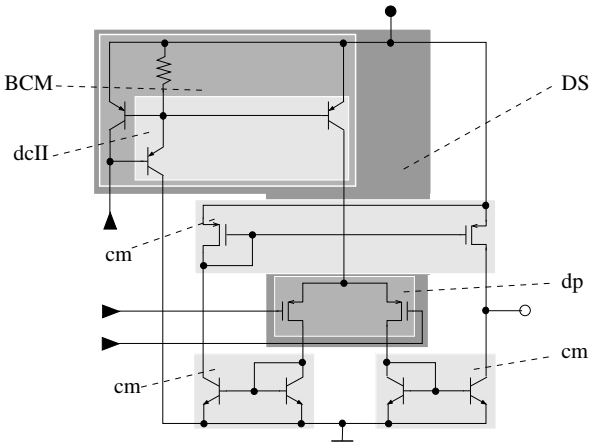

Figure 4. Detected building blocks in a BiCMOS OpAmp

Circuit	Number of transistors	Detected building blocks Level of hierarchy 0	1	2	3	Total
Fig. 4	11	11	5	1	1	18
BiCMOS BA.	16	14	7	2	1	24
OP-27	29	19	11	3	2	35
NE 5534	24	16	7	2	1	26

Table 1. Number of detected building blocks for several operational amplifiers

leads to a reduction of the complexity of the design process, since it reduces the number of free design parameters. Both together enable a reliable design process.

4.2 Circuit Sizing and Design Centering

Circuit sizing means that circuit parameters are tuned in order to achieve the performance specification. The task of design centering is to tune circuit parameters in order to maximize the parametric yield (i.e., percentage of circuits satisfying specified performance bounds) with respect to manufacturing tolerances. For circuit sizing and design centering, we used WiCkeD [13].

Incorporating the equality constraints and exploiting symmetries in the circuit in Fig. 4, the number of design parameters was reduced to eight. The chosen operating parameters were supply voltage and temperature.

Circuit sizing was performed twice from the same initial point, once with considering sizing rules, once without. Table 3 shows for six performances of the presented BiCMOS OpAmp, the corresponding specifications, the initial values, and the optimized values for both runs. The optimization algorithm stopped, as soon as all specifications were met, regardless of the circuit yield. At the initial point, the specifications were not met and two sizing rules were violated. After the automatic sizing process, all specifications were met in both runs. The simulation effort for the run with sizing rules was somewhat higher since this run also included 27 simulations that were performed to first find a point where all sizing rules were fulfilled. In the run without considering sizing rules, seven sizing rules were violated, which lead to essential differences in both efficiency and effectiveness.

Circuit	#Equalities	#Inequalities	Total
Fig. 4	6	61	67
BiCMOS BA.	9	69	78
OP-27	25	83	108
NE 5534	19	59	78

Table 2. Number of sizing rules for the given circuit examples

Performance	Specification	Initial Value	After Sizing with Sizing Rules	After Sizing without Sizing Rules
$DCGain$ [dB]	> 40	42.6	42.0	41.1
$CMRR$ [dB]	> 80	87.0	88.5	83.3
$PSRR$ [dB]	> 80	85.4	85.4	80.4
f_T [MHz]	> 45	10.2	45.1	49.8
PHM [^{o}]	> 70	94.3	85.6	92.2
SR_+ [V/μs]	> 6.0	7.74	6.87	7.40
#Violated Sizing Rules		2	0	7
Operating Range Violation		yes	no	yes
Number of simulations			172	154

Table 3. Comparison of automatic sizing results

After sizing, a parameter sweep over the operating parameters was performed. Exemplarily, the sweep result for the power supply rejection ratio (PSRR) over the supply voltage V_{dd} is shown in Fig. 5. Without sizing rules, the specification is met at the nominal supply voltage, but the design is very sensitive to variations of operating conditions. With smaller V_{dd}, the PSRR diminishes down to a value of less than 20dB at V_{min}. With sizing rules however, automatic sizing leads to a robust design with respect to operating tolerances. The PSRR stays above the specified lower bound of 80dB over the operating range of V_{dd}.

Starting from the results of automatic sizing, design centering was performed to maximize the circuit yield. Table 4 shows the design centering results for the BiCMOS OpAmp in Fig. 4. It shows all four cases from considering sizing rules throughout the whole optimization process to never considering sizing rules. For each case, Table 4 shows the overall yield, the number of simulations needed (unless the algorithm terminated prematurely) and the number of sizing

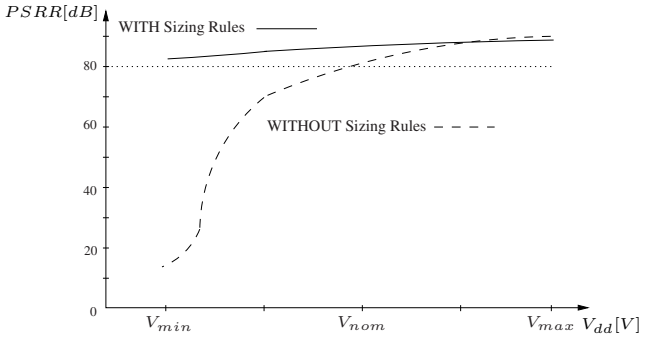

Figure 5. PSRR over supply voltage sweep

Design Centering	Automatic Sizing: with sizing rules	Automatic Sizing: without sizing rules	
with sizing rules	$> 99.99\%$	99.98%	yield
	1365	2475	#sims.
	0	0	#viol.
without sizing rules	78.9%	71.2%	yield
	no convergence	no convergence	#sims.
	1	7	#viol.

Table 4. Comparison of automatic design centering results

rules violated at the end. In the design centering run where sizing rules were considered, the yield was nearly 100%. In the run where sizing rules were not considered for automatic sizing, the simulation cost was about 80% higher. When no sizing rules were considered for design centering, the algorithm terminated prematurely. The reason for this can be explained as follows: The algorithm in WiCkeD that we used for design centering is based on piece-wise linear approximations. When sizing rules are fulfilled, the circuit's behavior is only weakly nonlinear. But as soon as sizing rules are violated, the circuit performance becomes strongly nonlinear and the linear models become too inaccurate to guarantee a proper result. Here, the algorithm terminated with a "linearization error". Thus, design centering could not be performed without the consideration of sizing rules. This clearly shows that sizing rules are essential for an efficient design centering.

5. Conclusion

In this paper, a generic hierarchical library and sizing rules for bipolar transistor building blocks have been introduced. The library is constructed hierarchically, so that an existing algorithm [5] for detection of transistor building blocks can be used. The large number of sizing rules of a circuit clearly shows that these cannot be established manually for each circuit.

The significance of the presented method follows from applications to circuit sizing and design centering. The results also show that sizing rules for CMOS and bipolar transistors fit well together to produce technically meaningful and robust results.

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