The ARTEMIS Cross-Domain Architecture for Embedded Systems

Hermann Kopetz
Technische Universität Wien, Austria
hk@vmars.tuwien.ac.at

Today the embedded system market is a highly fragmented market, where custom-designed solutions dominate, resulting in a significant duplication of development effort for hardware, software and services. The ever-increasing complexity level of embedded systems, the technology trends of the semiconductor industry to large production series of chips, and the increased competition in the world market entail the need for a European-wide coherent and integrated development strategy for embedded systems. The ARTEMIS technology platform has been created to fill this need by joining the forces of many of the European players in the embedded system market in order to create the critical mass that is necessary to tackle the formidable challenges of the field.

A first step of ARTEMIS was the setting up of an agreed strategic research agenda (SRA) in order to establish a common view of the issues that must be resolved in order that the world-wide leadership of the European embedded system industry can be maintained in the years to come. For this purpose, three expert groups, one on *Reference Designs and Architecture*, another one on *Seamless Connectivity and Middleware*, and a third one on *Design Methods and Tools* were formed. The mission of the *Expert Group for Reference Designs and Architectures* was to define the research priorities for future embedded systems that will lead to the *creation of a generic platform and a suite of abstract components with which new developments in different application domains can be engineered with minimal effort* [1]p.16. Generic platforms, or reference designs, will be based on a common architectural style that supports the composition of systems out of pre-validated independently developed subsystems that meet the requirements of the different application domains. Given a core *architectural style*, different *instantiations* of the generic platform (we call them also *artifacts*) can be created for different specific application domains, while retaining the capability of *component reuse* across these application domains.

The expert group on *Reference Designs and Architecture* developed the following strategy to meet its demanding mission. In a first phase the *constraints and requirements* that delimit the design space for the envisioned ARTEMIS cross-domain reference architecture have been established. Following the proverb *Good design comes from the proper constraints*, more than one-hundred fifty requirements and constraints have been collected from the different industries represented in the expert group. These requirements and constraints have been classified from the point of view of different application domains into five categories: *essential, very desirable, desirable, don't care, forbidden*. A detailed analysis of these classification led to the following seven high-level research topics: *Composability, Networking and Security, Robustness, Diagnosis and Maintenance, Integrated Resource Management, Evolvability, and Self Organization*. In the next phase the research and industrial community is asked to submit *conceptual architecture blueprints* for a European cross domain architecture for embedded system. These conceptual architecture blueprints will be evaluated with respect to satisfying the requirements and constraints that have been captured in the first phase. This second phase is expected to be financed by the European Commission in the form of FP 7 STREP projects. In a third phase one or two of the conceptual architecture blueprints will be selected for the implementation of *proof-of-concept architectural prototypes*. After a detailed test and evaluation of these *proof-of-concept prototypes* the industrialization of an ARTEMIS conformant architecture can start.

The *elevation of the level of design abstractions* was considered the most important issue that must be tackled by the envisioned Artemis Cross-Domain Architecture for Embedded Systems in order to manage the ever-increasing complexity of large embedded system. In order to manage the complexity of an evolving design at a higher level of abstraction, we must conceptualize subsystems that form *stable intermediate forms* and exhibit *aggregate properties*. If we can describe and specify these aggregate properties on their own by an appropriate interface model, then it is *not required to understand the structure and the interactions within the subsystems* in order to reason about the *interactions among subsystems* and the emerging system properties. It is then possible to change and enhance the implementation of the subsystems in response to technological developments (technology obsolescence management) without a redesign of the system at this

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higher level of abstraction. The architecture must provide the means to precisely specify the interfaces of a subsystem—we call it a component--in both dimensions, the value dimension and the temporal dimension. Additionally, the composition of systems out of independently developed and tested components must be supported by the architecture such that no unintended side effects of the integration will occur. Furthermore, the architecture must provide mechanisms for fault containment and the elimination of error propagation paths, such that faulty components can be localized and the consequences of component failures are mitigated.

The significant advances in communication technology, particularly in wireless transmission methods, make the vision of ambient intelligence, where ad hoc service networks are formed dynamically, come closer to reality. Whenever embedded systems are connected to open networks, such as the Internet, the issues of security, privacy, and confidentiality of information must be resolved. The research challenge in embedded systems is the development of resource-efficient security techniques, since the available resources (power, silicon real-estate) for security management are limited.

System robustness was also regarded to be in need of a primary research focus. System robustness is concerned with the provision of an acceptable level of service at the system level, even if transient or permanent failures occur within components, residual specification or design errors are present in the design (software or hardware), or the system is used outside its specification. In large system that must operate 24 per day for 365 days per year the occurrence of failures in the components and the operation must be considered the norm, not the exception. Architectural means that help to diagnose faulty components and to mitigate the consequences of hardware component failures might become a necessity when using the upcoming submicron devices, as stipulated in [2]p.6: *Relaxing the requirement of 100% correctness for devices and interconnects may dramatically reduce the costs of manufacturing, verification and test. Such a paradigm shift is likely forced in any case by technology scaling, which leads to more transient and permanent failures of signals, logic values, devices, and interconnects.* One technique to mask component failures and thus increase the system reliability is triple-modular redundancy (TMR). The envisioned ARTEMIS architecture must provide the framework - e.g. a deterministic communication infrastructure - such that TMR systems can be implemented without undue efforts.

The further shrinkage of the VLSI devices entails an increase in power densities across a silicon die that must be controlled at the system level. The integrated management of power, execution speed of the individual processors of a multi-core chip, and real-time deadlines is a new research topic that spans may level of system design, from the development of power-aware algorithms, to new scheduling techniques in the operating down to the proper architectural mechanism to control the selective power consumption of the upcoming billion transistor system-on-a-chip.

The evolvability of existing applications, up to the level where and assembly of nodes is capable to reflect on its situation and its environment and organize itself without any intervention from the outside, such that the optimal service will be provided, has been identified as an important long-range research topic.

References

[1] ARTEMIS Strategic Research Agenda 2005, <http://www.artemis-office.org/DotNetNuke/Portals/0/Documents/sra.pdf>

[2] International Technology Roadmap for Semiconductors 2005 Edition - Design, 2005 <http://www.itrs.net/Links/2005ITRS/Design2005.pdf>