Diagnosis, Modeling and Tolerance of Scan Chain Hold-Time Violations

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ABSTRACT

Errors in timing closure process during the physical design stage may result in systematic silicon failures, such as scan chain hold time violations, which prohibit the test of manufactured chips. In this paper, we propose a set of techniques that enable the accurate pinpointing of hold time violating scan cells, their modeling and tolerance, paving the way for the generation of valid test data that can be used to test chips with such systematic failures. The process yield is thus restored, as chips that are functional in mission mode can still be identified and shipped out, despite the existence of scan chain hold time failures. The techniques that we propose are non-intrusive, as they utilize only basic scan capabilities, and thus impose no design changes. Scan cells with hold time violations can be identified with maximal possible resolution, enabling the incorporation of the associated impact during the ATPG process and thus the generation of valid test data for the chips with such systematic failures.

1. INTRODUCTION

In very complex or custom macro designs, automation in the generation of timing models does not exist. Timing models are an abstraction of the design indicating timing dependencies for the PD (physical design) flow. Rather, generating timing models may be a manually intensive process that involves characterization across many corners (variables). Therefore, it is likely that a timing model may be invalid upon creation. Also, due to tool capacity limitations especially for very large designs, typically PD and timing analysis must be completed hierarchically with timing models of numerous cores. A timing model by itself has a slight inaccuracy and timing paths that intersect with multiple timing models will have a larger potential deviation. Consequently, in large hierarchical designs that consist of hard macros, the probability of invalid timing model usage increases. Thus, the risk of unknowingly closing chip timing in PD with invalid timing models does exist, potentially resulting in manufactured chips with hold time violations.

Furthermore, incorrect modeling of certain silicon characteristics, such as clock skew, or overlooking timing constraints in test mode may lead to hold time violations in this mode. These violations often times remain uncaught, as thorough verification processes, such as timing-annotated simulations, typically are too time consuming, and are thus dropped especially during the later stages of the tape-out process due to fast approaching time to market deadlines. As a result, hold time violations on scan path may show up in manufactured ICs.

Other reasons, such as true manufacturing defects, or process variations on a die, may also result in ICs exhibiting scan path hold-time violations. These type of failures, however, manifest sporadically in manufactured ICs, resulting in process yield degradations only. Other type of defects on scan chains, such as stuck-at defects on scan path, are also in a similar category as they too represent the manufacturing process imperfections, and thus manifest sporadically. The aforementioned physical design errors, on the other hand, result in systematic IC fails on the tester, and thus require special attention, as catastrophic process yield ensues otherwise.

An interesting observation about scan chain hold violations is that they do not interfere with the circuit‘s functional operation. The implication of these violations rather affects the test mode; the impact is the invalidation of the test procedure. Scan chain integrity tests, which consist of shifting a number of predetermined patterns through scan chains without effecting capture, are able to detect scan chain hold time violations. Structural ATPG patterns cannot be applied subsequently, if such violations are detected, as they too would fail on all the functional chips with scan chain hold time violations.

Although they may be perfectly functional, the manufactured chips with a hold time violation on their scan path cannot be shipped out to customers without the application of a proper manufacturing test via pre-computed ATPG patterns. In the case systematic failures due to design errors, the outcome is a **zero yield**. Expensive solutions to handle this type of a problem consist of fibbing or metal revision, which enable the manufacturing test, and thus recovering yield. The solution that we propose, on the other hand, is based on understanding and modeling the behavior of scan hold violations, and generating test data by accounting for the impact of these violations, so as to enable manufacturing test. Slight degradations occur in test quality, however, due to the controllability and observability loss induced by the scan hold violations. The original yield is perfectly restored at the expense of negligible coverage loss, a point that we revisit in the experimental results section, without resorting to expensive, alternative methods.

A hold time violation on a scan chain manifests on two fronts: the mismatch of the inserted scan stimulus and the intended one, and the mismatch of the scanned-out response and the expected

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one. The consequence is the inability to apply ATPG patterns through these chains, and hence, the failure to test and manufacture chips that has scan chain hold violations.

In this paper, we investigate the problem of scan chain hold time violations. Although the techniques that we propose can be used also on any chip that contains scan chain hold time violations induced by manufacturing defects, we specifically focus on the more critical problem of hold time violations induced by design errors instead. Our goal is to improve process yield in the case of such systematic chip failures without resorting to expensive techniques such as fibbing or metal revision. We provide solutions that enable the generation of valid test data for chips that has scan chain hold time violations, paving the way for being able to apply ATPG tests through these hold time violating chains and to screen out chips that truly fail in mission mode. The methodology we propose helps identify the chips that are functional in mission mode, which can still be shipped out despite the scan hold time violations in the scan chains, thus improving the yield cost-effectively.

We thus provide a suite of accompanying techniques; the proposed diagnosis technique is capable of identifying the hold time violating scan cells with maximal resolution, while the proposed modeling technique helps incorporate the appropriate changes in the netlist provided to the ATPG tool for generation of valid test data. Maximal possible resolution attained by the proposed diagnostic technique is crucial, since the overall goal is to accurately model the scan chain hold time violations and to tolerate them during the structural testing of the chips. In this suite of techniques, multiple intermittent/permanent scan hold time violations can be handled regardless of their distribution in the scan chains. In these techniques, the existing scan capabilities are utilized rather than any design changes or improvements, resulting in an elegant and practical solution that can be widely utilized.

2. PREVIOUS WORK

Significant amount of research work has been conducted in the area of scan chain diagnostics. Most of the work in the literature focused on sporadic defects rather than systematic failures however; defects that exhibit a stuck-at, transition, or hold-time violation behavior have constituted the underlying fault model in most of the papers that have been published in this area.

Various techniques [1, 2, 3, 4] have been based on improving the scan capabilities at the expense of increased area overhead so as to attain better scan chain test diagnostics. Improved scan capabilities consist of set/reset and toggle features added to scan cells by inserting multiplexers or XOR gates on the scan path. Area cost incurred by these approaches limit their practicality.

Kundu proposes the utilization of functional path so as to justify the scan cells to deterministic values [5], thus eliminating the ambiguity induced during scan-in operations in the defective scan chain. Sequential ATPG techniques are incorporated in this technique, rendering this methodology impractical especially for larger designs.

Simulation and scoring based approaches [6, 7, 8, 9, 10] have also been proposed for diagnosing scan chain failures. Based on a certain underlying fault model, individual faults are simulated and scored by comparing against expected responses. These techniques produce a range of scan cells as the suspect defective scan cells subsequent to extensive fault simulation, which limit their application on larger designs.

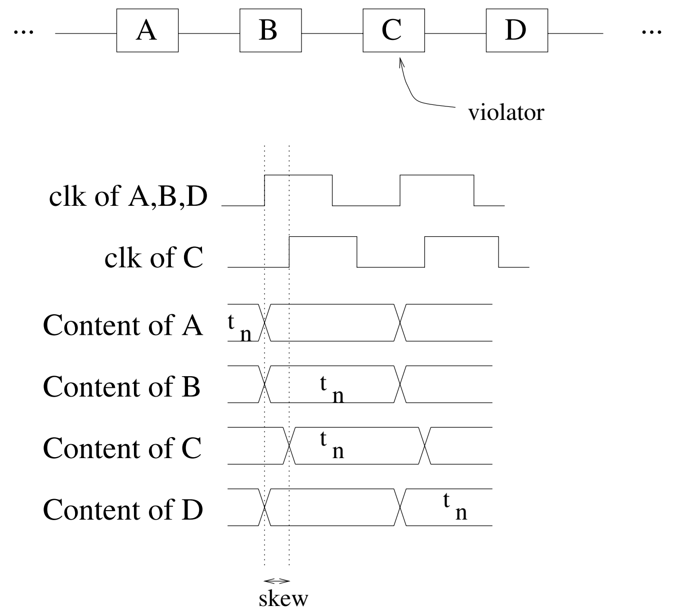

Figure 1: Scan chain hold time violation

Our approach to the scan chain problem is slightly different than these techniques. We aim at scan chain hold time violations that result in systematic failures, for which the previous techniques can also be applied as well; however, the proposed approach is based on diagnosing these failures with maximal resolution, rather suggesting a range of scan cells, so as to model them accurately and tolerate them in manufactures ICs.

3. CHALLENGES

In order to cope with scan chain hold-time violations, their impact needs to be modeled. In simple terms, a hold time violation occurs if the intended data input is changed before the active clock edge hits the flip flop; this typically happens due to clock skew. In the context of scan operations, a scan flop with a hold time violation results in the preceding scan flop on the chain acting like a buffer. During shift operations, the test data bit that is shifted into a scan cell also gets stored into the succeeding scan cell, if the latter cell is hold time violating. The resulting impact is thus a *bit skipping impact* in the context of scan chain hold time violations.

Due to the bit skipping impact of hold-time violations, the intended scan stimulus differs from the stimulus inserted into the scan chain with a hold time violating scan flop. Specifically, each of the scan cells between the hold-time violating flop and the scan-out pin, including the hold time violating flop itself, receives the scan bit that is intended for its preceding scan cell upon the completion of the scan shift operations prior to the capture operation. The stimulus delivered into the scan cells between the hold time violating flop and the scan-in pin remain unaffected. This impact is illustrated in the example in figure 1; a scan chain fragment of 4 scan cells, with a single hold time violating scan cell, namely, C, is shown. While the other three scan cells, namely, A, B, and D, latch their scan input on time, scan cell C latches its scan data late. As a result, the scan data that gets latched into B also gets latched into C erroneously. The scan cell that precedes the hold time violator scan cell, namely the scan cell B, acts just like

a buffer rather than a storage device, reducing the effective scan depth by one; the scan data in scan cell A reaches the scan cell D in two cycles due to the hold time violation, while this operation should take three cycles in a functional scan chain fragment of 4 cells.

Analogously, captured test responses get modified during scan-out due to hold time violations on the scan path. Specifically, the response bit captured in the scan flop that precedes the hold time violating flop is overwritten by the response bit captured in the preceding cell, and thus is lost. Furthermore, each response bit captured in a scan flop between the hold time violating flop and the scan-in pin is scanned out one cycle earlier than it is supposed to. The response bits captured in the scan flops between the hold time violating one and the scan-out pin, including the hold time violating scan cell, are scanned out intact.

While the diagnosis of the hold time violating scan cells can be driven by a comparison between the expected responses and the scanned-out responses, this process is complicated by the circular dependency induced by scanned-in test vectors differing from the intended ones. To break this circular dependency, test vectors that are *immune* to any scan path hold time violation should be used in this diagnosis process; a test vector that is immune to hold time violations is one that is scanned-in intact despite hold time violations. As the impact of a hold time violation on a scanned-in stimulus is simply the skipping of bits, a stimulus of all identical bits is immune to such an effect. Therefore, shifting of all 0s or all 1s as a scan stimulus will result in the delivery of known values into the scan cells that contain hold time violators. It should also be noted that, such stimuli is still immune to hold time violations even with inverters between scan cells on the scan path; the intended vector will be identical to the one scanned in no matter where and how many hold time violating scan cells and inverters exist on a scan chain. Scanning out the captured responses of the chip to the hold time violation immune test vectors will enable the location of these violators.

In any diagnostic process, the more the test vectors, the better the resolution. The number of hold time violation immune test vectors is determined by the number of chains with hold time violations and the number of scan cells in the scan chains with no hold time violations. A series of identical bit values need to be shifted in to the scan chains with violations, while the scan cells in the remaining chains can be freely filled in with arbitrary values. For F chains with hold time violations, and C scan cells on functional scan chains, 2^{F+C} hold time immune test vectors exist.

In this paper, we propose a methodology to identify hold time violating scan cells. The proposed methodology is based on the application of as many hold time violation immune test vectors as possible to the circuit under test and on analyzing the relationship between the expected and the scanned-out responses. The methodology we propose is capable of providing maximal possible diagnostic resolution.

We provide two algorithms for identifying the set of hold time violator scan cells. The first algorithm is a linear complexity algorithm that fails in certain corner cases, while the second algorithm is of quadratic complexity and can handle any corner case. The first algorithm may pinpoint a wrong set of scan cells as the violating cells in the case of consecutive hold time violating scan cells. It should be noted, however, that this is a highly unlikely case, as for two consecutive scan cells to be both hold time violating, the violation on the succeeding scan cell must be a gross violation. The clock arrival to the succeeding scan cell should occur later than the data arrival from scan out port of the second preceding scan cell; only a clock skew that is greater than the sum of two scan-out to scan-in path delays may result in such a scenario, which is quite unlikely.

As scan chain hold violations do not interfere with the functionality of the circuit in mission mode, ICs with these failures can still be manufactured, given that they can be screened through a proper high quality ATPG test. In this paper, we also propose a modeling technique to reflect the hold violation effects into the circuit netlist that is the input to the ATPG tool, providing a perfect match between the netlist and the manufactured silicon. The proposed modeling technique enables the generation of valid test data that can be applied with the existence of scan hold time violations, paving the way for applying manufacturing tests to screen out the chips that fail in mission mode. The only implication is a slight degradation in fault coverage in testing the chips with scan hold time violations, as controllability and observability is hampered. Functional chips with scan chain hold violations can still be shipped out, with no application of expensive FIB techniques. It is important to note that the diagnostic resolution in this process directly impacts the reduction in fault coverage, when chips with scan hold violations are structurally tested with the proposed modeling technique. The diagnosis methodology we propose nicely complements this modeling technique in that sense, as it is capable of providing maximal possible resolution.

4. PROPOSED DIAGNOSTIC PROCEDURE

In this section, we present the proposed scan chain hold time violation diagnosis procedure. This procedure is a four-stage process applied on the chips that have failed the chain integrity tests.

4.1 Stage 1: Identifying the number of hold time violations

The first stage of the proposed procedure aims at verifying that the chip failure is indeed due to scan hold time violation. A sequence of 0s is inserted to the failing scan chains for as many cycles as the number of scan cells (N) in the chain in order to fill in the entire scan chain with 0s. Subsequently, all 1s are inserted while the scan out pin is observed. In a chain with f hold time violating cells, the first 1-bit should be observed during the $(N - f)^{th}$ cycle; furthermore, a total of $N - f$ consecutive 1s should be observed. In order to rule out the possibility of stuck-at defects, the same procedure is applied by replacing 0s with 1s and vice versa. At the end of the first stage, not only is the scan hold time violation behavior of the chip verified, but furthermore, the number of such violations on every chain is identified.

4.2 Stage 2: Application of hold time violation immune test stimuli

Subsequently during the second stage, test vectors that are immune to any scan hold violation are applied to a chip that has failed the chain integrity tests. As many immune test vectors as possible are applied in a manner identical to the way static ATPG patterns are applied; the captured responses of the chip are subsequently scanned-out and collected for analysis.

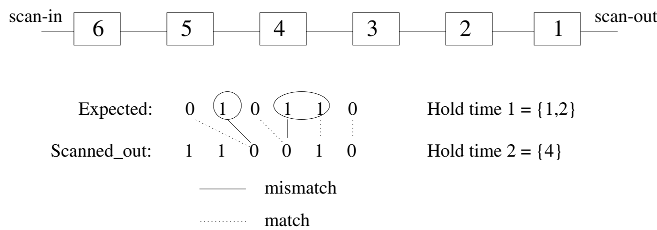

Figure 2: Bit by bit comparison to pinpoint hold time violating cells

4.3 Stage 3: Pinpointing hold time violating cells per test pattern

The third stage, wherein the scanned-out and the expected responses are analyzed to pinpoint the candidate scan hold violator cells, is the computationally dominating part of the diagnostic process. As the impact of a hold time violation is effectively bit skipping, the violator location problem is no different than the problem of comparing two bit strings and identifying the bit locations wherein one of the strings are missing bits. The deletion from the expected response bit string of the bits that correspond to the scan cells that precede the hold time violator cells should produce the scanned-out response string, except for as many leftmost bits as the number of hold time violations in the scanned-out response. For instance if the expected response is "011101100", and if the rightmost scan cell is hold time violating, the scanned-out response should be "x01110110", as the second rightmost bit, which is a 0, is skipped; the value of the leftmost scanned-out response bit depends on the next stimulus bit to be shifted in. It is interesting to note that an identical scanned-out response will be obtained if the second rightmost cell is hold time violating. Scanned-out responses may point to multiple scan cells as the responsible scan cell for a single hold time violation, consequently.

We propose two algorithms to solve the problem above; the first algorithm is a linear complexity algorithm but cannot handle certain corner cases, while the second algorithm that is of quadratic complexity is a complete one.

In the first algorithm, a bit by bit comparison is effected between the expected and the scanned-out responses starting from the first bit that is shifted out. The first bit location wherein there is a mismatch hints the location of the potentially hold time violating scan cell; the corresponding scan cell's successor is potentially hold time violating. It is important to note that there may be multiple scan cells that can account for the same hold time violation; this happens when consecutive bits of the expected response are identical. In this case, the skipping of any one of these consecutive identical bits results in an identical scanned-out response. All the associated cells are thus stored in the set of candidate hold time violating scan cells.

The comparison continues with a single bit offset; each expected response bit is compared against the response bit scanned-out one cycle earlier. Every time a mismatch occurs, a hold time violating scan cell is identified, and the offset is increased by one. The algorithm terminates when all the expected response bits are compared against the appropriate scanned-out response bits. The number of hold time violations identified by the algorithm should match the number identified in the first stage of the proposed diagnostic process. The execution of this algorithm is illustrated in figure 2; first, the rightmost bits of the expected and the scanned-out responses are compared, which is a match in this example. Similarly, the comparison of the second rightmost bits results in a match as well. A mismatch occurs, however, when the third response bits are compared; starting from that point on, expected response bits and scanned-out response bits are compared with a single bit offset. The fourth rightmost expected response bit matches the third rightmost bit of the scanned-out response bit, while there is a mismatch between the fifth rightmost bit of the expected response and the fourth rightmost scanned-out response bit. Since this is the second bit mismatch, the offset is incremented by one; thus, the leftmost bit of the expected response is compared against the third leftmost bit of the scanned-out response, which is a match. The algorithm terminates by reporting mismatches in the third and the fifth rightmost bits of the expected response. As the third and the second rightmost bits of the expected response are identical, the deletion of either bit accounts for the bit mismatch. Thus, either one of the second or the third rightmost cells must be the scan cell that precedes the first hold time violating scan cell; the first hold time violator should either be the first or the second scan cell from the right. As the fifth rightmost bit in the expected response is different than the fourth rightmost bit, the fifth scan cell is the only candidate preceding scan cell; the second hold time violator should be the fourth scan cell, consequently.

While the computational complexity of this algorithm is linear in the number of scan cells, the algorithm may fail to handle certain corner cases, wherein hold time violations occur in consecutive scan cells. In such a case, the algorithm, in all likelihood, will point to a number of hold time violations that is different than the one identified in the first stage, in which case the malfunctioning of the algorithm will be detected and the second algorithm should be utilized instead. For instance, if the expected response is "010101" and the scanned-out response of the chain that is known to have 2 hold time violations is "110101", the first algorithm will fail to pinpoint two hold time violating cells. Actually in this case, either the second and the third rightmost cells or the second and the third leftmost cells are hold time violating.

The second algorithm is based on a dynamic programming technique that is commonly known as the longest common subsequence problem [11]. The expected and the scanned-out responses are taken through this analysis so as to pinpoint the hold time violating scan cells. This algorithm is capable of handling any corner cases; however, its complexity is quadratic.

It should also be noted that both algorithms are capable of handling unknown bits in the expected responses. Bit comparisons are effected so as to report a bit match whenever an unknown bit in the expected response is compared against a bit in the scanned-out response.

4.4 Stage 4: Intersection of Candidate Scan Cell Sets

In the final stage, the candidate hold time violating cell sets, one identified for every hold time immune pattern application, are intersected; distinct intersection operations are effected for each hold time violation. Any inconsistencies among the candidate scan cell sets point to a possibly intermittent behavior of hold time violations. The intersection of the sets consists of all possible hold time violating scan cells that account for all the scanned-out responses collected, as illustrated in figure 3. In this example, as there are two patterns, and two hold time violators, two intersec-

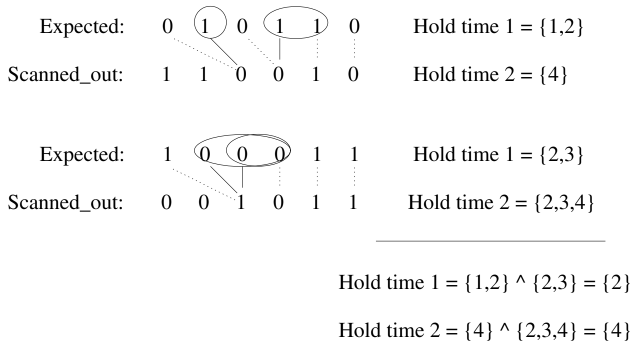

Figure 3: Identification of hold time violating cells via set intersection operations

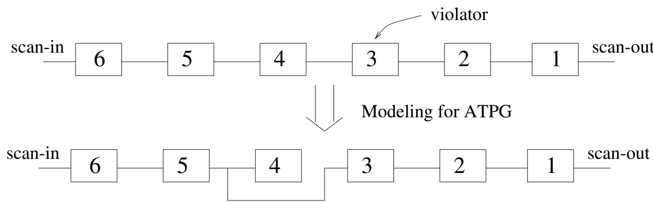

Figure 4: Modeling hold time violations for ATPG

tion operations are effected, one for each hold time violator. Both hold time violators are identified with perfect diagnostic resolution, as a single scan cell exists in the two final candidate hold time violator sets.

5. TOLERATING SCAN CHAIN HOLD TIME VIOLATIONS

For the ATPG tool to generate patterns that will pass on functional chips with scan chain hold violations, the impact of these violations should be accounted for in the netlist that is provided to the ATPG tool. Upon the execution of the proposed diagnostic procedure, the hold time violating scan cells can be identified. The bit skipping impact of the violations can then be reflected via modifying the circuit netlist that is provided to the ATPG tool, enabling the generation of valid ATPG patterns that will pass on functional chips with scan hold time violations.

In a scan chain with a hold time violating scan cell, the effective shift length is reduced by one bit. Also, the response bit captured in the scan cell preceding the violator scan cell is lost, rendering the preceding scan cell unobserved. Furthermore, the scan stimulus bit intended for the preceding scan cell overwrites the bit intended for the violator scan cell; the same bit is shifted into both cells, resulting in controllability loss as well. Consequently, the netlist modifications should be in the form of leaving the scan-out pin of the preceding scan cell unconnected, and of shorting the scan-in pins of the preceding and the violating scan cells together. The same set of modifications should be repeated for every identified hold time violation to perfectly match the netlist and the silicon. In the example illustrated in figure 4, a single hold time violator exists. As the third scan cell is the hold time violator, the preceding scan cell, namely the fourth one, acts like a buffer during shift operations; this impact is modeled as shorting the scan-in inputs of the third and the fourth scan cells together. Furthermore, as the response bit captured in the fourth scan cell will not be observed due to the hold time violation in the third scan cell, the scan out pin of the fourth scan cell is left unconnected. This way, the ATPG tool is forced not to give credit for the fault effects captured in the fourth scan cell, reporting an accurate fault coverage for the chips with scan chain hold time violations.

ATPG tool executed on a netlist that is modified in the aforementioned manner produces test vectors and expected responses that will be identical to the scanned-in stimulus and scanned-out responses in the presence of the associated scan chain hold time violations[1].

The aforementioned solution works perfectly well in the case of perfect diagnostic resolution, i.e., when the resulting candidate scan cell sets are singleton for each hold time violation. If multiple candidate scan cells exist for a hold time violation, then a conservative approach should be employed, enabling the generation of valid test data at the expense of slightly raised test quality degradation. As explained in the proposed diagnosis methodology section, there may be cases wherein any one of a set of multiple contiguous scan cells can perfectly account for the hold time violation. In such cases, the scan-in pins of these contiguous cells should be shorted together and their scan-out pins should be left unconnected. Furthermore, a number of dummy scan cells should be inserted at the beginning of these contiguous scan cells in order to adjust the effective shift length of the chain appropriately. The conservativeness serves the purpose generating valid test data; yet fault coverage degradation ensues.

The better the diagnostic resolution, the less the test quality degradation. A hold time violation immune stimulus that will be result in fewer contiguous identical bits in the captured response will provide better diagnostic resolution. An efficient and automated selection of scan hold time violation immune stimuli is an open research question that can be addressed subsequently.

6. EXPERIMENTAL RESULTS

We have implemented the proposed scan chain hold time violation diagnostic tool and the netlist modification tool, both in C programming language. We have executed these tools on ISCAS89 benchmark circuits [12]. In these experiments, we assume hold time violations in a number of randomly chosen scan cells. We have used the ATALANTA [13] as ATPG tool in our experiments.

We present the experimental results in table 1; in our experiments, all the benchmark circuits are configured to have 10 scan chains. The first column denotes the circuit name, while the number of hold time violations is provided in the second column. The number of hold time violation immune test vectors used to attain a perfect diagnostic resolution is given on the third column; in all cases, the actual scan cells with a hold time violation are exactly identified. The fourth and the fifth columns show the ATPG results for the original netlist, while the sixth and the seventh columns depict the ATPG results for the modified netlists that represent the impact of hold time violations.

The results in this table show that only a few hold time violation immune test vectors, which are randomly generated, suffice

[1]The presence of inverters between the scan cells will break this equivalence relationship; however, any commercial ATPG tool will account for these inverters, still producing valid test data, as the netlist modifications perfectly represent the scan chain hold time violations.

Circuit	Hold time violations	Immune vectors used	ATPG on original netlist		ATPG on modified netlist		
			Patterns	coverage (%)	Patterns	coverage (%)	coverage loss(%)
s13207	1	6	464	98.46	465	98.29	0.17
	2	4			461	98.00	0.46
	4	6			467	97.16	1.30
s15850	1	9	442	96.68	436	96.62	0.06
	2	11			434	96.55	0.13
	4	9			440	96.43	0.25
s35932	1	5	65	89.81	63	89.77	0.04
	2	5			66	89.72	0.09
	4	7			66	89.64	0.17
s38417	1	10	938	99.47	920	99.43	0.04
	2	10			915	99.39	0.08
	4	12			893	99.30	0.17
s38584	1	9	661	95.85	648	95.84	0.01
	2	11			655	95.79	0.06
	4	13			671	95.68	0.17

Table 1: Experimental results

to perfectly diagnose hold time violations in the scan chains. Perfect diagnostic resolution enables the accurate modeling of these hold time violations via netlist changes. While the fault coverage levels degrade slightly, the structural ATPG patterns generated on the modified netlist can be utilized in a production environment, enabling the manufacturing test of chips with scan hold time violations.

7. CONCLUSION

In this paper, we target the scan chain hold time violations that are induced due to physical design process errors, which lead to systematic chip failures on the tester, and to chips that are functional but cannot be tested. We propose a methodology wherein the hold time violating scan cells are accurately pinpointed. Furthermore, we propose another technique so as to model the impact of the hold time violating scan cells on scan shift operations, enabling a subsequent ATPG process to account for these violations, and thus generating structural ATPG patterns that will test chips with scan chain hold time violations.

The diagnostic technique that we propose is based on the application hold time violation immune stimuli to a chip that is known to have scan chain hold time violations. The captured responses of the chip are scanned out and collected for analysis. We also propose a pair of algorithms that compare the scanned-out responses with the expected ones, pinpointing any possible hold time violating scan cell that perfectly accounts for all the scanned-out responses.

The scan chain hold time violation diagnosis technique that we propose is based on the utilization of existing scan capabilities, imposing no design changes whatsoever. Single or multiple, intermittent or permanent scan hold time violations can all be handled.

The accurate and exact diagnosis of the hold time violating cells through the proposed diagnosis methodology enables the application of the modeling technique that we also propose. The modeled impact of the hold time violating scan cells can be reflected back into the netlist that the ATPG tool is executed on. The test patterns generated in this manner can be used for testing chips that has this systematic failure, restoring manufacturing process yield in a cost-effective manner.

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