Master Courses

M1 Constraint and Integer Programming Techniques and Tools for Digital System Design

Organiser: Michela Milano, DEIS, Bologna U, IT
Speakers: Michela Milano, DEIS, Bologna U, IT
Krzysztof Kuchkinski, Lund U, SE
Jean-Francois Puget, ILOG SA, FR

The purpose of this master class is to present to the Digital System Design community a set of effective techniques for solving large scale combinatorial optimisation problems related to hardware and software co-design.

In general, these problems are faced by modelling and solving them via Integer Programming (IP) techniques. Recently, Constraint Programming (CP) has emerged as a powerful programming paradigm that can be used in alternative or in conjunction with Integer Programming. Constraint Programming integrated concepts from different areas such as Artificial Intelligence, Mathematical Programming, Networks and Computational Logic. Its main strength concerns its efficiency, simplicity and flexibility. In particular flexibility is fundamental for changing the problem model adding or removing constraints without changing the solver.

In the master class we

1) focus on finite domain Constraint Programming and its integration with Integer Programming,
2) describe system level design applications modelled via Constraint Programming
3) present ILOG, a leading edge, commercial tool embedding both Linear and Constraint Programming solvers.

M2 RTL Power Optimisation: Concepts, Tools and Design Experiences

Organiser: Massimo Poncino, Verona U, IT
Speakers: Massimo Poncino, Verona U, IT
Prassanna Sithambaram, BullDAST, IN
Roberto Zafalon, STMicroelectronics, IT

The objective of this master class is that of describing how emerging design methodologies for RTL power optimisation have found their way into commercial EDA tools, and how such tools have been successfully exploited in industry-strength designs. The course is organised into three main sections. The first one provides a review of the most effective RTL power optimisation techniques currently available. The second part is dedicated to the presentation and demonstration of innovative commercial EDA tools that implement the surveyed estimation and optimisation techniques. The third part reports on industrial experience on the usage of the methodologies and tools introduced in the previous sections.

Intended audience for this class includes designers and design team managers from semiconductor companies and system houses, R&D engineers from EDA companies, and academic researchers and Ph.D. students in the field of IC/system design.

M3 Modern Design Techniques with SystemC

Organiser: Martin Speitel, Fraunhofer IIS, Erlangen, DE
Speakers: Bernhard Niemann, Frauhofer IIS, Erlangen, DE
Axel Braun, Tuebingen U, DE
Karsten Einwich, Fraunhofer IIS, EAS Dresden, DE
Martin Speitel, Fraunhofer IIS, Erlangen, DE
Christian Haubelt, Erlangen U, DE
Frank Mayer, Fraunhofer IIS, Erlangen, DE

Even with new design languages coming up, SystemC is widely accepted by EDA companies and used in many design teams. The tutorial gives an extensive overview of the application of SystemC for various aspects of system-on-chip design. It starts with an introduction to SystemC 2.0. Modelling at different levels of abstraction — from system development down to a synthesisable ASIC implementation — are covered. The tutorial is extended by HW/SW partitioning methodologies using SystemC, and includes analogue and mixed analogue/digital modelling with SystemC AMS. The verification of hardware dependent software and the novel SystemC verification library and its usage are also presented.

Intended audience: This master course is targeted to designers, who want to acquire basic knowledge of SystemC and its applications as well as design managers, searching for an inside view on the usage of SystemC in a C/C++ based design flow.