Net and Pin Distribution for 3D Package Global Routing

Jacob R. Minz, Mohit Pathak, and Sung Kyu Lim
School of Electrical and Computer Engineering
Georgia Institute of Technology, Atlanta, GA 30332-0250
{jrminz,mohitp,limsk}@ece.gatech.edu

Abstract

In this paper, we study the net and pin distribution problem for global routing targeting three dimensional packaging layout via System-on-Package (SOP). The routing environment for the new emerging mixed-signal SOP technology is more advanced than that of the conventional PCB or MCM technology – pins are located at all layers of SOP packaging substrate rather than the top-most layer only. This is the first work to formulate and solve the multi-layer net and pin distribution for layer, wirelength, and crosstalk minimization.

1. Introduction

The true potential of SOP (System-On-Package) technology lies in its capability to integrate both mixed-signal active components and passive components all into a single high speed/density three dimensional packaging substrate. Innovative ideas in the development of computer-aided design (CAD) tools for multi-layer SOP technology is crucial to fully exploit the potential of this new emerging technology. However, there has been very little development, if not none, of CAD tools that handle the complexity of automatic 3D SOP layout generation. The physical layout resource of SOP is multi-layer in nature: all layers are used for both placement and routing, and pins are now located at all layers. Therefore, the existing routing tools for PCB or MCM can not be used directly for SOP routing. In this paper, we study the net and pin distribution problem for global routing targeting three dimensional packaging layout. This is the first work to formulate and solve the net and pin distribution for layer, wirelength, and crosstalk minimization in three dimensional packaging layout. Our experimental results demonstrate the effectiveness of our algorithm.

2. Net and Pin Distribution Algorithm

2.1. SOP Global Routing

We define the SOP global routing problem formally as follows: Given a set of floorplans $F=\{f_1,f_2,\ldots,f_k\}$, netlist $N=\{n_1,n_2,\ldots,n_n\}$, and the routing resource graph, generate the routing topology $T(n)$ for each net n, assign n to a set of routing layers and assign all pins of n to legal locations. All conflicting nets are assigned to different routing layers while satisfying various capacity constraints. The objective is to minimize the total number of routing layers used, wirelength, and crosstalk. A detailed description of routing resource graph and layer structure in SOP is available in [2].

Our SOP router is multi-phased, where we divide the routing process into coarse pin distribution, net distribution, detailed pin distribution, topology generation, 2D layer assignment, channel assignment, and pin assignment step. The process of determining the location of entry/exit points for each routing interval is called pin distribution. The process of assigning nets to routing intervals (= routing layers between a pair of floorplan layers) is called net distribution step. In the coarse pin distribution step, which is done before net distribution, we find a coarse location for the pins and use this information for the net distribution. After the net distribution, detailed pin distribution step assigns finer location to all pins. A Steiner tree based routing topology for each net is constructed and a layer pair is assigned to it during topology generation step. In case we have many nets, the conflict among the nets for routing resources is resolved and layer pairs are assigned during 2D layer assignment step. The channel assignment problem is to assign each pin in the pin distribution layers to a channel in the floorplan layers. The purpose of pin assignment is to assign a location to the pin on the block boundary on the floorplan layer. We recently have implemented coarse pin distribution and 2-D layer assignment algorithms for SOP global routing [2].

2.2. Net Distribution Algorithm

A proper distribution of the nets is required to ensure end results are close to optimal. Net assignment for some nets is straight forward. When the floorplans are visited bottom to top, all nets having their pins in the lowest floorplan are assigned to the routing interval above it. The nets having pins the top-most floorplan are assigned the routing interval right below it. If the net is an x-net (= a net that spans multiple floorplan layers) it is propagated through every layer until its topmost floorplan is reached.

1530-1591/04 $20.00 (c) 2004 IEEE

The net distribution of the i-nets (= nets that are contained in a single floorplan layer) is flexible—we can assign them to either the above or below the floorplan layer. The objective of this step is to reduce crosstalk. We use the amount of overlap of bounding boxes of the nets as a measure of crosstalk. We also studied the case when no i-nets are propagated. We have developed a sophisticated heuristics wherein we partition the nets so that the crosstalk is minimized for each layer.

The net distribution problem is modeled as a graph with each i-net in the routing interval as node and the crosstalk interaction as edges. The weight of the edges denotes the amount of crosstalk between the nets. The crosstalk is calculated by the overlap of the bounding boxes of the net. The coarse pin distribution is used as the approximate location of the pins. It is assumed that nets in different interval are crosstalk shielded, which means no crosstalk exist between nets in different interval. The problem can then be seen as a restricted graph partitioning problem where some of the nodes can only go to one of two predetermined partitions. All nodes have two cost functions, *up_cost* and *down_cost* which are the costs of putting the net in either top or bottom routing interval. These costs are calculated based on the crosstalk induced by fixed nets and also the "movable" nets, which are nets assignable to the top or bottom routing interval. A probability of .5 is assigned to each movable nets. Once the nodes are moved to their routing intervals, the costs of all neighboring nodes are updated. In order to achieve better results iterative techniques similar to ones in [1] are used. The complexity of the algorithm is O(V+E) where V is number of nodes and E is the number of edges in the graph model.

2.3. Detailed Pin Distribution

The purpose of this step is to legalize the location of the pins while respecting the coarse pin assignment and optimizing wirelength. The results of the coarse pin assignment are used for force-directed placement of the pins in the pin distribution layers. Since we did not consider the layer in which the pin was located in the coarse pin redistribution, it may be possible that the pins exceed the capacity of the partitions local to the routing interval. However our algorithm handles this by moving the pins from such location to the closest available position. The pins are placed in locations near the centre of the net. The pins furthest from its center of the net in coarse assignment, gets placed in the best location (location nearest to the center) in the local partition.

The algorithm uses the "approximate" position of the nets as found by coarse pin distribution and the net distribution results to determine the initial location and routing interval of the pin. The position of the nets is stored as the grid location of the coarse pin distribution. The center of each net is calculated from this position of the nets. The displacement vector is calculated by taking the difference of the position of the center of net and the pin. A pair of numbers (a,b) such that $0<a<1$, $0<b<1$ is added to the position of the pins. The numbers reflect the scaled magnitude of the displacement vector. The variables a and b are less than 1 so that we can still keep track of the partitions of the pins. The pins in each routing interval are sorted according to their new positions. The pins are then sequentially assigned to grids previously determined.

Table 1. The impact of various detailed pin distribution.

	CPD		RAND		DPD	
ckt	*#lyr*	*wl*	*#lyr*	*wl*	*#lyr*	*wl*
n10	3	22	3	1111	3	1016
n30	6	1100	4	3889	4	3393
n50	4	807	5	5725	5	4553
n100	13	2999	6	8779	7	6893
n200	27	11424	12	18395	11	14020
n300	12	8627	13	20508	13	16169

3. Experimental Results

In Table 1 we report the number of layers required to complete routing (#lyr) and the total wirelengh (wl) for various pin distribution schemes. CPD is where no detailed pin distribution was carried out. The pins were assigned a location in the centre of their coarse partition without legalization. RAND randomizes pin locations while respecting the coarse partitions of the pins. DPD is our wirelength oriented pin distribution Algorithm. We include CPD since the wirelength can be seen as a tight lower bound for other schemes. We used our crosstalk driven net distribution algorithm for all schemes. The results show that DPD achieves the lowest wirelength for all circuits, while also decreasing the number of layers. Other related experiments show that our net distribution algorithm is effective in reducing crosstalk. More detailed results are available through our technical report [3]. Our future work includes channel assignment and pin assignment of the global routing and detailed routing.

References

[1] Jason Cong and Sung Kyu Lim, "Physical Planning with Retiming", IEEE International Conference on Computer Aided Design, p2-7, 2000.

[2] Jacob R. Minz and Sung Kyu Lim, "Layer Assignment for Reliable System-on-Package", Asia South Pacific Design Automation Conference, Jan 2004.

[3] Jacob Minz, Mohit Pathak, and Sung Kyu Lim, "Global Routing Paradigm for System-On-Package", GIT-CERCS-03-14, September 2003.