Power Supply Noise Monitor for Signal Integrity Faults

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Abstract *– We propose a monitor able to detect on-line excessive Power Supply Noise (PSN) at the power/ground lines. It has high resolution (100 ps), enough to collect the important features of PSN and its output is isolated from the local PSN. It is useful for any scheme that takes corrective actions to prevent signal integrity faults after detection of excessive PSN.*

1. Introduction

Power supply noise (PSN) is a major concern in the design of modern ICs. Current spikes produced during the switching activity are transformed in voltage bounces in the supply lines. This transient reduction in the supply voltage decreases the gate drive strength, thus increasing the gate delay and lowering the circuit performance, thus producing potential delay faults [2], [3].

On-line monitoring of PSN appears as an interesting possibility to obtain information about the presence of excessive PSN to warn that a delay fault is likely to occur. This allows to a system controller to take corrective actions. Desirable features of such monitors are: (a) They should be located anywhere in the circuit to check the PSN in the local power/ground lines. (b) They should be able to check PSN at a given time (high time resolution). (c) They must be sensitive to PSN on supply *and* ground lines.

In this paper we describe a novel proposal on a monitor for PSN that fulfils the requirements above mentioned.

2. PSN monitor circuit

The main idea consists of measuring the power supply noise through its effect on the propagation delay of an inverter chain. Figure 1(a) shows the schematic of the proposed PSN monitor. The three inverters block works as a delay line, whose delay depends on its effective supply voltage. In synchronous systems, the PSN is triggered by the clock signal. Accordingly, the input of the delay line is connected to a signal derived from the clock line of the circuit.

The NOR gate works as a control gate to disconnect or test the monitor when desired. When the monitor is working, signal CTRL must be at "0". Transistor MP1 works as a switch, which connects and disconnects capacitor C_Y from the local supply line. Capacitor C_Y must be large enough to keep the voltage V_Y practically constant during the sampling process, thus isolating the monitor's output from the influence of V_{DD} variations.

Transistors MP2 and MP3 work as switches connected in series between voltage V_Y and capacitor C_X. When signal CK is at "0", switch MP3 is open and MP2 is closed. Also, capacitor C_X is discharged through MN1 and voltage V_X is zero. The rising edge of the clock line closes switch MP3 and a current begins to flow to capacitor C_X increasing voltage V_X (Figure 1(b)). This current charges the capacitor C_X until the output signal of the inverter block changes, opening the switch MP2. Thus, the total charge supplied to C_X is proportional to the propagation delay of the inverter block. As the propagation delay depends on the effective supply voltage seen by this block, the V_X voltage at the end of the sampling period depends also on the supply voltage. As the power/ground bounce is produced just after the clock edge, the voltage V_X will be dependent on the power/ground bounce: the higher the bounce is, the longer the propagation delay and the higher the voltage V_X will be. Figure 1(b) shows the delays t_{d1} and t_{d2} due to two bounces in the supply voltage ($PSN_1 < PSN_2$). Voltage V_X increases accordingly, and in this way the V_X voltage is a sample of the effective supply voltage at the point where the monitor is connected.

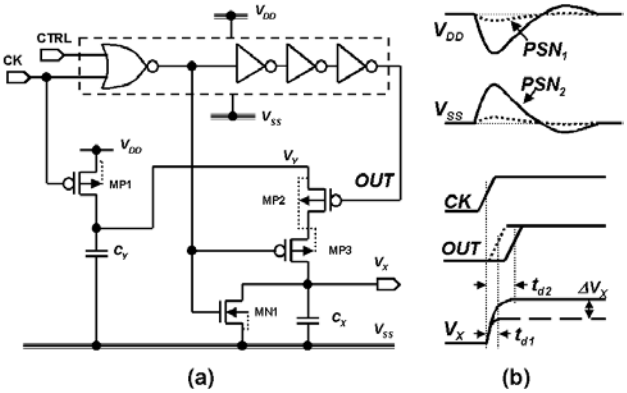

Figure 1. PSN monitor circuit.

The monitor samples the PSN during a time interval that is much smaller than the duration of the PSN [1]. The sensor sampling time corresponds to the moment when a rising edge is produced in the CK signal. By introducing a

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programmable delay line from the CK signal to the NOR input, we can change the sampling moment and obtain samples of the V_X voltage at different times to check the PSN in the whole clock cycle.

In addition, we have included a simple and fast comparator that uses the threshold voltage of one inverter as a reference to detect excessive PSN. It consists of a first inverter with adjustable threshold with its input connected to V_X, a second inverter, which provides feedback to the first one, and a last inverter that provides a clean digital output.

3. Simulations

This section presents simulation results of the PSN monitor built in a 100 nm CMOS technology. The results show that the monitor behaves in agreement with the previous analysis. The test bench consists of generating simple dips in the supply voltage synchronised with the rising edge of the clock signal. The waveforms of the dips are trapezoids put over the nominal V_{DD} and ground values. The delay between the dip and the clock edge, the dip width and the dip amplitude, are controlled to investigate the effect of these parameters on the monitor's behaviour. The dips are symmetrically applied to the power and the ground lines to check the correct behaviour of the monitor.

Figure 2 shows $\Delta V_X = V_X$(with dip) - V_X(without dip), that is to say, the increase in the V_X voltage due to PSN. Simulations with fast, nominal and slow corners have been performed to obtain the sensitivity of the monitor response to process variations. As can be seen, the variability of ΔV_X is small, which highlights the monitor robustness. In this figure *Vnoise* is the sum of V_{DD} and the GND dip/bump amplitudes.

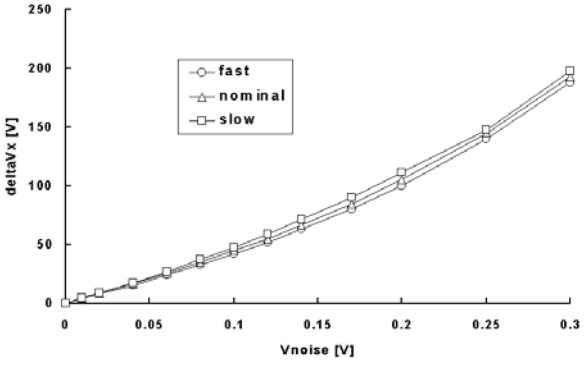

Figure 2. ΔVx versus Vnoise for fast, nominal and slow process corners

Finally, figure 3 shows the clock, V_{DD}, ground, V_X and VOUT waveforms. Clock frequency is 1 GHz, and a 100 mV PSN, 100 ps wide is introduced in alternate clock cycles. As can be seen, the comparator's output (signal VOUT) is activated (a zero pulse) only in the cycles where the noise is produced.

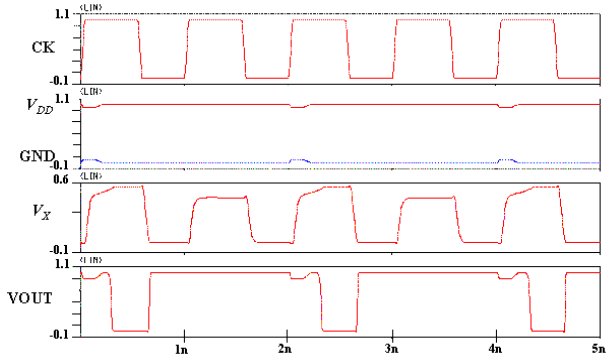

Figure 3. Monitor output for a clock frequency of 1 GHz and Vnoise=100mV

4. Conclusions

The PSN monitor described above is suitable for deep sub-micron technologies. It has the following features: (a) It can be located anywhere in the circuit and check the PSN in the local power/ground lines where the monitor is connected. (b) It has high resolution (100 ps), to collect the main features of the PSN in modern circuits. (c) It measures the PSN on supply *and* ground lines. (d) Its output is isolated from the PSN because it uses a locally generated "clean" power supply. (e) A high-level controller can easily change the sampling time, if required. (f) Control input allows selecting the desired clock cycle to measure PSN.

As the monitor is able to detect on-line the presence of excessive PSN, it can be used in any scheme that changes the operating circuit parameters to prevent signal integrity faults.

Acknowledgements: J. Rius acknowledges the support of the CICYT under projects TIC2001-2246, TIC2002-03127 and the Secretaría de Estado de Educación, Universidades, Investigación y Desarrollo in Spain.

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