Enhancing Testability of System on Chips Using Network Management Protocols

O. Laouamri & C. Aktouf
LCIS - INPG
50, rue Barthélémy de Laffémas –BP54-
26902 VALENCE cedex 9, France
Tel : (+33) 4 75 75 94 46, Fax : (+33) 4 75 75 94 50
{oussama.laouamri, chouki.aktouf}@esisar.inpg.fr

Abstract

This paper shows how to adapt the P1500 Design-For-Test standard through network management protocols to make the testing problem of System-On-Chips (SoCs) easier and cost-effective. For this purpose, a SoC is analyzed as a distributed system in which its own basic components or IP Cores (Intellectual Proprieties) are considered as network agents according to SNMP (Simple Network Management Protocol) protocol. An experimental study was carried out to show the effectiveness of such an approach.

1. Introduction

Today, The progress in *VLSI* technology allows the design of System-on-Chips (*SoC*). A *SoC* can embed hundreds of million of transistors. Such a huge amount of transistors within a single chip makes possible the implementation of complex functionalities for signal processing, calculation, memorizing, etc. The forecast of evolution made by the *SIA* (Semiconductor Industry Association) shows that the number of transistors per circuit will be multiplied by a factor fifty in the ten coming years [1]. Designing a *SoC* is mainly based on the use or the reuse of Intellectual Proprieties (*IP*) such as processor and memories (Fig 1) [2].

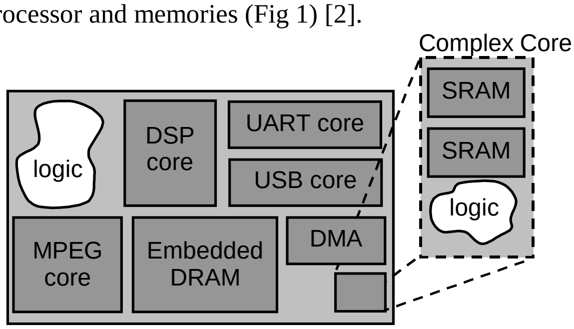

Fig. 1: Example of a *SoC* architecture.

The new design methodology of *SoCs* raises new testing problems [2,3]. Indeed, testing today integrated circuits involves the responsibility of not only the device manufacturer but also the designer and the *IP Core* provider.

An *IP Core* is tested by the core integrator as a part of a *SoC.* This is accomplished by using test vectors that are given by the *IP Core* provider. Indeed, the integrator of a *SoC* has few information on the used *IP Core. IP Cores are* considered as black boxes. Today, more than ever an *IP* has to be designed with testability issues in mind [2]: test point insertion, *Scan*, *BIST* insertion, etc.

Hence, the problem of *SoC* testing requires new challenges [3]:

- The transfer of an *IP Core* testing information from the designer to the user,
- The access to a testing *IP Core* infrastructure, so as to be able to reach the inputs/outputs and to connect them to an *ATE* (Automatic Test Equipment) or to a *SoC* logic *BIST*.
- The optimization of test integration to ensure a good trade-off *performance/cost.*

Beyond testing, another problem comes from the diversity of the origin and the technology of *IP Cores*. Indeed, the *IP Cores* are heterogeneous from several point of views: the used communication protocols, the used bus interface, frequency, etc. Such heterogeneous parameters imply connection and communication problems between the *IP Cores*. Thus, flexibility and compatibility are more than required by *IP Core* users.

Many test standards have been proposed to make *SoC* testing an easier and complex problem, in particular the *P1500 IEEE* standard [3,4]. Thus, the consortium Virtual Socket Interface Alliance [5] (*VSI Alliance*) insists on the intensive acceleration of the *SoC* development by specifying standards facilitating the mixture and the interconnection of *IP Core* coming from multiple sources. It also recommends the transfer of the test information between the provider and the integrator.

2. Test protocol approach

In this work, a novel design-for-test approach is proposed. The approach enhances the accessibility of *IP*

Cores, given a complex *SoC*. It takes advantage of the *SNMP* protocol which was originally proposed to enhance the management of *TCP/IP* local area networks, within a *SoC* for better testability of all *IP Cores* and consequently of all *SoCs* which constitute the electronics system. Indeed, *P1500* facilitates the access to the internal structure of an *IP Core* and the transfer of the information of test between the provider and the *IP Core* integrator. This new approach allows the mix of the *P1500* test architecture and the network management protocol *SNMP*. This also improves the maintainability of the *SoC* when used within a complex electronic system. *SNMP* was originally suggested by the Internet Engineering Task Force (*IETF*). Known as a simple and very efficient, *SNMP* embeds a set of functionalities that allow the management of the heterogeneous and complex networks. In this work, *SNMP* protocol is considered beyond the classical framework of the network management because it is implemented within a *SoCs*.

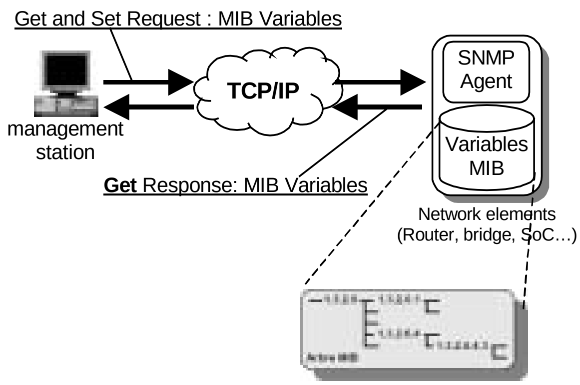

Fig. 2: SNMP environment

An *SNMP*-based network (fig. 2) consists of several components [6,7]: a Network Management Station (*NMS*), a Network Elements (*NE*), a database called *MIB* (Management Information Base) and a protocol. The *MIB* is a collection of objects stored into a virtual information base. An *SNMP* agent is a *NE*. It seeks network information such as the number of erroneous packets and sends them to the *NMS*.

Main motivations of using *SNMP* as a backbone of a testing strategy are summarized as follows:

- Management and monitoring of the activity of various electronic equipments that are widely used in local networks (computer, router, switch, etc.),
- Collecting of a deep state information on the state of each component,
- Detecting network failures,
- Elaboration of a standard management as regards to remote access to the information base (*MIB*),
- Take benefit from available network management software tools such as *HPOPENVIEW* of *Hewlett-Packard*.

More precisely, using the proposed approach, each *IP Core* with a *SoC* behaves as an *SNMP* agent. It is noteworthy that *P1500* has been considered for the following reasons: (1) it helps in the isolation of an *IP Core* among those that compose the *SoC*, (2) it provides a standard mechanism of access to internal logic, (3) it facilitates the mix and the interconnection of *IP Cores* which are provided form multiple vendors, (4) it is an *IEEE* standard widely spread and well documented.

3. Experimental results and conclusion

Several experimentations have been carried out using twenty-two benchmarks known as *ITC99* benchmarks. The area that is necessary at the level of an *IP Core* is low as shown in the following figure:

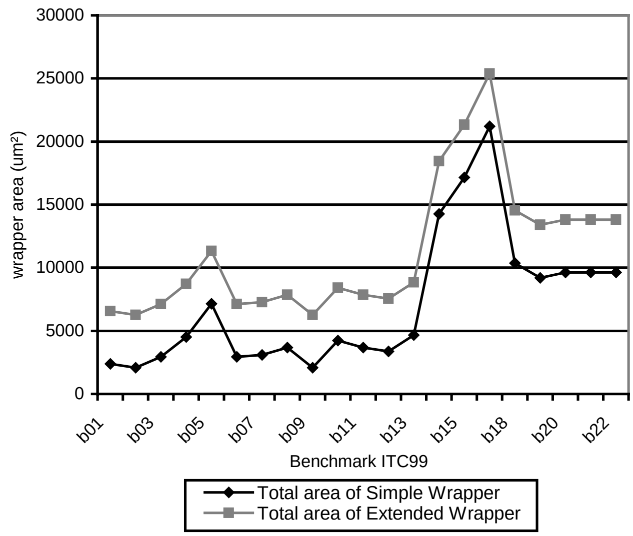

Fig. 3: Total area occupied by Wrapper adapted to benchmark ITC99.

For a complex *IP Core*, a *SNMP* interface necessitates a few added logic. Other experiments have been conducted which show the good trade-off *performance/cost* of the proposed testing approach. In future publication, the results and the research perspectives will be detailed.

4. References

[1] SIA Web site. http://www.semichips.org/

[2] Y. Zorian, "Embedded Tutorial: System-Chip Test Strategies". *Papers 35th Design Automation Conference ACM*, pp 752, Francisco, USA, June 1998.

[3] E. J. Marinissen, R. Kapur and Y. Zorian, "On Using IEEE P1500 SECT for Test Plug-n-Play". *IEEE International Test Conference (ITC)*, pp 770-777, Atlantic City, NJ, October 1-5, 2000.

[4] IEEE P1500 Web Site. http://grouper.ieee.org/groups/1500/

[5] VSI Alliance Web Site. http://www.vsi.org/.

[6] Douglas R. Mauro & Kevin J. Schmidt, "*Essentail SNMP* " O'Reilly, 2001.

[7] D. Perkins & E. McGinnis, "Understanding SNMP MIBs" Prentice Hall, Inc, 1997.