Accurate Estimation of Parasitic Capacitances in Analog Circuits*

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Abstract

This paper presents efficient and accurate techniques for modeling parasitic capacitances in analog CMOS circuits. A layout aware synthesis flow using these parasitic models has been proposed. The fast parasitic estimation process replaces the time consuming steps of layout generation and extraction during synthesis. Results indicate that these models are extremely fast and accurate.

1 Introduction

Although analog circuits occupy a small fraction of the total die area of a mixed signal IC, they are often the most difficult to design. One of the reasons for this being the extreme sensitivity of analog circuits to various layout-induced parasitics. Not accounting for layout parasitics during circuit synthesis often yields designs which do not meet performance constraints at the post-layout stage. Traditionally, circuit synthesis and layout synthesis steps are carried out independently, the latter following the former as presented in Figure 1A. This leads to multiple iterations of circuit synthesis and layout synthesis before a functional post-layout design is obtained.

In [1, 2], a layout aware synthesis methodology is proposed where layout synthesis and extraction is moved inside the circuit synthesis loop as shown in Figure 1B. This approach relies on Procedural Layout Generators (PLGs) for fast layout generation in the sizing loop.

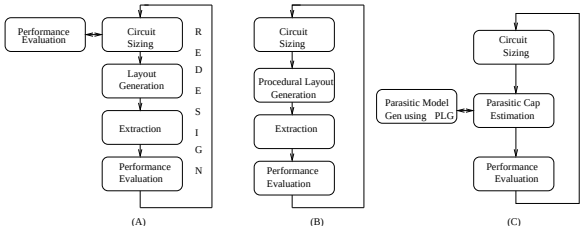

Fig. 1. (A) Traditional (B) Layout-in-the-loop (C) Proposed

This paper presents a technique for estimating parasitic capacitances. A layout-aware synthesis approach using these parasitic models has been proposed in Figure 1C. We build parasitic macro-models by analyzing several instances of layouts produced by PLGs. Since the parasitic models are fast and accurate, a circuit synthesis system using these models would be capable of accurately accounting for layout-induced effects during sizing. This would lead to designs of comparable quality as that obtained using a layout-in-loop approach. A large portion of the synthesis time is spent in layout generation and extraction in the layout-in-the-loop approach. Replacing the slow layout generation and extraction steps with an estimation step would help in reducing the overall synthesis time by a large margin. The proposed models thus would enable us to obtain designs which meet performance constraints at the post-layout stage in a shorter period of time.

In this paper, we focus exclusively on parasitic capacitances as in [1, 2] which dictate analog circuit performance in the sub GHz range. For RF circuits operating above 1GHz, inductive and resistive parasitics will also be needed.

2 Classification of Parasitic Capacitances

The various steps for layout synthesis of analog circuits are: circuit partitioning into modules, module generation, module placement and routing. A module is defined as a single device or a small group of devices which are laid out together. Examples of modules are transistors, differential pairs, current mirrors, etc. The module generation task is performed by PLGs using a predefined layout template. For the purpose of modeling, we have classified the parasitic capacitances into two categories:

- Intra-module parasitics, which are further sub-classified into (a) diffusion caps and (b) non-diffusion caps which include well, gate and interconnect caps (both area and coupling caps).
- Inter-module interconnect parasitics, which include the area and coupling caps of the inter-module interconnect fabric.

3 Intra-module Parasitics

All parasitics (device and interconnect) internal to a module belong to this category. The Module Specification Language (MSL)[3] system was used for the purpose of module generation. MSL provides a procedural layout generation environment for specifying parameterized layout generators. When the parameter values (typically device sizes) are supplied, a physical layout is generated. Off-the-shelf extractors can be used to extract a circuit including parasitic elements from this layout.

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3.1 Diffusion Parasitics

The parasitics associated with the diffusion (ndiff/pdiff) region of the active devices fall in this category. The diffusion parasitics are generally extracted in the form of area and perimeter of the drain and source of each transistor. These values (named AD, PD, AS, PS in spice transistor models) are used by numerical simulators to calculate the diffusion parasitics internally. For fingered devices, the diffusion area and perimeter of the entire structure are usually associated with the first finger and the remaining fingers have these values set to zero. Module Characterization Table (MCT) is obtained by gathering data from several instances of a module. It is a lookup table with one or more input variables (input columns) and one or more output variables (output columns). Input variables are usually the size parameters of the module and output variables are the various capacitances or the diffusion area/perimeter values observed from the extracted circuits. Table 1 shows the diffusion area and perimeter values for various instances of a fingered transistor module.

Tab. 1. Diffusion Caps for Fingered Transistor

Width (lambda)	AD	PD	AS	PS
50	6.5p	12.6u	6.5p	12.6u
150	13.5p	25.4u	13.5p	25.4u
300	21p	38.4u	27p	50.8u
450	34.5p	63.8u	34.5p	63.8u
600	42p	76.8u	48p	89.2u

In this paper, table lookup with linear interpolation was adopted for modeling the parasitics. Although simple, this method proved to be fast and accurate in practise, as evident from the experimental results. However, this method can be used only when the MCT size is not too large (within a few GB). Fortunately, for the type and size of circuits considered, MCTs are small enough to be used as lookup tables. Table 2 shows experimental results demonstrating the accuracy of MCT table lookup with linear interpolation. For each module, the variable was the transistor width, the MCT size was 500 and 200 validation points were considered. The MCT generation time reported in column 2 includes the time required for generating MCTs for diffusion and non-diffusion parasitics.

Tab. 2. Diff Cap Deviations for Modules

Circuit	MCT Gen Time(s)	Mean Dev(%)	Max Dev(%)	Std Dev(%)
Fingered Tran(n)	1150	0.05	1.4	0.19
Fingered Tran(p)	1150	0.09	1.33	0.24
Current Mirror	1250	0.09	1.33	0.24
Diff Pair	1250	0.21	2.45	0.38

3.2 Non-Diffusion Parasitics

Parasitics capacitances of the non-diffusion layers internal to a module belong to this category. These include parasitics associated with the well (nwell/pwell), gate (polysilicon) and interconnect (metal, polysilicon, etc). These parasitics are extracted as explicit capacitances between nodes in the circuit.

Tab. 3. Non-Diff Cap Deviations for Modules

Circuit	MCT Gen Time(s)	Mean Dev(%)	Max Dev(%)	Std Dev(%)
Fingered Tran(n)	1150	0.3	2.9	0.52
Fingered Tran(p)	1150	0.19	2.66	0.3
Current Mirror	1250	0.25	2.62	0.24
Diff Pair	1250	0.21	3.15	0.23

Both area and coupling capacitances have been considered. Several layout instances for the modules are generated and the values of these parasitics were accumulated into an MCT which could be used later for quick estimation during synthesis. The accuracy of the non-diffusion parasitic caps has been demonstrated for several modules in Table 3. The MCT size for each of the modules was 500 and 200 random validations were performed. The MCT generation time reported in column 2 includes the time required for generating MCTs for diffusion and non-diffusion parasitics.

4 Inter-module Interconnect Parasitics

The parasitic capacitances associated with the inter-module interconnect belong to this category. These parasitics are determined by the placement and routing of the modules in the circuit. In PLGs, the relative placement of the modules is fixed and the routing between modules is attained using routing boxes in MSL. Each net in the layout is defined using a routing box which comprises of a horizontal wire and several vertical wires. The MCT for these parasitics would necessarily have multiple input columns unlike the MCTs for the intra-module parasitics which generally have a single input column. A similar technique as that used for intra-module parasitics is used for MCT generation.

5 Conclusion

A look-up table and linear interpolation based technique was presented for modeling parasitic capacitances of analog circuits. The accuracy of these models have been demonstrated in the experimental results. The use of these models in a circuit sizing flow would help in achieving designs of quality comparable to layout-in-the-loop approach while reducing the overall synthesis time significantly. In this work only capacitive parasitics have been considered which is valid for circuits operating in the sub GHz frequency range. This work is a part of the SHARC (Synthesis of High Performance Analog and RF Circuits) tool-suite developed at University of Cincinnati under the DARPA NEOCAD program.

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