# A Macromodelling Methodology for Efficient High-Level Simulation of Substrate Noise Generation

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## Abstract

*Efficient prediction of the substrate noise generated by digital sections is currently a major challenge in System-on-a-Chip design. In this paper a macromodel to accurately and efficiently predict the substrate noise generated by digital standard cells is presented. The macromodel accuracy is demonstrated for some simple circuits.*

## 1. Introduction

Coupling through the silicon substrate in advanced integrated circuits (IC) is a severe source of problems and performance limitation. In this paper, we present a macromodeling methodology to predict substrate noise generated by large digital sections. The macromodel is generated element by element from identification of physical elements relevant to noise generation from the layout of the library cells.

## 2. Overview of substrate noise analysis and macromodelling proposals

A review of the most important existing methodologies for the substrate noise analysis and simulation is performed (SubWave methodology, from Berkelay [1], University of Hiroshima macromodelling approach [2] and SWAN methodology from IMEC [3]). The modelling of the substrate, that can be considered a resistive mesh between the substrate nodes of interest for frequencies up to a few GHz [4] is addressed using commercial CAD tools like SubstrateStorm from Cadence [5].

## 3. Gate Level Noise Macromodel

In this work, an improved noise macromodelling for the digital gates is presented. The macromodel is the basis of a noise evaluation methodology similar to [3] and [7]: individual gate macromodels are combined to form the complete circuit macromodel, and the event information of a logic simulator will be used for a SPICE simulation of this whole model.

The macromodel proposed is based on two main assumptions. First, the substrate noise introduced from the power-supply lines is considered dominant, as found in most typical situations [6,7]. Second, the high density of polarization contacts in the digital sections allows the substrate underneath the circuit, that is biased by the digital on-chip *gnd* line, to be considered a single node, independently of the substrate type, with a very low impedance connection to the local *gnd* node of each digital gate. As a consequence, the substrate noise is dominantly generated by the dI/dt noise present at the *gnd* line.

Figure 1(a) shows a basic digital gate (an inverter) loaded with another gate. Figure 1(b) shows the equivalent circuit for this gate and the reduced macromodel proposed in this work. The components of the equivalent circuit of Fig. 2(b) can be easily extracted from the transistor level description of the gates of a digital library. A simplified macromodel is obtained from the equivalent circuit obtaining the Norton equivalent, as shown in Fig. 1(c).

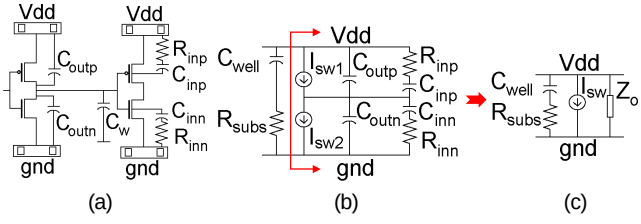


**Fig. 1: (a) Basic digital gate circuit, (b) equivalent circuit, and (c) macromodel.**

## 4. Macromodel parameters extraction

Compared to the existing methodologies presented in section 2, the proposed macromodelling approach provides a better understanding of the origin of the different elements that contribute to substrate noise in the macromodel, its relation with the real parasitics and active elements of the digital gate circuit, and a simplified and meaningful extraction process for the macromodel component values.

The well to substrate capacitance Cwell and Rsubs are obtained from the layout and a substrate model obtained with conventional substrate extraction tools [5]. The intrinsic

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capacitances shown in Fig. 1(b) between output and power supply ($C_{outp}$ and $C_{outn}$) are the drain diffusion capacitances to the well (*Vdd*) and substrate (*gnd*), respectively. They are calculated from the cell layout geometry and technology information. The extracted diffusion capacitances are averaged according to the possible gate states. The fanin capacitances and resistances of each gate input terminal ($C_{inp}$, $R_{inp}$, $C_{inn}$, $R_{inn}$) are also obtained during this phase and stored in the library database. The waveforms of the two current sources in the equivalent circuit ($I_{sw1}$ and $I_{sw2}$) are obtained by measuring the current at the local *Vdd* and *gnd* nodes, respectively, from a simulation of the gate netlist extracted from the layout including the substrate model. Different waveforms must be obtained for every input vector, therefore a database including all possible input transition combinations must be created for every gate. Fanout and input rise/fall time dependence is also accounted for in the current waveforms.

In the case of gates with complex NMOS and PMOS trees but with a single stage (NAND, NOR, etc.), the capacitance between the output and the local power supplies are calculated by averaging the capacitances of all the possible states of the gate, assuming that all states have the same probability. For multistage gates (OR, AND or flip-flops) an efficient extraction procedure has also been developed.

## 5. Validation of the macromodel

Figures 2, 3 and 4 show simulation results where the substrate noise waveforms obtained with the proposed macromodel are compared with full transistor SPICE simulations for different circuits.

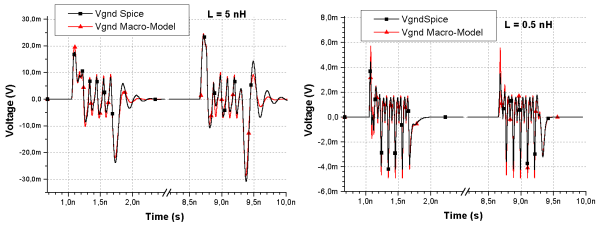


**Fig. 2: Substrate noise for an 11 inverters chain.**

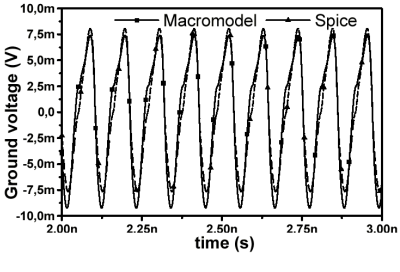


**Fig. 3: Substrate noise for a ring oscillator.**

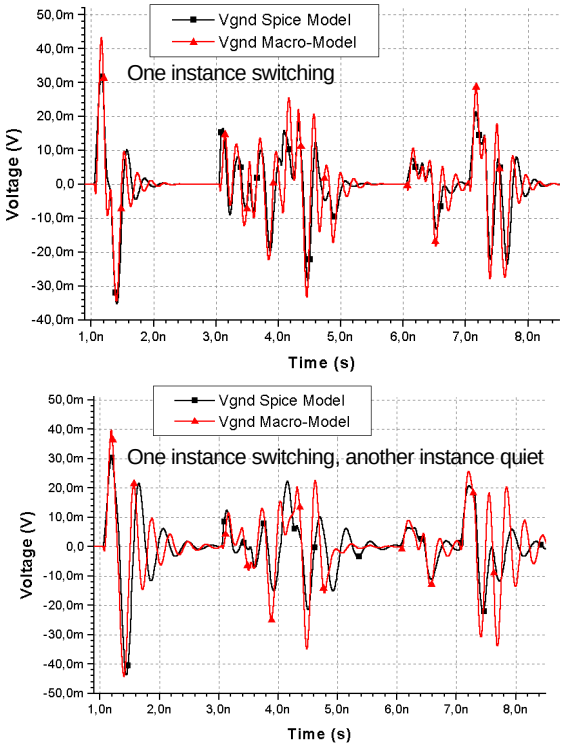


**Fig. 4: Substrate noise waveforms for ISCAS27.**

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