Hierarchical Modeling and Simulation of Large Analog Circuits

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Abstract

This paper proposes a new hierarchical circuit modeling and simulation technique in s-domain for linear analog circuits. The new algorithm can perform circuit complexity reduction by deriving the exact or approximate admittances in rational form in the reduced circuit matrix and deriving the circuit characteristics for very large linear analog and interconnect circuits. We characterize some theoretical results regarding the conditions on the generations of canceling terms during the general hierarchical circuit analysis and propose an explicit de-cancellation scheme to remove canceling terms based on a new hierarchical symbolic analysis framework. The resulting algorithm can be used for modeling and simulation of linear analog and interconnect circuits in both frequency and time domain.

1 Introduction

In this paper, we propose a new modeling and simulation technique via a hierarchical symbolic analysis technique. The new algorithm can reduce the circuit complexities by subcircuit reduction and keep the generated admittances in the reduced circuit matrices in the exact or approximate rational forms. Our work is inspired by the recent work of Qin and Cheng [1], where node reduction (called $Y-\Delta$ transformation, which is essentially the symbolic Gaussian elimination) is performed to reduce the circuit complexities and the resulting circuit admittance are kept as rational functions of s in reduced order. But this method only works for linear circuits with limited element types (RCLK-VJ) and cannot be applied to analyze general linear analog circuits. A more general circuit complexity reduction method based on the general subcircuit elimination has been proposed recently [3], which can be applied to any linear circuits. In this paper, we follow the same subcircuit-based reduction strategy. Our new contributions are follows: (1) we propose a new graph-based hierarchical decomposition scheme, which is more de-cancellation friendly and more compact than existing approaches; (2) we further characterize the conditions on the generations of canceling terms during the subcircuit elimination process; (3) we propose an explicit de-cancellation scheme to remove the canceling terms. The resulting algorithm can be used for modeling and simulation of linear analog circuits in both frequency and time domain.

2 New Hierarchical Decomposition

Consider a subcircuit with some internal structures and terminals. The circuit unknowns—the node-voltage variables and branch-current variables—can be partitioned into three disjoint groups $\mathbf{x}^I$, $\mathbf{x}^B$, and $\mathbf{x}^R$, where the superscripts *I, B, R* stand for, respectively, *internal* variables, *boundary* variables and the *rest* of variables. With this, the system-equation set $\mathbf{Ax}=\mathbf{b}$, can be rewritten in the following form:

$$\begin{bmatrix} \mathbf{A}^{II} & \mathbf{A}^{IB} & 0 \\ \mathbf{A}^{BI} & \mathbf{A}^{BB} & \mathbf{A}^{BR} \\ 0 & \mathbf{A}^{RB} & \mathbf{A}^{RR} \end{bmatrix} \begin{bmatrix} \mathbf{x}^I \\ \mathbf{x}^B \\ \mathbf{x}^R \end{bmatrix} = \begin{bmatrix} \mathbf{b}^I \\ \mathbf{b}^B \\ \mathbf{b}^R \end{bmatrix}. \quad (1)$$

The matrix, $\mathbf{A}^{II}$, is the *internal* matrix associated with internal variable vector $\mathbf{x}^I$.

Subcircuit suppression (Schur Decomposition) is to eliminate all the variables in $\mathbf{x}^I$, and to transform (1) into the following reduced set of equations :

$$\begin{bmatrix} \mathbf{A}^{BB}-\mathbf{A}^{BI}(\mathbf{A}^{II})^{-1}\mathbf{A}^{IB} & \mathbf{A}^{BR} \\ \mathbf{A}^{RB} & \mathbf{A}^{RR} \end{bmatrix} \begin{bmatrix} \mathbf{x}^B \\ \mathbf{x}^R \end{bmatrix} = \begin{bmatrix} \mathbf{b}^B-\mathbf{A}^{BI}(\mathbf{A}^{II})^{-1}\mathbf{b}^I \\ \mathbf{b}^R \end{bmatrix}, \quad (2)$$

Suppose that the number of internal variables is *m*, and the number of boundary variables is *l*. Then we have the following theorem without proof.

Theorem 1 *Each element in the modified* $\mathbf{A}^{BB}$ *submatrix can be written in the following form:*

$$a^{BB*}_{u,v} = \frac{det(\mathbf{A}^{II}_{(u,v)})}{det(\mathbf{A}^{II})} \quad (3)$$

where $u,v = 1,...,l$ *and Each element in the modified* $\mathbf{b}^B$ *vector can be written in the following form:*

$$b^{B*}_{u} = \frac{det(\mathbf{B}^{II}_{(u)})}{det(\mathbf{A}^{II})} \quad (4)$$

where, where $u = 1,...,l$ *and* $\Delta_{u,v}$ *is the first-order* cofactor *of* $det(\mathbf{A})$ *with respect to* $a_{u,v}$, $det(\mathbf{A}^{II}_{(u,v)})$ *is the determinant that consists of* A^{II} *plus row u and column v of the flatten matrix of the whole circuit;* $det(\mathbf{B}^{II}_{(u)})$ *is the determinant that consists of the* A^{II} *plus row u of the flatten matrix and the right hand side column* $\mathbf{b}^I$. *The* $det(\mathbf{A}^{II}_{(u,v)})$ *and* $det(\mathbf{B}^{II}_{(u)})$ *are illustrated in Fig.1.*

With Theorem 1, we only need to one DDD (as $det(A^{II})$ is shared by all the involved matrix elements for each subcircuit) for each boundary-variable related element in the reduced circuit matrix instead of representing each individual first-order cofactors of $det(A^{II})$ explicitly. An important feature of such DDD-only representation is that it is more amenable for removing cancellations during subcircuit reduction process as shown in the next section.

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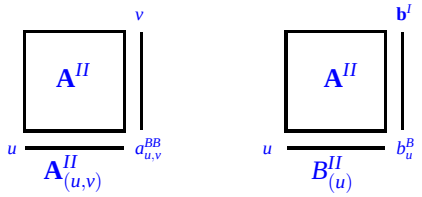

Figure 1. Illustration of Theorem 1

3 Term and Common-Factor Cancellations in Subcircuit Reductions

Term cancellation (involved terms become zero when added together) will happen when MNA formulation is used where each device admittance may appear more than once [3]. It turns out that common-factor cancellation, which happens when a common factor appear in both the numerator and the denominator of the resulting rational functions, will also be introduced. The common factors, which are rational functions or polynomial of s themselves may increase the orders of the resulting rational admittances. This can lead to large errors when only limited order of s are kept for those admittance as the required coefficients of specific order of s^i in a polynomial may be truncated due to shifting of their orders. It was shown in [3] that in general $det(A^{II})^m$, $m \geq 1$ may becomes a common factor due to multiplication of composite admittance terms. In general, we have the following results regarding the term cancellation during the subcircuit reduction process.

Theorem 2 *For a given product term from a determinant, which consists k first-order cofactor* $\Delta_{i_1,j_1}...\Delta_{i_k,j_k} k \geq 2$*, if there are two first-order cofactors that share the same row index or column index, then there exists another product term which will cancel with this product term.*

Note that since we only need to compute the rational functions for determinants during the reduction process in the new hierarchical decomposition framework, it is sufficient to consider cancellation conditions in a determinant. This is in contrast with the method in [3], where cancellations during the merging of composite admittances from different subcircuit levels have to be considered and treated explicitly.

4 New Hierarchical Circuit Modeling and Simulation Algorithm

4.1. Overview of the New Modeling And Simulation Framework

Our new circuit modeling and simulation algorithm is based on a new hierarchical decomposition framework and cancellation rules given in early sections. The basic idea is to reduce subcircuits and the right-hand side vector in a hierarchical and cancellation-free way. The new admittances coming from subcircuit suppressions shown in Eq.(3) and Eq.(4) are kept as rational functions of s in the exact or order-reduced form (with fixed order of s). Such reduction can be repeated until we reach the top level circuit, which is typically small enough to be solved exactly symbolically (s is still the only symbol). From a simulation perspective, once parent circuit variables $\mathbf{x}^B$ and $\mathbf{x}^R$ are obtained, we can obtain the internal variables of subcircuit A^{II} by solving

$$A^{II}\mathbf{x}^I = \mathbf{b}^I - \mathbf{A}^{IB}\mathbf{x}^I. \quad (5)$$

In this way, we can obtain all the unknown variables in the rational form. From a modeling perspective, we can easily obtain the network functions of the given circuits to compute other small-signal characteristics of analog circuits and second or higher order effects as distortion and nonlinearity can be estimated based on network functions of linearized circuits.

4.2. De-cancellation Schemes

The de-cancellation process needs to remove two types of cancellations, the common-factor cancellation and term cancellation. It was shown in [3] that common factors can be removed during the rational function computation using so-called *constant-admittance* strategy. Although this method also takes care of the term cancellation as those terms will eventually cancel out numerically. But it will cause more unnecessary polynomial divisions. In this paper, we explicitly remove the term-cancellation terms by constructing term-cancellation-free YDDD graphs. The idea is to remove all the term-cancellations during the YDDD graph construction. Theorem 2 clearly predicts which product term in a determinant is a canceling term or not. This strategy used here is similar to device level term cancellation [2], where canceling list is built for each YDDD index and YDDD can be built cancellation-free.

As an example, we drive the transfer function of a simple RC circuit shown in Fig. 2 that has a circuit hierarchy definition. There are four subcircuits. Subcircuit 1 is composed of node 1, subcircuit 2 is composed of subcircuit 1 and node 2 and so on. The transfer function computed from the hierarchical circuit is

$$\frac{V_8(s)}{V_5(s)} = \frac{\frac{15+98s+174s^2+76s^3}{5+18s+11s^2}}{\frac{56+412s+914s^2+648s^3+128s^4}{5+18s+11s^2}}$$

which agrees with the exact transfer function obtained from flatten circuit. The new method can solve much larger circuits than before due to its hierarchical nature [3].

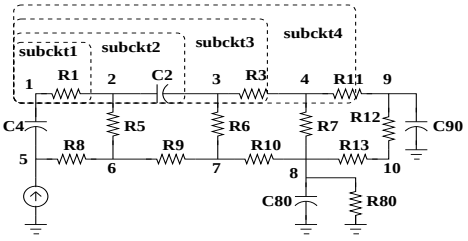

Figure 2. A RC network with hierarchical definition

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