Design and behavioral modeling tools for optical network-on-chip

M. Brière, L. Carrel, T. Michalke, F. Mieyeville, I. O'Connor and F. Gaffiot
Ecole Centrale de Lyon
Laboratory of Electronics, Optoelectronics and Microsystems
36 avenue Guy de Collongue, 69134 ECULLY, FRANCE
matthieu.briere@ec-lyon.fr

Abstract

In this paper, we present a tool to analyse photonic devices that can be used to realize basic building blocks of an optical network-on-chip (ONoC). Co-design between electrical tools and optical tools is possible. The VHDL-AMS language has been used to implement behavioral models of photonic devices. For low-level simulation, a gateway between an optical simulator, based on the finite elements method, and a typical EDA layout editor has been realized.

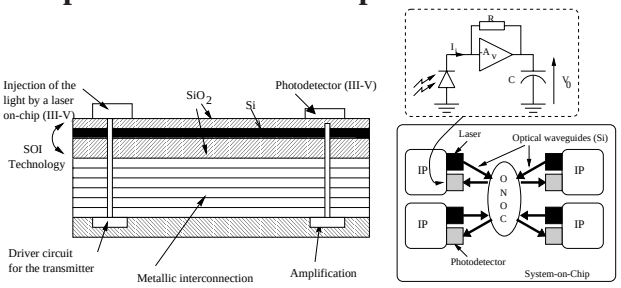
1 Introduction

Optics is in widespread use in long-distance communications, but this solution has not yet been widely used in chip-to-chip or on-chip interconnections. Some benefits of optics in data transport and clock distribution can be pointed out. However, optical interconnect in the centimeter or micrometer range, as well as optical integrated devices are not yet industry-manufacturable owing to the lack of (and need for) fully mature technologies.

To evaluate the benefits of optical interconnect with respect to metallic interconnect limits, the development of multi-domain tools (electrical and optical) are necessary for optimization and analysis.

In this paper we present an optical simulator and simulation results obtained by behavioral modeling of an ONoC.

2 Optical Network on-chip CAD tools



(a) Optical interconnect technology (b) ONoC system

Figure 1. ONoC description

Figure 1 shows an ONoC with all electronic interfaces: photodetector and laser in III-V technology and optical network in SOI technology (Silicon On Insulator). Intellectual property (IP) blocks shown can be processors, memories, etc. This is is a multi-domain device with high speed optoelectronic circuits (modulation of the laser current and photodetectors) and passive optics (waveguides and passive filters).

2.1 Specific optical tools

The main family of methods used to analyse the behavior of optical devices are the Finite Element type Methods (FEMs). FEMs is a numerical computer-based technique for calculating the behavior of engineering structures. We have developed an in-house program implementing the Finite-Difference Time-Domain algorithm [1]. This algorithm calculates the electric and magnetic fields (i.e. the "value" of the light wave) in the structure. These electromagnetic fields give informations about the propagation of the wave in a structure. With these field values, the power (with the Poynting vector) can be calculated over some surfaces of the structure (at the outputs of a waveguide for example).

2.2 Specific electrical tools

To analyze the receiver IC (top of figure 1(b)) a behavioral description is necessary. Behavioral description with a standard language such as VHDL is an essential stage in IC system design. It is used in all design steps from specification to the realization of systems.

VHDL-AMS [2](IEEE standard 1076.1) allows the extension of the VHDL concept to analog and mixed domains, as well as non-electric physical phenomena descriptions such as optical, thermical, mechanical, ...

3. Design solution

For ONoC design and simulation, there is a multi-domain need: a possible solution is to use an unified description language. There are several advantages: i) local and global optimization becomes possible and ii) exploration of the design space is easier. However, the communications and the interfaces between the subsystems are described in a more abstract way. The VHDL-AMS language is a suitable behavioral description language. With this lan-

1530-1591/04 $20.00 (c) 2004 IEEE

guage, it is possible to formalize the behavior of complex ONoCs.

Design and behavioral modeling tools based on previously described concepts have been developed. These tools use a hierarchical design with physical representation for low-level simulation. The top-down simulation concept is adopted. An optimization of optical devices is possible with a return of data from simulations of the optical filter and from physical measurements on the chip.

3.1 Hierarchical design

The left of figure 2 shows the typical design flow for electronic system simulation. A similar design flow can be used for ONoC simulation (shown on the right of figure 2). In the middle of figure 2 specific simulation tools are displayed. The designer can note that for the low level step, the same tool is used; thus, concurrent electronic and photonic simulation is possible.

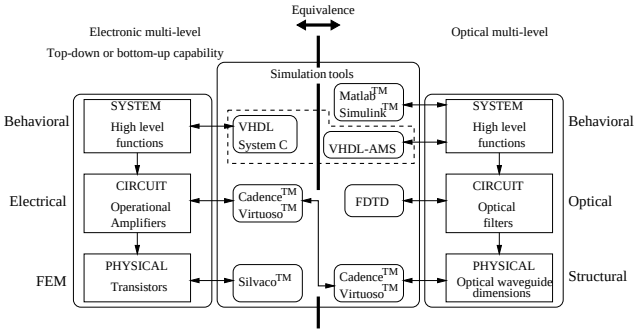


Figure 2. Electronic and optical design flows

A library of models has been created with several "black boxes" which describe the behavior of a photonic component with its spectral response *R*. A photonic device can be considered as a filter with several inputs and outputs.

A simple example of an optical network, created with the VHDL-AMS language, is shown in table 1.

```
Ka: entity work.ring_milieu(x_deuxdisque) generic map(L1,L2,c,nom,long1,t0)
port map(eone,etwo,etree,efour);
KK: entity work.ring_milieu(x_deuxdisque) generic map(L1,L2,c,nom,long2,t0)
port map(etree2,efour2,efive,esix);
KKK: entity work.ring_milieu(x_deuxdisque) generic map(L1,L2,c,nom,long3,t0)
port map(efive2,esix2,eseven,eeight);
```

Table 1. Example of network code

3.2 Physical design

To optimize the photonic devices it is necessary to go down to a low level of simulation; this corresponds to the FDTD method (shown in figure 2). With this method an optimization of the device is possible (dimension, injection value, ...). Virtuoso^{TM} is the layout editor of the Cadence^{TM} suite. We have coupled Virtuoso^{TM} with the FDTD algorithm (with the SKILL^{TM} language developed by Cadence^{TM}). The designer can draw the device to simulate it in the layout editor and then directly perform FDTD simulations.

The parameters which communicate between the FDTD algorithm and layout editor are the waveguide and substrate indices, spatial discretization step (for the dimension of the mesh) and the cartesian position of photon injection.

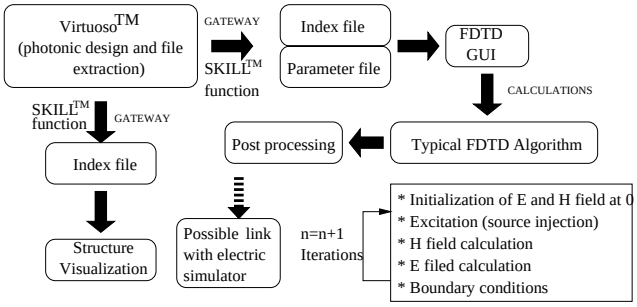


Figure 3. Design flow for low level simulation

4 Optical Network on-chip applications

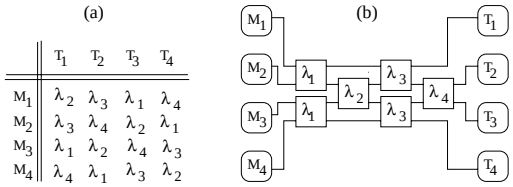
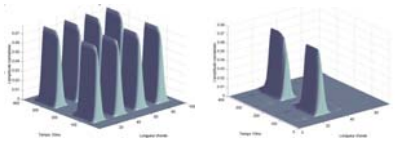


Figure 4. Optical network 4 X 4

Figure 4(b) illustrates a possible 4 X 4 ONoC. M_i are the masters (processor, IP, ...) which can communicate with targets T_i (memory, ...). The network is comprised of 4 stages, each associated with a single resonant wavelength. The operation of the 4 X 4 network is summarized in the table of figure 4(a). The basic element (box λ_i) is an optical filter

With behavioral modeling (high level simulation), this working can be verified. An injection of 4 wavelengths is realized (λ_1, λ_2, λ_3, and λ_4) at the port M_1 at the same moment (shown in figure 5(a)). Figure 5(a) is a 3-dimensional representation with wavelength on the X-axis (representing the 4 channels), time on the Y-axis and power (normalized) on the vertical axis. The ONoC tool analyses the 4 outputs T_1, T_2, T_3 and T_4 (T_2 shown in figure 5(b)). As predicted in table 4(a), only λ_3 is detected at the output T_2.



(a) Input M_1 (b) Output T_2

Figure 5. VHDL-AMS simulation

It is necessary to carry out a low level simulation ("physical" analysis) with the FDTD tool.

Several measures on simple optical filters (in SOI technology) have been realized and validate the model.

References

[1] A. Taflove. *Computational electrodynamics - The Finite-Difference Time-Domain Method*. Artech House, 1995.

[2] A. Vachoux, J. M. Bergé, O. Levia, and J. Raillard. *Analog and Mixed Signal Hardware Description Languages*. Kluwer Academic Publishers, 1997.