A Digital Test for First-Order ΣΔ Modulators

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Abstract

This paper presents a digital structural test for first order Sigma-Delta modulators. A periodic digital sequence is used as a stimulus to obtain a signature of the integrator leakage. This parameter is known to be related to the modulator precision and its estimation is of great importance to assess if the modulator works as expected. As the proposed technique is fully digital, it is specially suitable to test modulators embedded in complex Mixed-Signal circuits.

1. Introduction

Since the apparition of ΣΔ modulation concept, A/D converters based on this principle have gained a wide acceptance and can be found in a large variety of applications. Though many of these applications use high order ΣΔ modulators with a complex architecture, the first-order single-bit modulator is still an important building block. It can be found in multistage ΣΔ modulators [1] or also in large mixed-signal systems for low-accuracy analog-to-digital conversion. Recently, the use of first-order ΣΔ modulators has been proved efficient in the context of Built-In Self-Test (BIST) for analog circuits[2,3].

The 1st order ΣΔ modulator exhibits a very specific behaviour related to non-linear dynamics. One well-known example of such a behaviour is the appearance of limit cycles for rational DC input. This phenomenon is strengthened when the integrator is leaky, as limit cycles become stable over a given range of DC inputs [4]. Therefore, this phenomenon greatly decreases the resolution of the converter and may be critical for some applications. In [5], Huang and Cheng propose to use slow ramps as a test stimulus to measure some step width of the modulator DC transfer function. Indeed, the domain of existence of a limit cycle other than (-1 1) is related to the integrator leakage [4]. Nevertheless, the use of this kind of stimulus may not be sufficiently area efficient if the ramps have to be generated on-chip. Moreover, their simulations show that integrator leakage could be not always detected.

What is intended in this paper is to provide a fully digital test for the integrator leakage of first order ΣΔ modulators. The test strategy is similar to what was proposed in [6] for 2nd order modulators, but it will be shown that the case of the first-order single-bit ΣΔ modulator is much less straightforward than it could be thought.

2. The test

A simple scheme of the proposed test is shown in Figure 1. A digital sequence of period *L* with *(L-1)* "1" and 1 "-1" is sent to the modulator under test and the output bitstream is summed over a number of sample N. The integrator leakage is modelled in Figure 1 as a pole *p* with a value different from 1. If the integrator is ideal (i.e. *p=1*), the sum of the output bitstream is equal to the sum of the input sequence. Otherwise, the corresponding deviation depends on the integrator leakage. An input-referred offset (*off*) is also considered.

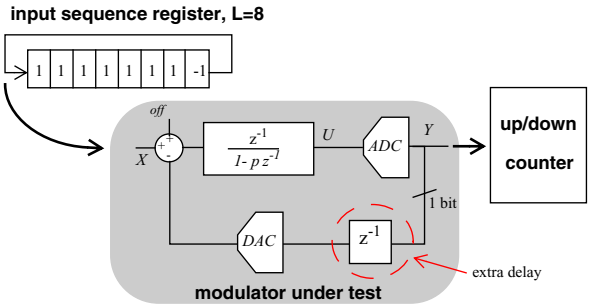

Fig. 1: Basic test scheme

For test purpose, the modulator has to be slightly modified. Its clocking is modified such that the feedback DAC (Digital to Analog Converter) is used to generate both the feedback signal and the input test sequence. Moreover, the addition of an extra delay in the feedback path is necessary. If this delay is not introduced, the output bitstream always follows the input sequence [7].

When the integrator presents no leakage, a simple time-domain step-by-step analysis shows that the integrator output *U* follows a pattern of period *2L* which can be easily

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determined. The integrator leakage acts as a perturbation on this ideal response that has the shape of an exponential decay. This small perturbation breaks the ideal pattern periodically, every k pattern periods (that is every $2kL$ samples). This term k can be calculated using the modulator behavioural model. This tedious calculation is not presented here for the sake of brevity. It comes,

$$k = \left\lceil \frac{\ln\left(max\left(0, \frac{\alpha}{\alpha - (1-p^{2L})u_{mid}}\right)\right)}{2L\ln(p)} \right\rceil \quad (1)$$

with

$$\alpha = -2 + 2p^{L-2} + 2p^{L-3} - 2p^{L} + off\frac{1-p^{2L}}{1-p} \quad (2)$$

and

$$u_{mid} = -2 + 2p^{L-2} + 2p^{L-3} \quad (3)$$

During the calculation of k, it also comes that the input sequence period L should be higher than 5.

While the integrator follows the ideal pattern, the modulator output bitstream is periodic and its mean value is equal to the input sequence mean value. But when the pattern is broken, a small change is introduced in the output bitstream, modifying the overall mean value. It can be shown that the sum of the output bitstream over N samples is,

$$counter = N\frac{L-2}{L} - 2\left\lfloor \frac{N}{2Lk+L} \right\rfloor \quad (4)$$

The proposed test strategy was simulated in Matlab using a Simulink model of the scheme in Figure 1. An input referred offset *off=0.001* was introduced. The output bitstream was summed over 10000 samples for an input sequence of length *L=6* (5 "1" and 1 "-1") and its opposite (5"-1" and 1 "1"). A random noise of 80dB below full-scale was summed to the digital input sequences. Figure 2 shows the absolute value of the simulated and expected counter outputs as function of the integrator leakage p. The matching between the expected and the simulated values is very good. The counter outputs exhibit a strong dependency on the integrator leakage but also on the input-referred offset. Hence, a combination of the results from different sequences, in particular from a sequence and its opposite, may be used to derive estimates of the modulator integrator leakage and input referred offset. More work is being done to make a proper use of linear approximations of Eq. (4) and to maximize the measurements precision.

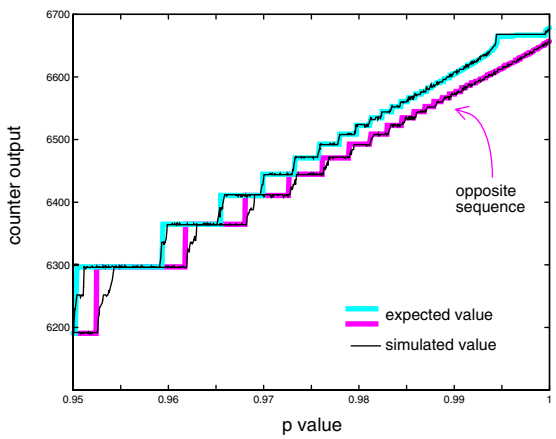

Fig. 2: Counter output for the input sequence L=6 and an offset of 0.001

3. Conclusions

A digital procedure has been presented to test the integrator leakage in a first-order single-bit sigma-delta modulator. This parameter is known to be related to the sigma-delta converter precision and its estimation is of great importance to assess if the modulator works as expected. The simulations presented here seem very promising. The generated signature has been shown to have a strong dependence on integrator leakage but also on input-referred offset. Therefore, the proposed procedure could be used for the test of these two parameters.

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4. References

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