A 0.18 µm CMOS Implementation of On-chip Analogue Test Signal Generation from Digital Test Patterns

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Abstract

The test of Analogue and Mixed-Signal (AMS) cores requires the use of expensive AMS testers and accessibility to internal analogue nodes. The test cost can be considerably reduced by the use of Built-In-Self-Test (BIST) techniques. One of these techniques consists in generating analogue test signals from digital test patterns (obtained via ΣΔ modulation) and converting the responses of the analogue modules into digital signatures that are compared with the expected ones. This paper presents an implementation of the analogue test signal generation part that includes programmability of the circuit blocks, leading to an improvement of performance and a reduction of circuit size with respect to previous approaches. A 0.18 µm CMOS circuit has been designed and fabricated, allowing the generation of test signals ranging from 10 Hz to 1 MHz.

1. Introduction

The on-chip generation of analogue test signals by low-pass filtering a periodically reproduced bit-stream previously encoded via sigma-delta modulation was proposed in [1]. This technique is especially suitable for the generation of single and multi tone test signals, producing high quality signals that are not susceptible to filter shape.

In this paper, we will show an improved realization of this technique. The improvement comes from the programmability of the shift-register length and the sampling frequency, allowing the generation of higher quality tones with a reduction of circuit size. This is because shorter digital test patterns need to be scanned into the chip for generating tones at low and moderate frequencies.

The paper is organized as follows. Section 2 presents the technique used for analogue signal generation and describes a CAD tool developed so as to obtain and optimize the digital test pattern. Section 3 shows the implementation in 0.18 µm CMOS and displays the actual chip test results. Finally, Section 4 concludes this paper with a summary of our current and future work.

2. Technique and digital test pattern generation

The principle of operation of the technique proposed in [1] is shown in Figure 1. A short digital test pattern that encodes the desired analogue test signal (via S? modulation) is initially scanned into a shift-register during a first phase T1. In a second phase T2, the output of the shift register is connected to its input and the bit stream is periodically reproduced.

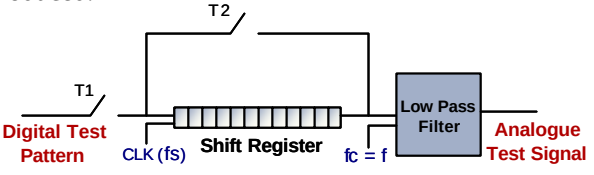

Figure 1. Principle of Operation

It is well known [2] that by repeating a set of N samples loaded into a shift-register that is clocked at frequency f_s, the spectrum of the signal at the register output will contain a discrete number of coherent frequency components given by:

$$f = \frac{M}{N} f_s \qquad M = 0,1,2,3,..., \frac{N}{2} \qquad (1)$$

where f_s is the sampling frequency and M=1 corresponds to the fundamental frequency. The oversampling low-pass ΣΔ modulator pushes the quantization noise to higher frequencies. The higher the oversampling ratio OSR=$f_s/2f$, the higher the signal quality. We can obtain higher quality results with better frequency resolution if, rather than changing the number of harmonic M, we always generate the fundamental frequency (M=1) and we choose adequate values of sampling frequency and shift-register length. Programmable control of the shift-register length can be easily achieved. Programming of the sampling frequency can also be attained by simple division of the chip clock by a power of two.

In order to efficiently eliminate this quantization noise the filter has to be of an order higher than that of the modulator. In addition, the filter must have a good linear behaviour such as it does not modulate the high frequency noise back to our band of interest [3].

The architecture is shown in Figure 2. The shift register has a length programmable from 100 until 200 bits. For comparison purposes, an additional shift-register length of 1024 bits can be programmed. The frequency divider is programmable with a division factor that ranges from 1 to 524288(=2^{19}). A switched-capacitor filter bank can be programmed to perform low-pass filter functions from 2nd to 6th order. The cut-off frequency f_c of the filter is equal to the desired frequency f. The digital test pattern contains two

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parts: one that gets loaded into a control register for programming the circuit, and another one that gets loaded into the shift-register and codes the desired signal.

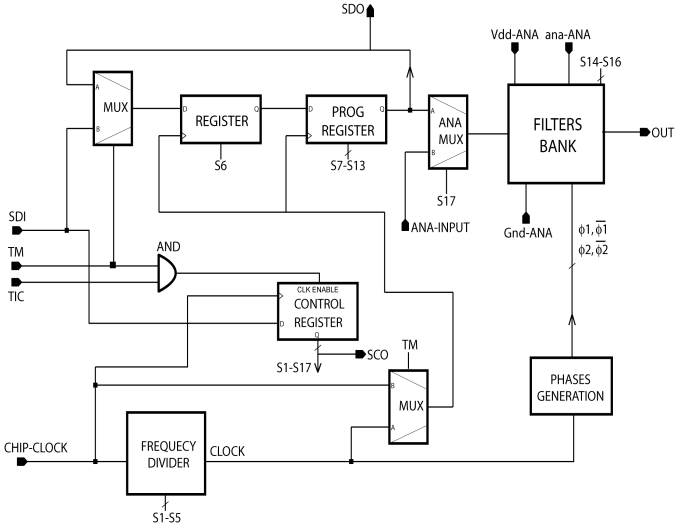

Figure 2. Circuit architecture for on-chip analogue test signal generation from digital test patterns

In order to obtain the digital test pattern a CAD tool has been developed. This software permits to find the adequate input signal phase optimizing at the same time the parameters that characterizes the signal quality: SFDR (Spurious Free Dynamic Range), THD (Total Harmonic Distorsion), Adev (Amplitude Deviation), Peak-to-Peak and RMS (Root-Mean-Square). This optimisation can be performed by three different algorithms: Montecarlo, WARGA (Weighted Average Ranking Genetic Algorithm) and NSGA (Non-Dominated Sorting Genetic Algorithm). After a few iterations, the optimal test pattern generation is worked out and the bit-stream is saved in a file ready to be scanned into the digital tester.

A significant point in the evaluation of this technique is the fact that the results obtained for N even are much better then the results obtained for N odd. Thus the pattern length has to be limited to N even. Despite this, the resolution frequency is still better than 1% with a maximum output frequency equals to 1% of the clock frequency.

3. Actual 0.18 µm CMOS chip results

This strategy has been implemented in 0.18µm CMOS technology from STMicroelectronics. We can see in the Figure 2 that the frequency divider allows us to choose the sampling frequency by means of bits S_1-S_5. The shift register length is controlled by bits S_7-S_{13} permitting to vary the length between 100 and 200 bits. Additionally, bit S_6 makes possible the utilisation of a 1024 bit pattern for comparison purposes. The bits S_{14}-S_{16} program the order of the switched-capacitor filter bank (order 2 to 6). The bit S_{17} allows to directly take an analogue input to the filter.

The filter bank is composed of four 1st and 2nd order Rauch filters with programmable capacitances. The result is a low-pass Butterworth filter of second to sixth order.

A photo of the fabricated chip is shown in Figure 3. The full design architecture has been included in the right part of the chip. The silicon area overhead by this full architecture is 1mm^2. The simplest architecture including only a 3rd order filter and a programmable shift-register length up to 200 bits is included in the left part of the chip, with an overhead area of 0.500mm^2. The central part is dedicated to other purposes.

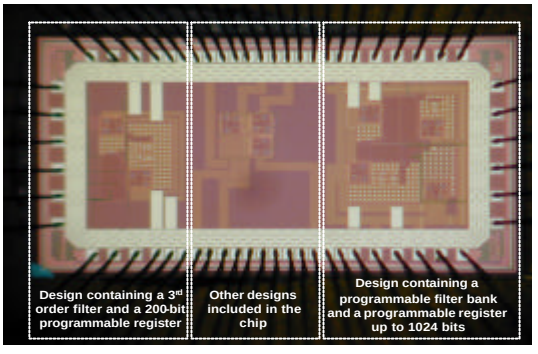

Figure 3. Photo of the fabricated chip

The test results confirm that the circuits works correctly for all orders (2 to 6) allowing the generation of single tones between 10 Hz and 1 MHz, with a SFDR always better than 42 dB, achieving until 53 dB for some frequencies. Figure 4 shows the snapshot and the spectrum of a single tone signal at 2.02 kHz generated from 198 bits.

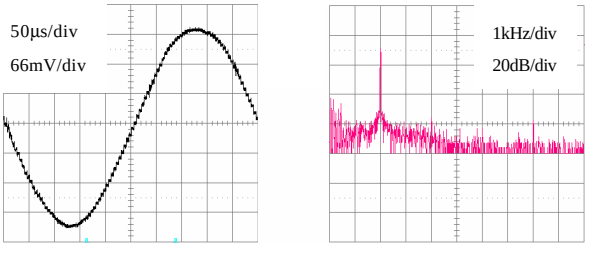

Figure 4. Experimental result with a single tone at 2.02 kHz

6. Conclusions and future work

A technique for on-chip analogue test signal generation from digital test patterns has been validated and implemented. The test results have confirmed the advantage, in terms of quality, frequency resolution and overhead area, of using programmable length and sampling frequency instead of a fixed length of 1024 bits. Future work will include the analysis of the analogue response.

References

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