A Direct Bootstrapped CMOS Large Capacitive–Load Driver Circuit

José C. García, Juan A. Montiel–Nelson, J. Sosa & Héctor Navarro *
Institute for Applied Microelectronics, Department of Electronic Engineering and Automation,
University of Las Palmas de Gran Canaria
E–35017 Las Palmas de Gran Canaria, Spain. E–mail: jcgarcia@iuma.ulpgc.es

Abstract

A new $2.5V$ CMOS large capacitive–load driver circuit, using a direct bootstrap technique, for low–voltage CMOS VLSI digital design is presented. The proposed driver circuit exhibits a high speed and low power consumption to drive large capacitive loads. We compare our driver structure with the direct bootstrap circuit [1] in terms of the product of three metrics, active area, propagation time delay and power consumption. Results demonstrate the superior performance of the proposed driver circuit.

1. Introduction

For next–generation CMOS VLSI circuits, low supply voltage is the unavoidable trend. The development of new CMOS drivers capable of working at reduced power supplies makes it the top objective for many VLSI applications.

In a practical driver, *bootstrapping* [1, 2] is a dynamic circuit technique that obtains a full rail–to–rail output swing and reduces propagation time delays. Such technique uses a capacitor to couple charge from a source. The charge boosts an internal node or output node above the power supply voltage, achieving a full output voltage swing and a high switching speed. Indirect bootstrap consists in connecting a node of the bootstrap capacitor to the gate of the output device — NMOS/PMOS transistor — of the driver circuit. Whereas, in direct bootstrap, a node of the bootstrap capacitor is the output port of the driver. The effectivenes of the direct bootstrap technique used in the driver circuit is determined by the bootstrap capacitor.

This paper presents a comparison between two direct bootstrapped driver circuits. The driver circuits are based on the scheme of a sub–1V CMOS large capacitive load driver circuit using direct bootstrap technique [1]. Section 2 and 3 refer to the circuit topology and operation of our driver, respectively. Section 4 focuses on performance evaluation and comparisons.

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2. Driver Circuit Structures

D-driver relates the circuit driver in [1]. The proposed circuit (*M–driver*) is illustrated in Figure 1.

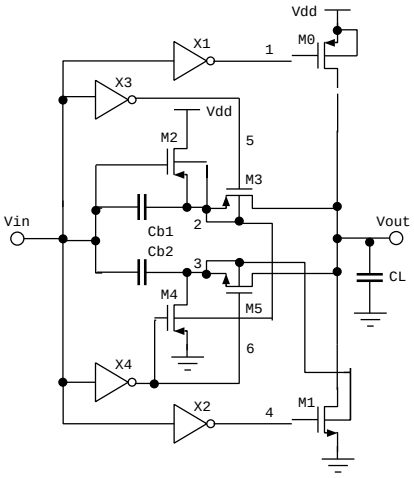

Figure 1. M–driver.

As a key improvement, we have enhanced the driving capability of nodes `1` and `4`. Instead of connecting pass transistors `M3` and `M5` to nodes `1` and `4`, their gate channels are controlled by inverters `X3` and `X4`, respectively. Outperforming the power consumption of the driver circuit in [1] is carried out by the inverter `X4`, which controls the transistor `M4`.

3. Circuit Operation

The structure of the driver shown in Figure 1 consists in three stages, namely, controlling signal circuit, positive and negative pumping circuit, and, driving circuit.

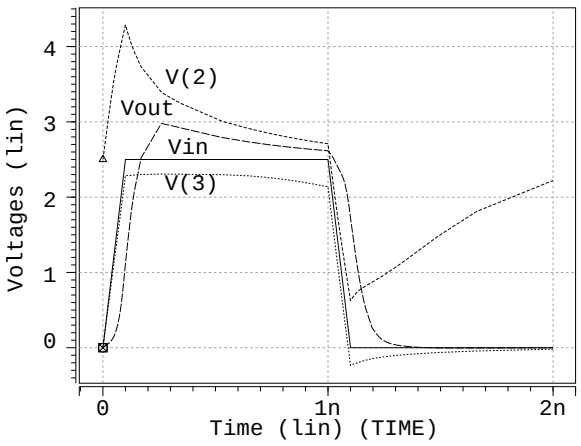

Figure 2. Voltage waveforms of M–driver.

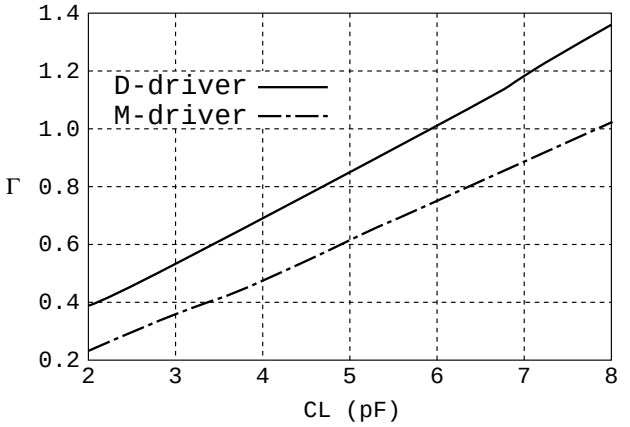

Figure 3. Delay $\times$ Active Area $\times$ Power versus load capacitance.

The controlling signal circuit is composed of the inverters `X1`, `X2`, `X3` and `X4`. They generate inverting signal of the input port `Vin`. `X1` and `X2` control pull–up and pull–down transistors `M0` and `M1`, respectively. Whereas `X3` and `X4` control a pass transistor to directly pull–up/down the output port, respectively.

The second stage is a positive and negative pumping circuit. It consists of a transistor with one pumping capacitor for positive and negative voltage pumping. The last stage is the driving circuit, it is composed of a pair of PMOS and NMOS transistors, `M0` and `M1`, respectively.

Prior to pull–up operation, the bootstrapping capacitor `Cb1` is precharged to `Vdd` through `M2`. During pull–up cycle, node `Vin` is at high logic level (*high*) and `V(1)`, `V(5)` and `V(6)` — logic levels of node `1`, `5`, and `6`, respectively — are at low logic level (*low*), causing `M0` and `M3` to turn on, and `M2` to turn off. When `M3` is on, nodes `2` and `Vout` are bootstrapped, and output node `Vout` is quickly pulled to *high*. While `M4` turns on precharging `Cb2` to *high*, `V(6)` and `V(4)` are *low*. Therefore, `M5` and `M1` are turned off.

During pull–down operation, node `Vin` is *low* and `V(1)`, `V(2)`, `V(5)` and `V(6)` are *high*, causing `M5` and `M1` to turn on, and `M4` to turn off. When `M5` turns on, nodes `3` and `Vout` are bootstrapped, and the output is quickly pulled to *low*. While `M2` turns on precharging `Cb1` to *high*, `V(5)` and `V(1)` are *high*. Therefore, `M3` and `M0` are turned off. Figure 2 illustrates the voltage waveforms of the nodes `2`, `3`, `Vin` and `Vout`. Note that the output voltage may surpass to $2.9V$ for a short period time.

4. Comparative Evaluation

In this section, we compare the performance of the novel driver circuit *M–driver* against the best published direct bootstrapped driver circuit [1]. We designed both circuits using a $0.25\mu m$ CMOS SALICIDE $2.5V$ process from UMC. The circuits were used to drive a clock signal of $500MHz$, and $100ps$ of rise and fall times. The driver circuits were loaded with capacitances from $2pF$ to $8pF$ representing a clock network capacitive loading.

To provide a fairer comparison between drivers circuits, we define a Figure of Merit (Γ), as the product of the performance active area, delay and power.

Figure 3 illustrates Γ in terms of the load capacitance for the drivers. Γ is defined as $nJ \times \mu m^2$. It is shown that *M–driver* has the best Figure of Merit. In particular, *M–driver* is a 30% faster, and consumes 20% less power than the conventional *D–driver*. *M–driver* circuit occupies an active area of $84\mu m^2$, that is an increment of 8% in comparison with *D–driver* circuit ($78\mu m^2$).

5. Conclusions

In this paper, we have introduced a new direct bootstrapped CMOS driver, termed *M–driver*. Using a $0.25\mu m$ CMOS SALICIDE $2.5V$ process from UMC, this circuit exposes the best compromise in terms of speed, power and active area in comparison with *D–driver* [1].

References

[1] P. C. Chen and J. B. Kuo, "Sub–1V CMOS large capacitive–load driver circuit using direct bootstrap technique for low–voltage CMOS VLSI," *Electronics Letters*, vol. 38, no. 6, pp. 265–266, Mar. 2002.

[2] J. H. Lou and J. B. Kuo, "A 1.5-V Full–Swing Bootstrapped CMOS Large Capacitive–Load Driver Circuit Suitable for Low–Voltage CMOS VLSI," *IEEE J. Solid–State Circuits*, vol. 32, no. 1, pp. 119–121, Jan. 1997.